A Germanium Nanowire Reconfigurable Transistor Model for Predictive Technology Evaluation

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***Abstract*—Reconfigurable Field Effect Transistors can be electrostatically programmed to p- or n-type behavior. This device level reconfigurability is a promising way to enhance the functionality of digital circuits. Here, we present a Verilog-A based *Germanium* nanowire table model for the analysis of dynamically reconfigurable logic gates. The model is based on TCAD simulations of a nanowire transistor design with feature sizes compatible to a 14nm FinFET process. To showcase that our model enables digital circuit design for reconfigurable operation, performance and power consumption estimations for basic static as well as reconfigurable logic cells are given. Performance improvements over *Silicon* nanowire based designs are predicted, making Germanium RFETs a promising candidate for future co-integration into standard CMOS processes.**

***Index Terms*—reconfigurable transistor, functionally enhanced logic gates, germanium, RFET, MIGRFET, TIGFET**

I. Introduction

CONTINUOUS down scaling of the individual transistor feature sizes has been the main driver of today's complementary metal-oxide-semiconductor (CMOS) industry over the last 50 years. However, reaching below 10 nm nodes the fabrication of electronic systems has become increasingly expensive and complicated [1]. Thus, the quest for alternative solutions, which increase the circuit functionality without increasing the physical number of elements on chip has been going on from last decade. A widely explored approach to yield added benefit is the integration of embedded non-volatile memory elements, e.g. for memory in logic [2]–[5]. Typically, these elements rely on the integration of new materials into the front-end of line.

Another, more disruptive approach to add value to a given circuit are reconfigurable field effect transistors (RFET) with electrically controllable polarity [6]–[8]. Due to their inherent polymorphic nature, reconfigurable transistors are promising building blocks for many applications including, field programmable gate arrays, signal-processing at the edge, and hardware security, as well as future design paradigms like machine learning and asynchronous or approximate computing [9]–[15]. Beneficially, all materials and processes needed for those type of transistors are available in standard CMOS fabrication. At the laboratory demonstrator level, reconfigurable devices can be built on a variety of channel materials, ranging from FinFETs [16], to one-dimensional silicon [6], [8] and germanium nanowires [17], [18], and carbon nanotubes (CNTs) to 2D layered materials, such as graphene [19] or WSe_2 [20]. However, most work on circuit development has been focused on silicon as base material. In contrast, little work has been done on germanium-based devices.

Germanium is an especially promising channel material for RFETs, due to its integrability with standard CMOS processes paired with its low-bandgap [21]. As a result, a higher performance as compared to silicon channels of similar feature sizes are expected. Lab-scale device demonstrators on germanium nanowires have been shown [17], [18]. Recently scaling trends have been predicted [22]. However, up till now a comprehensive model to predictably analyze circuit designs built from germanium-based reconfigurable technologies was missing. In this paper, we introduce a Spice Verilog-A model derived from 14 nm FinFET process [23] optimized towards a reconfigurable germanium nanowire implementation. The Verilog-A model data files are available for download in the supplementary information.

The individual contributions of the work are:

- It provides a profound prediction of germanium nanowires as channel material for scaled reconfigurable devices, showcasing a 64% benefit in inverter delay over a silicon nanowire technology model with similar feature size
- It provides a table model compliant with circuit level simulation tools for predictive technology analysis
- It gives delay and power estimations for basic static as well as reconfigurable logic cells of this technology
- A 1-bit full-adder is analyzed as case study showing a critical path delay of 16.5 ps

The remainder of the paper is organized as follows: Section II provides an introduction into RFET technology and its applications. In section III, the predictive germanium technology model is explained. In section IV, the model capabilities are exemplified by transient analysis of individual logic gates, extraction of performance metrics, as well as a circuit design case study. Finally, in section V, steps towards a standard cell library based on or model are elucidated. Section VI concludes the paper.

II. Background and Motivation

A. Reconfigurable Transistors

1) Principle: Reconfigurable transistors merge the two basic elements of CMOS logic into one type of transistor [9],

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employing a structure with two or more independent gate electrodes. The operating principle is based on a selective charge carrier filtering capability in ambipolar Schottky barrier transistors. Traditional ambipolar transistors exhibit electron and hole transport and an absence of a clear off-state over a wide gate voltage range, causing a limited usability for complementary metal oxide semiconductor (CMOS) technology based circuitry. In reconfigurable transistors, the off-state is enabled by a potential barrier for one type of charge carriers. The barrier is formed by applying a voltage to the so-called program or polarity gates (PG) leading to a p- or n-type transistor function as shown in Fig.1. The control gate (CG) electrode is controlling the conduction of the device, acting as the usual CMOS gate electrode.

2) Design Variants: Depending on the number and placement of the PG and CGs, a number of RFET design variants are known in literature. Most works have been focused on either two top-gates [6] or three top-gates [7]. However, variants with four or more independent gate electrodes have been shown as well [24]. In some variants a back-gate is used instead [13], [25]. Depending on the number of gates along the direction of carrier flow, different properties result for the different variants. For example, RFETs with two gates typically exhibit lower off-currents while the variants with three or more gates show a steeper subthreshold slope of the transfer characteristics, since in the latter case, only thermally activated charge carriers are controlled. Depending on the bias conditions even steep subthreshold slopes below 60 mV/dec at room temperature have been demonstrated [26], [27]. The steeper transfer curve allows for a lower operating voltage, which is crucial for the power consumption of the circuit. For this reason, a three gated variant is chosen for the analysis in this work.

3) Material, Ge: Being based on Schottky contacts, lowering the threshold voltage and increasing the drive currents are two of the main challenges for RFET development. Both can be addressed by low-band channel materials such as Ge or InAs. By lowering the bandgap, the combined sum of p- and n-type Schottky barrier will also be decreased. As a trade-off higher static off-currents are expected. Ge and SiGe are especially promising, because they are already applied in CMOS technology for boosting p-channel performance [28].

B. Circuit Design Opportunities

1) Gate Level Design Features: In recent years a number of gate level features have been demonstrated for RFETs, which provide an added benefit over their CMOS counterparts: dynamic reconfiguration [29], intrinsic XOR [7] and wired-AND capabilities [24], threshold voltage control [30] and suppression of parasitic charge sharing effects in dynamic logic gates [31], [32]. This higher expressive capability of RFETs can be exploited to yield circuit designs with a higher compactness. Pioneer studies have shown that overall chip area can be saved albeit the larger size of the individual devices [10]. For example a 1-bit full adder built from silicon RFETs needs up to 42% less area than its CMOS counterpart [33].

2) Future Applications: Reconfigurable transistor concepts have been proposed for the co-integration of a number of add-on functionalities into classical CMOS, which go beyond general computing purposes. The polymorphic nature of RFET circuits enables new takes on hardware security solutions particularly IP protection schemes, such as logic locking, camouflaging, hardware watermarking, physically unclonable functions (PUFs) or chip authentication [12], [34]–[36]. RFETs-based XOR cells and flip-flops have been shown to be less prone to delay-side-channel attacks as their CMOS counterpart [37], [38]. Beyond that, RFETs have a high potential for new operation schemes, such as asynchronous or neuromorphic computing. For example a synaptic cell, which needs only three transistors to emulate a spiking behavior has been proposed recently [14].

3) Model Limitations: In the past, most work on RFET-based circuits has been focused on the logic gate level, due to a lack of circuit simulator compliant models. Albeit first compact models have been proposed in literature, they typically fall short describing the reconfiguration event [39], [40].Also they are often based on large-scale Si channel devices [41]. Here, a predictive Ge nanowire table model is proposed as an alternative to stimulate development of RFET based circuit designs.

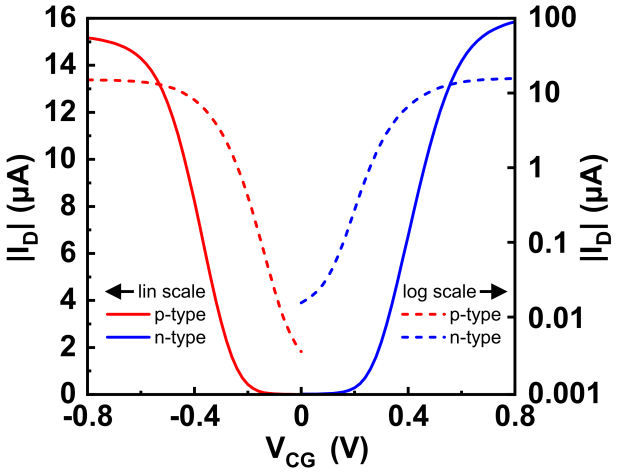

Fig. 1: Simulated transfer characteristics in linear (full lines) and logarithmic (dashed lines) scale of a single Ge-NW-RFET structure related to the 14 nm TCAD model for n-type (blue, $V_D = 0.8\,\mathrm{V}$, $V_{PG} = 0.8\,\mathrm{V}$) as well as p-type (reed, $V_D = -0.8\,\mathrm{V}$, $V_{PG} = -0.8\,\mathrm{V}$) configuration.

III. Germanium Nanowire Models

The main aim for our predictive germanium nanowire model is to be structural compliant with an established integrated process, ensuring exploration as an add-on functionality. For reasons elucidated hereafter we have chosen the 14nm FinFET process from Intel as reference process [23]. Key layout features are kept identical, such as contacted poly pitch (CPP) of 70 nm, fin pitch of 42 nm, equivalent oxide thickness (EOT) of 0.8 nm, and a via size compliant with a metal 0 pitch of 56 nm. The structural features of the device are shown in Fig. 2. First, a table comprising the data for the complex behaviour of the surface potential as a function of the three potentials V_D, V_{PG} and V_{CG} was generated from TCAD. Second, a Verilog-A implementation enabling a usage in SPICE was developed.

A. Predictive 14 nm TCAD Model

1) Device Parameter: As a starting point for the geometrical parameters, an optimum for the nanowire thickness t_{NW} was examined. As seen in Fig. 3, the drain current of the transistor increases at first with the shrinking of the channel diameter

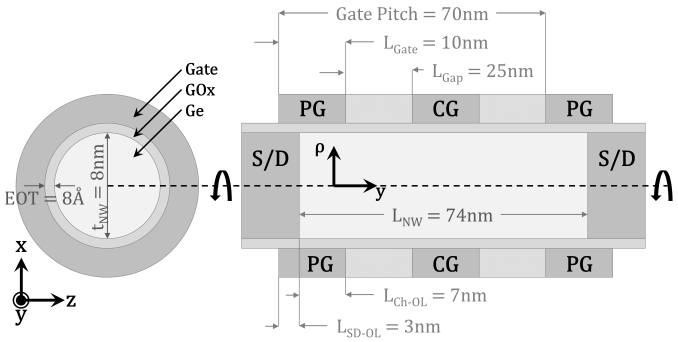

Fig. 2: Simulated nanowire structure for TCAD model including the dimensions compliant to a $14nm$ technology node.

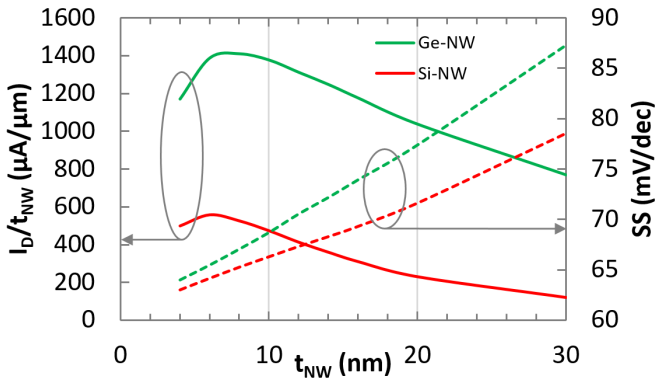

Fig. 3: Drain current normalized to the nanowire diameter as well as subthreshold swing as functions of the nanowire diameter of a simulated Ge-NW-RFET (green) as well as Si-NW-RFET (red). $V_D = 0.8\,\mathrm{V}$, $V_{PG} = 0.8\,\mathrm{V}$ and $V_{CG} = 0.8\,\mathrm{V}$

due to the progressively stronger band bending in the area of the Schottky junctions. However, once the limit of the density of states is reached, the total current decreases again due to the further reduction in channel cross-section. Based on this a t_{NW} of $8\,\mathrm{nm}$ was chosen here as the optimum wire geometry regarding current per width, albeit the on/off ratio would be further increased and the subthreshold swing would be reduced with smaller diameters. A matching and a comparable CMOS technology is the $14nm$ technology node from $Intel$ which has $8\,\mathrm{nm}$ as the *Fin* width [23]. Note, that, in principle, multiple vertically stacked nanowires could be integrated within a single fin [7], [42]. In order to ensure the comparability of circuit designs, a gate pitch of $70nm$ was adopted between the two program gates (matching the CPP). The control gate structure can be added by a self-aligned process as described in [43]. The self-aligned contact formation has to be adjusted to yield a metal/semiconductor transition below the program gates. The gate dielectric was assumed to have an identical EOT of $EOT = 8\,\text{Å}$ corresponding to a 3.0 nm HfO_2 high-k layer with 0.6 nm GeO_2 interface. The patterned gate lengths as well as the gaps between them were optimized under the aspects of ensuring gate control and reduction of parasitics [22].

2) Simulation Parameters and Models: The models used were drift-diffusion with modified local-density approximation, non-local tunneling based on Wentzel-Kramers-Brillouin approximation for finite-element-method, high-field mobility saturation and surface scattering. In most cases, the default

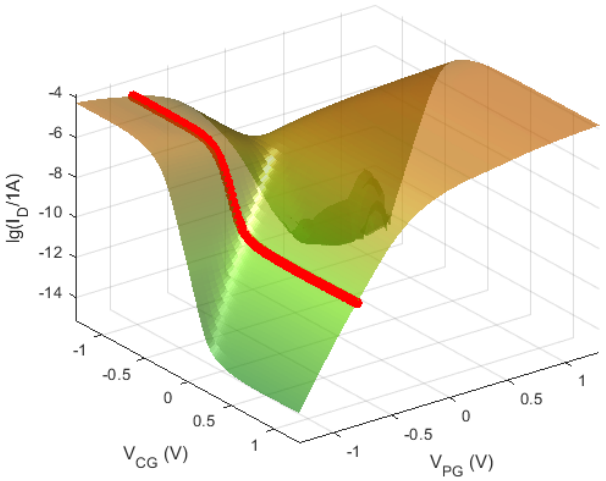

Fig. 4: TCAD simulation of a drain current field in logarithmic scale at $V_D = -0.8\,\mathrm{V}$. The red line shows the transfer characteristic for $V_{PG} = -0.8\,\mathrm{V}$.

values of the models were used. The effective tunneling masses of electrons and holes were assumed to be $m_e = 0.08 \cdot m_0$ and $m_h = 0.044 \cdot m_0$, respectively [44]. For the theoretical observations of this study, only the work functions of the source and drain regions ($W_{SD} = 4.34\,\mathrm{eV}$) as well as the work function of all gates ($W_G = 4.33\,\mathrm{eV}$) have been arbitrarily adjusted to realise a fairly symmetric static drain current (on-state) behaviour for the n- and the p-configuration of a single germanium nanowire RFET at $V_{DD} = 0.8\,\mathrm{V}$. As shown in previous studies of Silicon RFETs, a symmetrical I-V behavior between n- and p-configuration could also be achieved by the impact of mechanical stress on the carrier injection at the Schottky junctions [45]. This can also be applied to Ge RFETs.

3) Simulation Data Output: The dependence of the currents, capacities and charges on the three potentials (V_D, V_{PG} and V_{CG}) mentioned above results in a four-dimensional data field, respectively. Please note, that the two program gate terminals are assumed to be short-circuited and therefore always have the same potential V_{PG}. For instance, the transfer characteristic field for $V_D = -0.8\,\mathrm{V}$ is illustrated as three-dimensional logarithmic plot (Fig. 4) instead of a single curve. All simulation data are transferred to a table having a structure as shown in Table I. The applied voltages V_D, V_{PG}, and V_{CG} are swept from $-1.3\,\mathrm{V}$ to $+1.3\,\mathrm{V}$ at intervals of $50\,\mathrm{mV}$, $50\,\mathrm{mV}$, and $20\,\mathrm{mV}$ respectively, resulting in 367,979 individual bias points, offering a acceptable compromise between computation effort and accuracy for the description of the currents, the contact capacities as well as the contact charges. For each bias point, the drain to source current and the charges at each of the five terminals are stored. The table range is wider than the targeted power supply voltage of $V_{DD} = 0.8\,\mathrm{V}$ to account for over and undershoots in the circuit simulations.

B. Spice Verilog-A Implementation

The table is included in a simple SPICE model, represented by a quasi-static voltage-controlled current source between source and drain and the coupling between each gate, the channel, and its adjacent gates. Due to the three gates influence on each other, the exact charge distribution inside the channel is unknown, but it's net value is the voltage-dependent sum of

TABLE I: Germanium RFET Table Model

Variable	Name	Increment	Sweep Range	Unit
V_{CG}	Control Gate Voltage	0.02	[-1.3;1.3]	V
V_D	Drain Source Voltage	0.05	[-1.3;1.3]	V
V_{PG1}	PG 1 Voltage	0.05	[-1.3;1.3]	V
V_{PG2}	PG 2 Voltage	0.05	[-1.3;1.3]	V
I_D	Drain Current	Dependent Variable		A
Q_{CG}	Charge at CG	Dependent Variable		C
Q_{PG1}	Charge at PG 1	Dependent Variable		C
Q_{PG2}	Charge at PG 2	Dependent Variable		C
Q_S	Charge at Source	Dependent Variable		C
Q_D	Charge at Drain	Dependent Variable		C

the charges outside the channel, which is distributed between the respective terminals (Q_D, Q_{PG1}, Q_{CG}, Q_{PG2}, Q_S). The charge accumulated at each terminal is redistributed due to alterations caused by variation of the respective applied voltage. The current contribution caused by the dynamic switching behavior of a charge can be expressed as:

$$I = dQ/dV * dV/dt$$

Due to the high number of gates up to fifteen voltage-dependent capacitors would be needed to account for the exact coupling between terminals, which is computationally intensive. Instead, the voltage dependent charges Q(V) at each terminal are taken and a quasi-static coupling is assumed, which is modelled with help of a simple coefficient matrix. The splitting of that current is described by the coefficients, assigning for each terminal a factor to each other terminal and to ground.

1) Current Split Coefficients: In our matrix approach, the current towards a node is the scalar product of its respective row of the matrix and the column of charge variations $\frac{\partial}{\partial t}[Q]$:

$$[I] = [S] \cdot \frac{\partial}{\partial t}[Q]$$

$$[S] = \begin{pmatrix} S_{gnd,D} & S_{gnd,PG1} & S_{gnd,CG} & S_{gnd,PG2} & S_{gnd,S} \\ S_{D,D} & S_{D,PG1} & S_{D,CG} & S_{D,PG2} & S_{D,S} \\ S_{PG1,D} & S_{PG1,PG1} & S_{PG1,CG} & S_{PG1,PG2} & S_{PG1,S} \\ S_{CG,D} & S_{CG,PG1} & S_{CG,CG} & S_{CG,PG2} & S_{CG,S} \\ S_{PG2,D} & S_{PG2,PG1} & S_{PG2,CG} & S_{PG2,PG2} & S_{PG2,S} \\ S_{S,D} & S_{S,PG1} & S_{S,CG} & S_{S,PG2} & S_{S,S} \end{pmatrix}$$

where $[I]$ is the vector of current flowing into each terminal (GND, D, PG1, CG, PG2, S) and $[Q]$ is the charge at each terminal as a function of the applied voltages. $[S]$ is the proposed current-split coefficient matrix s_{ij} coefficient represents the coupling between i and j divided by the overall capacitance of j. Inside the matrix, the origin of charges is constant along a column and the destination, along a row. Consequently, the sum of each column must amount to 1. In its most simple form all charge variations are driven from the individual terminals to ground, which is described by $[S_{M1}]$= [1, ... , 1; 0, ..., 0; ...; 0, ..., 0]. Using the Verilog-A model in SPICE the transient switching behavior of a digital inverter was now as compared to a mixed-mode TCAD simulation, assuming the input signal is a rectangular pulse with a period of 100 ps, 0.5 duty cycle and a slope of 0.8 V/ps. An overall accuracy of 0.129 mean square deviation of the SPICE model was achieved. The main differences between both simulations (TCAD and SPICE) are the missing over- and undershoots as well as a little bit higher performance using the SPICE model. Both effects can be attributed to the missing parasitic miller capacitance's, which can be included and tuned by the matrix coefficients.

In order to include those effects, model can be extended by additional a coupling between the CG and D and between CG and S (due to symmetry). Additionally, also a coupling between each PG and its adjacent terminals and vice-versa can be included. Also a comparatively small coupling to ground is assumed to be present, specially for D and S. Considering the capacitance between terminals decaying with their distance, most of a terminal's overall capacitance will lay at the adjacent terminals and at ground. These considerations lead to the development of the following matrix:

$$[S_{M2}] = \begin{pmatrix} 0.1621 & 0.1332 & 0.1260 & 0.1332 & 0.1621 \\ 0.0000 & 0.2717 & 0.1799 & 0.1332 & 0.1135 \\ 0.3308 & 0.0000 & 0.2571 & 0.1902 & 0.1621 \\ 0.2316 & 0.2717 & 0.0000 & 0.2717 & 0.2316 \\ 0.1621 & 0.1902 & 0.2571 & 0.0000 & 0.3308 \\ 0.1135 & 0.1332 & 0.1799 & 0.2717 & 0.0000 \end{pmatrix}$$

The mean square deviation of the inverter when using matrix $[S_{M2}]$ is improved to 0.055 when compared to TCAD. All further simulations of the SPICE model shown in this work have been performed using $[S_{M2}]$.

2) Model Limitations: While the matrix model approach yields a good agreement with TCAD simulations, some limitations should be noted: the model is neither accounting for additional RC parasitic, such as via capacitances, nor accounting for non-quasistationary effects. As side effect of the quasi-stationary approach, nodes receive current contributions slightly different to the actual charge variation according to the TCAD simulation, that is because the coefficients are static. A possible improvement would be to compare the two charge variations and redistribute the difference; converging to the desired precision after enough iterations. In its current form we recommend the model for the development of digital design.

3) Run-time Optimization/Simulation speed improvement: An improvement of the simulation speed is possible by using a reduced version of the table. If the voltage increments of 200 mV at V_D, V_{PG} and 80 mV at V_{CG} are used, the simulation time is reduced at least by a factor of 10 with respect to the time needed when using the whole table. Despite a reduction of 64 times in the table density, the performance of the model coincides for transient simulations up to at least 10 GHz. All the SPICE model simulations shown in this publication have been performed using the simplified table.

IV. Analysis of Reconfigurable Circuits

In order to showcase the capability of our germanium nanowire RFET table model, various test circuits were analyzed regarding their transient behavior under runtime reconfigurable conditions. Circuit level analysis has been carried out using *Cadence Virtuoso* with our GeNW RFET model and the resulting performance metrics are summarized in TABLE II.

A. Boundary Conditions of Circuit Analysis

The following boundary conditions have been assumed for all circuit data discussed in this section:

- If not specified differently, square shaped input signals with a minimum interval of 100 ps were used, corresponding to 10 GHz operation frequency.

- If needed, complementary inputs are generated by an input inverter.
- In all our calculation, we have taken one of the inputs as a constant signal, driven as constant $0V$ or $800mV$. The other signal is a pulse with time period of 100 ps.
- For all calculations a fanout of 1 is assumed. Therefore, two stages of the same logic gate are used, where the first stage drives the load of the second stage. For example, an inverter drives another inverter and a NAND drives another NAND and so on. In case of 2 or more input logic gates, the output of the first stage is connected as one of the inputs of the next stage.
- For delay calculation, we have considered $50\% - 50\%$ measurement. This implies, that for both rise and fall times, we take the time difference starting from the point input signal reaches 50% of the full voltage swing to the point when the output signal reaches 50% of the full voltage swing. The propagation delay is calculated as the average of the rise and fall-delay $D_P = \frac{D_R + D_F}{2}$.
- The static power P_{stat} is calculated using the leakage current and V_{DD} when the logic gate is not switching.
- The capacitance of individual gates is calculated using DC analysis. The capacitance is used to calculate dynamic power. The calculation of dynamic power also requires an activity factor. The values for those are mentioned in the last column of TABLE II.
- The calculation of the short circuit power P_{sc} has been done by integration of current over during the phase the transistor is switching.

B. Transient Behavior of Logic Gates

For the analysis of various logic gates, we have considered three different families of logic gates: static gates without reconfiguration, dynamically reconfigurable gates, and logic gates using inherent reconfigurability [10], [46], [47].

1) Static Logic Gates: Albeit enabling a reconfigurable transport, this feature does not necessarily have to be applied in a given logic gate. V_{DD} and V_{SS} can also be mapped towards the program gates of a circuit in a way, that a static function similar to classical CMOS gate is achieved. This is especially interesting for hardware security techniques, like camouflaging or watermarking [36] or for enabling array-like sea-of-tiles regular circuit designs [48]. For example the design shown in Fig. 6(a) can be used as either NOR or NAND if the program signals are replaced statically with V_{SS} and V_{DD}. Performance data is given in TABLEII for static versions of inverter, 2-input NAND, 2-input NOR, and 2-input XOR gate using the design shown in [10]. Note, that NAND and NOR are not perfectly symmetric due to small differences in the underlying table data. However, the delay ratio of inverter, NOR and XOR matches well with theoretical predictions by the method of logical effort as described in [10], [49]. Further, for the simple inverter a propagation delay as low as 2.1 ps is achieved. This is a 64% reduction as compared to the 5.9 ps we achieved for a silicon based reconfigurable transistor model shown in [33] having similar feature sizes and assuming a C_{min} = 0.1 fF (as convergence parameter) and identical V_{DD}. The performance gain is purely resulting from in the usage of a germanium nanowire channel material, lowering the threshold voltages and increasing the currents. Simultaneously it comes at the expense of increasing the static power dissipation of the inverter from 0.82 nW to 16.3 nW due to the higher off-state leakage currents in the germanium technology.

2) Dynamically Reconfigurable Gates: In this section, we analyze the transient behavior of logic gates, which can be reconfigured by a dedicated program signal P. The first analysis was carried out on a reconfigurable inverter circuit Fig. 5(a). Since inverters are symmetrical regarding their *Pull-Up Network* (PUN) and *Pull-Down Network* (PDN) networks, the logic function after reconfiguration will be identical; the circuit is reconfiguration-invariant [6]. However, inverters pose an interesting model system to observe the behavior during a switching event. Fig. 5(b) shows a parametric sweep over the voltage transfer curves (VTCs) for an inverter circuit with several values of V_P. The gradual change of V_P from V_{DD} to GND, and vice versa for $V_{\bar{P}}$, resembles the potential change inside logic gates during runtime-reconfiguration. It can be seen that with both V_P and $V_{\bar{P}}$ sweeping towards V_{DD}/2, the VTC is first kept intact except for its dynamic range decrease, flattening until it no longer shows an inverting behavior. The reason for this is twofold: first, since the output operates between V_P and $V_{\bar{P}}$, the dynamic range decreases with decreasing program voltage; second, around V_{PG}=V_{DD}/2, RFETs are neither in a stable p- nor n-configuration, but in a low current ambipolar mode always passing current. This can also be observed in the transient case, as shown in Fig. 5(c), where the output signal first follows the program signal (or the inverted program signal). After the stable program state is lost all transistors switch into the ambipolar mode, and nearly no charge is transported anymore. Once the new program gate configuration surpasses this state, the inverter behavior recovers and the output voltage follows the inverted program signal (or the program signal). As a result one can see that the output is rather stable during the reconfiguration event and only small glitches appear in the reconfiguration event. The amplitude of the glitches depends on the output load and on the rise and fall times of the input signal, i.e. the time the devices in the logic gate are "shut down" during reconfiguration. Assuming equal leakage currents, a larger capacitance at the output needs more time to discharge, preventing its value from changing during reconfiguration.

A more application relevant logic gate facilitating runtime-reconfiguration is the NAND/NOR gate shown in Fig. 6(a). As compared to the inverter a higher number of program gates have to be reprogrammed during the reconfiguration event. As a result larger glitches can be observed. Notably, this glitches lead to an undershoot of $370mV$ with P switching from V_{DD} to 0. However, the circuit will retain its full output value within $50ps$, when driving an inverter at the output. Note that the propagation delay induced by the reconfiguration process is roughly 5.5 times larger than that of a normal data input. Thus, here we have used P as a pulse signal with the time period of $300ps$ for data calculation. Design-Technology-Co-Optimization (DTCO) strategies can be used to improve this behavior. For example the usage of multiple independent gates within a single device [24] will largely reduce the number of program gates, which have to be switched at the same time. Also an optimization of the capacitive behavior of the device will help to improve over- and undershoots. In our model such changes can be reflected by changes in the split coefficient matrix $[S_M]$. However, also note that the delay of inputs A and B just pose a small overhead as compared to their static counterparts, making the reconfigurable NAND/NOR (MIN) gate especially promising for applications, where the

functionality is altered occasionally, but not each clock cycle.

3) Exploitation of Internal Reconfiguration: Instead of having a dedicated program signal, some logic gates can also make use of the reconfigurability in a hard-wired configuration. For example a four-transistor 2-XOR variant as proposed in [7] can be derived. Depending on the used process design kit (PDK) up to 26% area gain versus classical CMOS XORs have been predicted for these designs [33]. Interestingly, the compact 2-XOR variant exhibits high signal spikes with nearly every input transition of signal B as shown in Fig. 6(b). This is caused by the internal reconfiguration, which is utilized here. The design exploits the fact, that for all possible input combinations only one presents a strong pull-up or pull-down transistor, while the other three reconfigure either into an off-state or a weak transistor placed into the wrong network. As a result, the overall gate will retain a complementary behavior [50]. One can notice that this XOR version shows much better delay numbers as compared to the static XOR. This is mainly enabled by the reduced number of transistors, which comes also with an reduced total capacitance to be charged. Note, that in contrast the purely *XOR_static* variant shows negligibly over and undershoots, when the input signal switches.

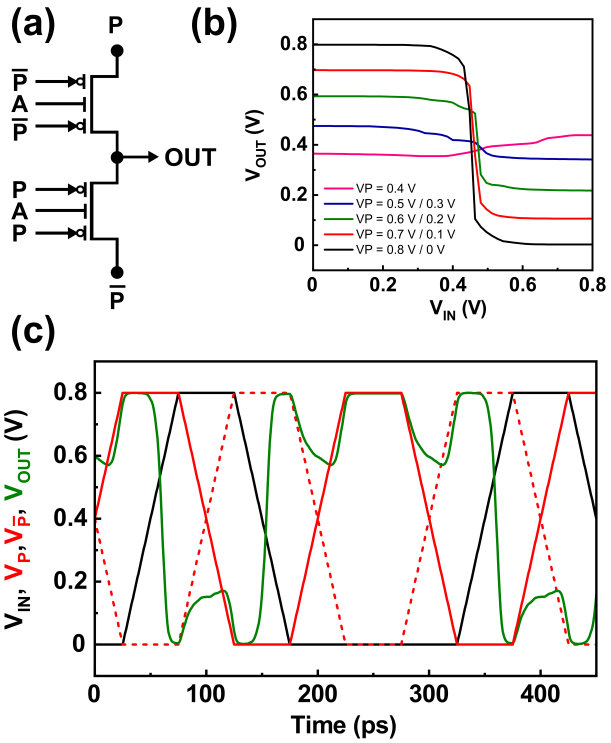

Fig. 5: Dynamically reconfigurable inverter (a) circuit diagram with applied signals (b) dynamic voltage transfer curve (VTC) and (c) transient behavior during the reconfiguration process.

C. Case Study and Scalability

Based on the individual logic gates demonstrated in the last section simple test circuits can be analyzed. To this end we carried out a circuit simulation case study for a compact 1-bit full adder design as proposed by [51]. For our analysis we have used XOR and Majority logic gates with internal reconfiguration to compute the sum and carry respectively. Based on a study by Gore et al. [33] up to 41% area reduction

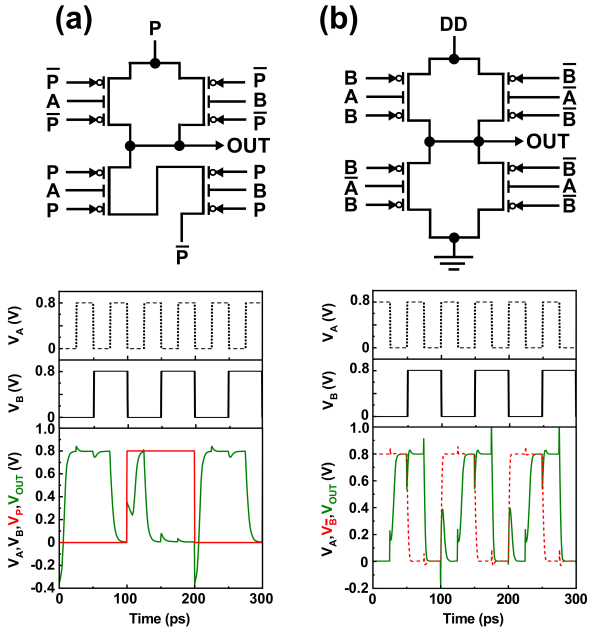

Fig. 6: Base versions of two reconfigurable circuits and their simulated transient behavior. (a) Dynamically reconfigurable NAND/NOR with dedicated program signal, (b) static 2-XOR exploiting internal reconfiguration.

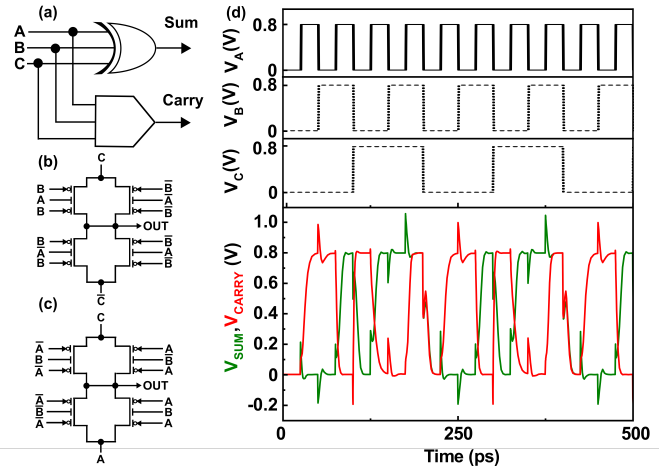

Fig. 7: 1-bit Full adder as proposed in [51]. (a) Generic 1bFA design with separated paths for SUM and Carry function comprise of (b) 3-XOR and (c) 3-MAJ. (d) Transient output sequence for the 1bFA.

can be achieved for such a full adder design. Functional verification by transient analysis is shown in Fig. **??**. As the design makes use of internal reconfiguration, its characteristic over- and undershoots are present. The individual delay values calculated are shown in Table III. Since the input signals are shared between the two logic gates, the delay calculated is larger as compared to the standalone logic gates, resulting in a critical path delay of $16.5ps$. To demonstrate that the proposed model is scalable to larger circuits, we have constructed a cascade of adders to form a 4-bit full adder comprising of 56 devices and 30 internal nodes. On an 8-core workstation complete output waveform over $10ns$ of operation was calculated within 29 minutes and 53 seconds. Reduced table versions further improve speed on cost of exactness.

TABLE II: Delay, capacitance, and power of major logic gates in reconfigurable Ge nanowire technology and Si reference

Logic Gates	Rise-delay (ps)	Fall-delay (ps)	Avg. Delay (ps)	P_{stat} (nW)	Capacitance (fF)	P_{dyn} (nW)	P_{sc} (nW)	Activity factor
Inv (Si Ref. [33])	4.7	7.0	5.9	0.82	n/a	n/a	1794	1/2
Inv	2.2	2.0	2.1	16.3	15.6	49	726	1/2
NAND	2.4	6.5	4.4	17.2	15.6	18.7	507	3/16
NOR	5.4	2.6	4.0	11.0	10.0	12	430	3/16
Minority(A|B, out)	3.9	5.6	4.7	4.61	17.0	2.7	3000	1/4
Minority(P, out)	20.8	31.3	26.0	4.61	17.0	2.7	3000	1/4
XOR_static; Design from [10]	14.7	10.8	12.7	44.6	1443	2270	1410	1/4
XOR(A, out); Design from [7]	6.0	5.5	5.8	82.5	282	451	1020	1/4
XOR(B, out); Design from [7]	8.0	6.8	7.4	82.5	282	451	1020	1/4

TABLE III: 1-bit adder

	Rise-delay (ps)	Fall-delay (ps)	Delay (ps)
	For Carry signal		
A, Output	23.4	9.7	16.5
B, Output	17.6	13.8	15.7
C, Output	12.3	14.0	13.2
	For Sum signal		
A, Output	7.5	14.0	10.4
B, Output	20.0	10.0	15.0
C, Output	3.6	8.3	6.0

V. Towards a Standard Cell Library

In chapter IV we have shown that our germanium nanowire table model has the capability to investigate disruptive circuit designs with RFETs and give a legitimate first-order estimation of delay and power consumption for specific logic gates. As a next step, a standard cell library containing all basic circuit elements has to be derived to enable large scale circuit designs. This still poses a great challenge, because the inherent higher expressive capability of RFET leads to a design space explosion. For example in Raitza et al. [52] it is analyzed that for a basic 3-MIN function there are 16 possible variants, where at least 6 of them are competitive in terms of power or delay for certain use-cases. Note, that this analysis was purely topological and did not yet consider area constraints or resulting parasitic. In order to include those measures a process design kit (PDK) has to be derived to provide design rules check (DRC) and layout versus schematic (LVS) kits as proposed in [33]. In order to foster those developments our germanium nanowire table model is derived from an established industry *FinFET* process, as introduced at the beginning of this paper. Device sizes are chosen in a way that key dimensions, such as contacted poly pitch (CPP), active area pitch, via and metal layer size are kept identical. The nanowire diameter is matched with the Fin width, so that three stacked nanowires can be accommodated by the same area. As both FinFETs and nanowire transistors only scale incremental with active area the same design rules can be applied here. Adjustments probably have to be made in the mid-of-line modules, to ensure a contact of source, drain and all gates to the metal layers. Next liberty and layout files have to be extracted for physical and logical synthesis as proposed by Rai et al. for silicon nanowires [53] in order to generate a germanium nanowire RFET standard cell library and perform benchmark level analysis, such as ISCAS combinatorial circuits.

VI. Conclusions

To sum up, we have presented a germanium nanowire table model for the analysis of dynamically reconfigurable logic gates as potential add-on functionality into classical CMOS. The model is based on TCAD simulations of a nanowire transistor design with feature sizes compatible to a 14 nm FinFET process. Performance and power consumption estimations for basic static as well as reconfigurable logic cells, and a 1-bit full adder, are given. For a simple inverter circuit 64% benefit in delay over a silicon nanowire based technology is predicted. The transient behavior during the reconfiguration event, basic performance considerations and steps towards a full standard cell library have been discussed. Overall, the new model will help to stimulate circuit design and application development for emerging reconfigurable devices.

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