Planned Collaborative Research Center 912

HAEC – Highly Adaptive Energy-Efficient Computing

Technische Universität Dresden

Funding Proposal
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Collaborative Research Center 912

"HAEC — Highly Adaptive Energy-Efficient Computing"

for 2011/2 – 2012 – 2013 – 2014 – 2015/1

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1.1 Key data

1.1.1 Bodies of the Collaborative Research Center

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The *CRC Board* consists of the speaker and two representative speakers, which will act for HAEC groups A and B, respectively. *Members* of the CRC are per definition all principal investigators stated in Section 1.1.2 and two representatives of the group of young researchers within HAEC. Additional members can join the CRC according to the Bylaws, see Chapter 4. All researchers working in CRC form together the *General Assembly*. In order to support research program evaluation and to strategically advise the CRC, representatives from industry and academia will be attained as *Strategic Advisors*.

1.1.2 Principal investigators

Principal investigators	Year of birth	Year of PhD obtained	Institution (location: Dresden for all PIs)	Project
Aßmann, Uwe, Prof. Dr. rer. nat. habil.	1963	1995	Institute for Software- and Multimedia-Technology, Chair for Software Engineering	B01
Baader, Franz, Prof. Dr.-Ing.	1959	1989	Institute for Theoretical Computer Science, Chair for Automata Theory	B02
Baier, Christel, Prof. Dr. rer. nat.	1965	1994	Institute for Theoretical Computer Science, Chair for Algebraic and Logical Foundations of Computer Science	B03
Dargie, Waltenegus, Dr.-Ing. habil.	1969	2006	Institute for System Architecture, Chair for Computer Networks	B06
Ellinger, Frank, Prof. Dr. sc. techn. habil.	1972	2001	Institute of Circuits and Systems, Chair for Circuit Design and Network Theory	A01, A07
Fettweis, Gerhard, Prof. Dr.-Ing.	1962	1990	Communications Laboratory, Vodafone Chair for Mobile Communications Systems	A02, Z01
Fischer, Andreas, Prof. Dr. rer. nat. habil.	1959	1987	Institute of Numerical Mathematics, Chair for Numerical Optimization	A02
Franz, Elke, Dr.-Ing.	1971	2002	Institute for System Architecture, Chair for Privacy and Security	A08
Härtig, Hermann, Prof. Dr. rer. nat.	1953	1984	Institute for System Architecture, Chair for Operating Systems	B04
Jorswieck, Eduard Axel, Prof. Dr.-Ing.	1975	2004	Communications Laboratory, Chair for Communications Theory	A03, A08
Lehner, Wolfgang, Prof. Dr.-Ing.	1969	1998	Institute for System Architecture, Database Technology Group	B05
Müller, Matthias Stefan, Dr. rer. nat.	1969	2001	Center for Information Services and High Performance Computing (ZIH)	A04
Nagel, Wolfgang Erwin, Prof. Dr. rer. nat.	1959	1993	Institute for Computer Engineering, Chair for Computer Architecture	A04
Plettemeier, Dirk, Dr.-Ing.	1962	2002	Communications Laboratory, Chair for Radio Frequency Technology and Photonics	A05
Schill, Alexander, Prof. Dr. rer. nat. habil. Dr. h. c.	1964	1989	Institute for System Architecture, Chair for Computer Networks	B06
Schröter, Michael, Prof. Dr.-Ing. habil.	1957	1988	Institute of Circuits and Systems, Chair for Electron Devices and Integrated Circuits	A06
Wolter, Klaus-Jürgen, Prof. Dr.-Ing. habil.	1949	1983	Electronics Packaging Laboratory, Professor for Process Technology for Electronics	A07

Table 1.1: Principal investigators of the CRC.

1.1.3 Participating institutions

All participating departments of the CRC belong to TU Dresden.

Department of Electrical Engineering and Information Technology

- Institute of Circuits and Systems
- Communications Laboratory
- Electronics Packaging Laboratory

Department of Computer Science

- Institute for Computer Engineering
- Institute for System Architecture
- Institute for Software- and Multimedia-Technology
- Institute for Theoretical Computer Science

Department of Natural Sciences, Mathematics Section

- Institute of Numerical Mathematics

Center for Information Services and High Performance Computing (ZIH)

1.1.4 Projects and project groups

Project groups

A) Energy-adaptive high-speed computing platform
B) Energy-adaptive computing management
Z) Central group

Projects

Project	Title	Research area	Principal investigators, institutes
A01	Millimeter-Wave Integrated Circuits for Ultra High-Speed Wireless Board-to-Board Computer Communication	Circuit Design and Network Theory	Prof. Ellinger, Institute of Circuits and Systems
A02	Ultra High-Speed Wireless Board-to-Board Communication	Mobile Communications Systems / Numerical Optimization	Prof. Fettweis, Communications Laboratory / Prof. Fischer, Institute of Numerical Mathematics
A03	Network Coding for Wireless and Wired Onboard and Backplane Communication	Communications Theory	Prof. Jorswieck, Communications Laboratory
A04	Analysis of Applications on a High Performance–Low Energy Computer	Computer Architecture	Prof. Nagel, Institute for Computer Engineering / Dr. Müller, Center for Information Services and High Performance Computing (ZIH)
A05	Antennas and Wave Propagation for Adaptive Wireless Backplane Communication	Radio Frequency Technology	Dr. Plettemeier, Communications Laboratory
A06	Process Technology Evaluation for Energy-Efficient System Design	Electronic Devices and Integrated Circuits	Prof. Schröter, Institute of Circuits and Systems
A07	Energy-Adaptive Optical Onboard Links for Inter-Chip Communication	Circuit Design and Network Theory / Electronics Packaging	Prof. Ellinger, Institute of Circuits and Systems / Prof. Wolter, Electronics Packaging Laboratory
A08	Secure Network Coding for Board-to-Board Communication	Communications Theory / Privacy and Data Security	Prof. Jorswieck, Communications Laboratory / Dr. Franz, Institute for System Architecture
B01	Energy-Aware Software Architecture	Software- and Multimedia-Technology	Prof. Aßmann, Institute for Software- and Multimedia-Technology
B02	Semantic Technology for Context Awareness	Logic in Computer Science, Knowledge Representation, Automated Deduction	Prof. Baader, Institute for Theoretical Computer Science
B03	Formal Methods for Quantitative Analysis and Optimization of Energy Models	Algebraic and Logical Foundations of Computer Science	Prof. Baier, Institute for Theoretical Computer Science
B04	Energy-Aware Resource Management	Operating Systems	Prof. Härtig, Institute for System Architecture
B05	Energy-Aware Stream and Configuration Management	Database Technology	Prof. Lehner, Institute for System Architecture
B06	Energy-Aware Service Execution	Computer Networks	Prof. Schill / Dr. Dargie, Institute for System Architectur
Z01	Central Tasks	Mobile Communications Systems	Prof. Fettweis, Communications Laboratory

Table 1.2: Projects of the CRC.

1.2 Scientific outline of the Collaborative Research Center

1.2.1 Summary

The energy consumption and ecological impact of main Internet components as data centers and the communications infrastructure are reaching alarming levels. In 2007 already the electric energy production for operating ICT (information and communications technologies) caused a CO_2 output reaching 25% of the level of world-wide automobiles. Current projections show that the growth in energy consumption of Internet components will be passing the levels of the last 15 years, which has been doubling every 5 years.

The visionary goal of the Collaborative Research Center HAEC (highly adaptive energy-efficient computing) is to research technologies to enable computing systems with high energy efficiency without compromising on high performance.

Certainly a straightforward way for improving energy efficiency is to reduce the energy consumption of every individual hardware component involved. However, more important is to understand how the software system can be adapted to the hardware and vice versa. Today, computational problems are written in software without any opportunity for being written to generate energy-aware code, and then the code is mapped onto generic hardware configurations of parallel machines. As the computational problems that are being executed require a certain amount of computational execution with complex and problem-specific intercommunication between the computations, a highly adaptive hardware system, which can optimize its configuration according to the needs of a software system could generate a much higher level of efficiency.

In addition, system states of the application and hardware system need to be monitored and taken into account during run-time as well. As a simple example, consider an e-reader, e.g. iPad, with a limited energy source, which should run a standard service: a high-definition video streamed onto the device over a wireless interface, e.g. WLAN. To generate a desired user experience (utility) a careful trade-off needs to be made between spending the energy on the lighting of the display, the processing of the video decompression, the video resolution and the wireless bandwidth (data rate) required. Hence, at the service and application levels new ways of controlling energy utilization must be found to carefully balance the need versus the gain. It must be made clear that this simple example of a handheld device was chosen here only to show the principle of the research problem, whereas HAEC will concentrate on researching larger server systems, from applications to hardware.

To achieve the goal of an integrated approach of highly adaptive energy-efficient computing (HAEC), the problem is approached at all levels of technology involved, the hardware, the computer architecture and operating system, the software modeling as well as the application modeling and runtime control levels. A novel concept, namely the HAEC Box, of how computers can be built by utilizing innovative ideas of optical and wireless chip-to-chip communication shall be explored. This would allow a new level of run-time adaptivity of future computers, creating a platform for flexibly adapting to the needs of the computing problem. A design time and a run-time real-time control loop will be researched, which shall be controlling the energy trade-off based on the current hardware state as well as the context-aware application requirement, taking the required utility into account. The HAEC Collaborative Research Center is a first attempt to achieve high adaptivity and energy efficiency with an integrated approach going through all levels of abstraction, from hardware components all the way to the application software. The technology being explored has the potential for HAEC to take on leadership in the scientific community on how to design future computing systems, and also, as it matures, to become a pace setter and have impact in the industry.

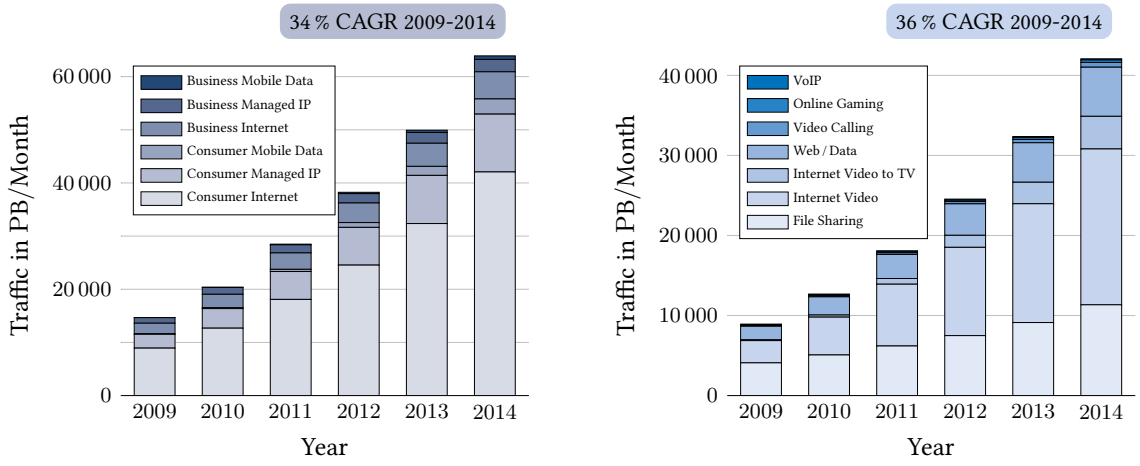
1.2.2 Research program

Motivation and goals

Dear reader – when does your bad conscience turn worse with respect to energy consumption and carbon dioxide pollution – if you are traveling by aircraft or if you browse through the Internet?

It may be surprising, however, the fact is that since 2007, the energy consumption and corresponding carbon dioxide pollution of the data servers and networks required for global Internet is higher than that of the world-wide air traffic [Heu07]. The research vision addressed by HAEC is to enable high-performance computing with high energy efficiency. To enable this vision, HAEC addresses with its research program key hardware, software and system challenges by creating technology for novel computing architectures and energy-adaptive distributed software. Projects must contribute to one of the criteria *design*, *monitoring*, *analyzing*, *improving/optimizing* and *controlling* within an overall process cycle to create high-performance low-power computing, or develop a clear vision on how to contribute to the central demonstrator in year 12 (the HAEC Box).

Considering the strong increase of the required data rates and number of users, this research vision will become even more significant in the future. Today, global Internet and web applications, such as upload and download of video content (video streaming), exchange of large files and Web 2.0 applications, require enormous computing and networking resources. As illustrated in Figure 1.1, the total amount of Internet traffic is estimated to grow about 34% per year until 2014 to more than a total of 63 Exabytes[1] (EB) per month. Among these, different types of video on demand (Internet-based high definition television, Internet video and peer-to-peer video) will account for approximately 50% of total IP traffic in 2011.



(a) Global IP traffic by segment

(b) Traffic by type for segment *Consumer Internet*

Figure 1.1: Cisco's global IP traffic forecast 2010 [Cis10].

This massive growth of Internet traffic heavily correlates with a growth in total energy consumption, both in the network as well as at the edge of the network. More network links and intermediate content distribution servers are needed to keep up with the Internet traffic growth caused by video on demand and other Internet and web applications. While these applications offer new means of individual entertainment, collaboration and interactivity, they increase the total energy consumption in the same way. Server farms will grow, consuming energy for operation and cooling. This means

[1] 1 Exabyte = 10^{18} Bytes.

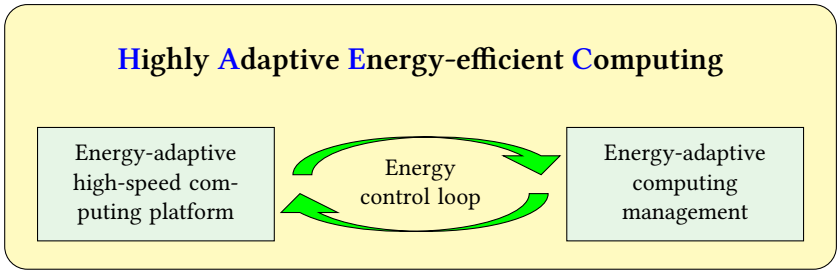


Figure 1.2: Overview of HAEC.

that energy efficiency is not only an important goal but an absolute necessity at all levels, particularly within network and content servers. Many other high-end computing scenarios yield similar characteristics and requirements.

While energy efficiency has already been considered at certain levels of the above mentioned scenario, such as energy-aware optimization of routing algorithms, what is needed is a comprehensive approach that takes the overall applications' demand and users' context as well as the particular aspects of computing resources (software and hardware) into account. At the moment, optimizations are considered on a component level, mostly in isolation, and do not take the demands of applications, user communities and contexts into account in an integrated holistic manner.

The goal and approach of the CRC is to do exactly that. We plan to address energy efficiency at all system levels, ranging from lowest levels of interconnection technologies to highest levels of software engineering approaches. The guiding principles are simple and uniform:

1. Ensure flexibility at all levels that allows to provide alternatives tailored to applications and situations.
2. Establish – mostly offline – the added value (utility) of spending energy in one or the other alternative.
3. Monitor current energy levels and other activities.
4. Take action at run time based on the monitoring results and the available alternatives.

The development of concepts for a computer system based on a holistic approach of energy adaptivity can only be achieved by considering hard- and software aspects together with their inter-relations. HAEC will perform basic research enabling highly adaptive energy-efficient computing, incorporating an energy-adaptive software architecture based on a high-performance energy-adaptive computing architecture. The goal is to provide solutions for scalable, energy-adaptive computing and content distribution for the next decades.

The CRC is split in two research groups, cf. Figure 1.2, HAEC-A being responsible for the hardware technological activities, while HAEC-B is in charge of the software activities. Both groups are highly interdependent. We know of no other undertaking of comparable comprehensiveness.

The goal of HAEC-A is to provide low-energy and highly-adaptive interconnection technology. Here, we assume that low-energy components will be contributed by industry and other closely related, complementary projects, such as CoolSilicon. The interconnection technology will allow to set up a communication structure closely following the communication demands of the software structures. It will also provide knowledge on the energy consumption of communication alternatives, beforehand by analysis and at runtime by monitoring techniques.

The goal of HAEC-B is to provide a comprehensive software structure to make use of the versatile HAEC-A structure. It employs the four guiding principles mentioned above at all software levels, ranging from low-level resource monitoring and scheduling via software engineering techniques to cluster-level network management.

A more detailed summary of HAEC-A and HAEC-B activities is given below. The innovations mentioned there can be found in Table 1.3.

Project group A: Energy-adaptive high-speed computing platform (HAEC-A)

At the hardware level, high-speed energy-adaptive computing demands a radically new hardware connectivity architecture for computers and their components (Innovation I-A). This architecture will complement current wired connections for high-speed applications. Today's copper-based connections have reached their fundamental physical limitations. It is expected that they will no longer be able to transmit the increasing data rates demanded between integrated circuits in typical high-performance cluster servers [YML+10].

In order to enable the targeted breakthrough in the area of computer connectivity, an aggregated band-width in Tbit/s regime must be achieved by improving the data rate per link and simultaneously the channel density for parallel links, while, overall, the specific power consumption per transferred data volume needs to be minimized. To meet this goal we propose to employ wireless beamsteered links for board-to-board and onboard optical links for chip-to-chip communication. This hybrid link technology will be employed for enabling a novel server architecture, the *fat tree with hyper connections*, which we refer to as *hyper-fat tree*, Figure 1.3. It has the potential to provide an excellent hardware infrastructure for energy-adaptive software and networks.

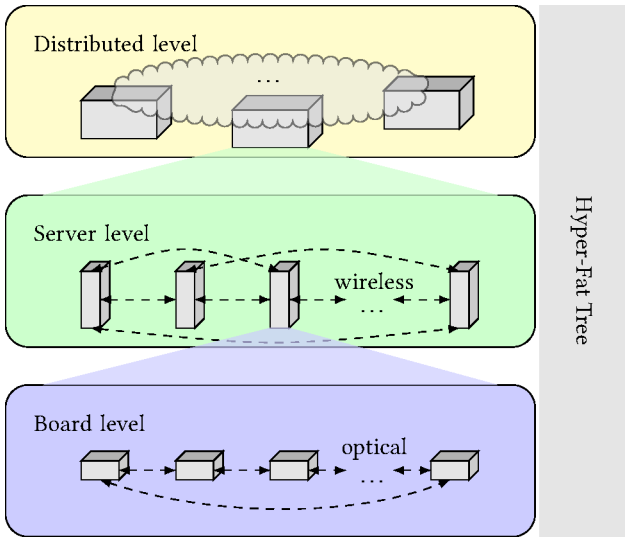


Figure 1.3: Hyper-fat tree architecture.

The spectral efficiency of the onboard and board-to-board communication is increased by clever routing and network coding design (Innovation I-A.10), which achieves the maximum multicast network flow. Considering security aspects of the network coding schemes is of essential importance for ensuring both confidentiality and integrity of the data to be transmitted even in the case of intended attacks. Introducing security mechanisms often increases the costs in terms of additional operations to be performed or additional data to be sent and, hence, influences the energy efficiency. One goal within the project is, therefore, to analyze the security of existing network coding schemes and investigate possible improvements of their security considering energy constraints (Innovation I-A.11). We refer to this novel computing architecture approach as the *HAEC Box*. The energy efficiency is increased by providing direct links reducing the amount of switches between nodes, as well as by

realizing the capability to adapt dynamically to the required data rates: hardware will be turned off when not needed or operated at lower power when lower data rates are sufficient.

The hyper-fat tree approximates one important feature of a scalable crossbar switch, the direct memory access with 0-copy chains. This ideal crossbar switch cannot be realized, but the hyper-fat tree architecture of the HAEC Box approximates it by realizing integrated memory access of logarithmic depth in the size of the tree (Innovation I-A.12).

With respect to the platform, one important innovation of the HAEC program consists in the multidisciplinary approach to the scientific and technical challenges of the two critical interconnect bottlenecks of the hyper-fat tree architecture: the board-to-board and the chip-to-chip onboard communication. We propose to rely on sub-THz wireless links for board-to-board and optical links for onboard communication, as shown in Figure 1.4.

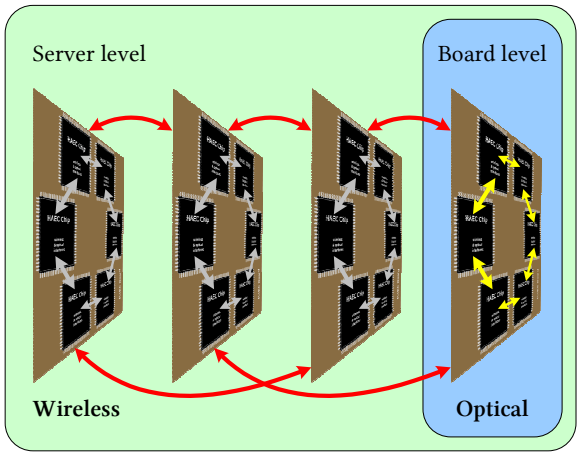


Figure 1.4: Simplified schematics of novel network topology for server farms combining the advantages of short-range wireless and E/O waveguide data communication enabling hyper and ring connections at relevant nodes.

Wireless communication between computer boards. As a significant novelty, we employ wireless communication techniques for data connection between the computer boards (Innovation I-A.5). Since no wires are required, wireless communication allows significantly lower routing complexity. Hence, novel and significantly more complex network architectures are possible. At the speed required for board nodes, conventional network architectures can be easily extended, e.g. with connections within the horizontal plane (Innovation I-A.3). These ring-extended trees, which can be further extended towards hyper-fat trees, significantly reduce the latency and increase the throughput on the boards, since the data does not have to pass the previous parent nodes typically acting as bottleneck. Conventional wireless systems operating in the lower GHz range are not sufficient to deliver the data rates required in HAEC systems: we will therefore exploit the frequency range from 100 GHz to 300 GHz. Within this frequency range, bandwidths and data rates above 25 GHz and 50 Gbit/s, respectively, are expected to be feasible under line of sight conditions up to 30 cm. Our plan is to research polarization multiplexing to enable data rates up to 100 Gbit/s per link, or data rates not realized to this date. Wavelengths in the millimeter and sub-millimeter range allow the realization of very compact high-gain antenna structures on several board nodes. Using modern beamforming and -steering techniques, different network topologies, including adaptive channel allocation, are applicable. This wideband wireless communication concept provides extremely flexible, robust and weight optimized data links between computer boards.

However, the challenges regarding digital modulation schemes, algorithms, circuits, antennas, interconnections, packaging, semiconductor technologies, modeling and electromagnetic interactions/ shieldings are significant. Transistors with transit frequencies of around 0.5 THz are required. In this context, we will consider leading-edge SiGe HBT (BiCMOS) technologies, aggressively scaled CMOS, e.g. 28 nm or below, and – in the long term – emerging technologies, such as nanotube and nanowire FETs. Studies will be performed to evaluate the suitability of advanced semiconductor technologies, device models and implementation of the electronic interfaces to improve the system-efficient integration and to reduce the link dimensions. Achieving speeds up to sub-Tbit/s per series link is very challenging since it requires the electronic circuitry to operate at frequencies close to the cut-off of most advanced silicon technologies. In this context, we plan to consider novel circuit topologies, suitable to extend the maximal frequency of operation, and circuit models accurate also in the breakdown regime, as well as on comparing different process technologies with respect to their performance and feasibility. This will include the exploration of ultimate technology limitations via computer models (Innovation I-A.8) and experimental characterization.

The architecture of the wireless system will impact critically the energy efficiency. Thus system-level decisions will be made across projects with the primary goal of achieving the required performance at the minimum power consumption. For example, it is planned to implement the beamsteering of each phased array in the analog domain, by controlling amplitude and phase at each antenna element with compact mm-wave components. This approach will enable energy efficiency improvements through a reduction in the number of integrated active blocks, as only one ADC per phased array is needed. The digital processing blocks will still have full control of the beam direction, while only a few dB of receiver sensitivity and transmit power will be sacrificed. This drawback is – however – acceptable, given the intrinsic short-range nature of board-to-board communication.

Optical inter-chip onboard communication. It is already widely accepted that onboard optical communication will displace electrical interconnects for very high data rates – only the when and how remained open. The *hybrid* HAEC approach now combines the flexibility of the wireless for board-to-board communication with the surpassing performance and bandwidth density of optical chip-to-board communication in order to simultaneously overcome both major intra-rack system bottlenecks. Moreover, in this interplay the optical onboard communication will work interference-free and allows for conversion-free system-spanning rack-to-rack interconnects, where optical yet has replaced electrical interconnects. In consequence, the traditional backplane could furthermore only exist for mechanical electrical power means and comparable low data rate control signalling.

Compared to competing approaches for optical onboard communication a major innovation within HAEC is the *energy adaptivity* (Innovation I-A.4). The newly designed transceivers can adjust their link parameters (e.g. trading data rate off for power consumption) with respect to the actual load condition and energy requirements. Existing integrated circuits (ICs) are either statically trimmed for highest performance or lowest energy consumption and do not provide such energy adaptivity. In HAEC, the dynamic link requirements will be determined by the energy control loops of the computing management as the focus of HAEC-B. As a consequence, a part of the parallel links can be switched off to save power, and the remaining active links can be optimized for lowest possible power. Due to the lower link bandwidth requirements at lower data rates, the circuit bandwidths, the clock frequencies, and hence the corresponding supply current (partly also the supply voltage) can be reduced for a link path. Besides the dynamic speed adaptivity also the advanced modulation schemes will be researched and assessed for power optimization to enable a certain data rate at different modulation schemes and symbol rates. The challenge is to find the optimal trade-off between number of active links, bandwidth per link and complexity of the data format and to quickly switch between these op-

tima as to the requirements. In later program phases, in addition to BiCMOS and CMOS technologies, the suitability of emerging technologies, such as nanotubes and nanowires will be investigated.

Since up to now there is no light-source capable for silicon integration, *novel packaging and assembly technologies* (Innovation I-A.9) are needed to build up hybrid silicon/SiGe/III-V transceivers with high-speed 3D stacking. Even though these lasers (VCSELs) can improve the bandwidth density by a higher per-link data rate over the electrical counter parts still massive parallelization is needed. Hence, these optical I/Os will be arranged in arrays. As a consequence, arrayed driver electronics have to be designed and then stacked for better high-speed performance than the already demonstrated lateral or even peripheral integration concepts. Only the close collaboration in the form of a joint project between packaging and chip design can guarantee the optimum system performance because assembling techniques can significantly affect the circuits' behaviour. Prospectively SiGe-compatible on-chip light-sources from the joint lab with the Leibniz institute IHP (Innovations for High Performance Microelectronics) can reduce this packaging complexity. Nevertheless, the challenge of the robust optical E/O device-to-waveguide coupling remains and is further complicated by the arrayed arrangement of the optical I/Os underneath the chip. The development of this complete electro-optical subassembly is also addressed within Innovation I-A.9. It will comprise of a coupling micro-optic that can redirect the light by 90 degree from the E/O socket on the board surface into the embedded waveguides. To allow further bandwidth density improvements the optical I/O pitches will be downscaled. Therefore, the micro-optics to be newly developed must provide an optical pitch conversion capability (fan-out) in order to passively couple the light into electro-optical circuit boards with relaxed accuracy requirements and low loss.

Due to the arrayed optical I/Os the board-level-waveguides will have to be a multi-layer structure to reroute the dense parallel optical bus. Packaging technologies will be developed for the patterning, stacking and integration of multi-layer optical PCBs for high reliability despite their compliance with PCB typical misalignments. Only this way repairing in the field will be enabled by using a low-cost substrate, which can achieve competitive solutions compared to current electrical solutions. The new technologies will drive the implementation of silicon photonics with their associated waveguide requirements for the later phases of the HAEC program.

HAEC Box simulator. A central part of this CRC is the analysis of the new means of wireless and optical chip-to-chip communication from the view of the computing system using them. With the holistic approach of this CRC, it is adequate to define energy efficiency as the amount of energy the HAEC Box needs to finish a specific task set.

An event-based simulator will be developed to emulate the interactions between the HAEC hard- and software models (Innovation I-A.13). The event trace-based simulator will be designed to emulate runs of energy-aware software on the HAEC operation system using the HAEC communication system providing sensor data for the HAEC monitoring system. For this, the HAEC Box simulator has to combine models of different abstraction levels (for energy consumption of components, communication, operation system, energy-aware software and monitoring). This combination is of central significance since, per design, HAEC hard- and software will be tightly coupled by energy/utility functions and energy control loops, see below.

The connected models include detailed information on energy consumption for all their relevant processes and system states. With this, the simulator becomes an environment to verify the HAEC design ideas and to analyze their impact on the energy efficiency at large. The systematic analysis of simulation runs will allow the specification of design requirements and optimizations for the hard- and software development.

Project group B: Energy-adaptive computing management (HAEC-B)

HAEC-B will contribute the software to make use of the adaptive hardware architecture of the HAEC Box for highly energy-efficient systems. To achieve this goal, few fundamental principles are used in an integrated holistic manner. At the core are *energy control loops*, which we call *HAEC Loops* in the following, and *energy/utility functions*.

Analogous to traditional control technology, the system state of controlled objects in the HAEC Loops are continuously monitored and controlled, cf. Figure 1.5. Controlled objects in the HAEC Loops are the physical and logical resources provided by HAEC hardware and software. HAEC control actions select, activate and deactivate such physical and logical resources. Information about these resources is collected by HAEC monitoring techniques. HAEC algorithms implement the control law and optimize the usage of energy based on an analysis of monitoring results. For example, DVFS (dynamic voltage and frequency scaling of CPUs) could be called a HAEC Loop.

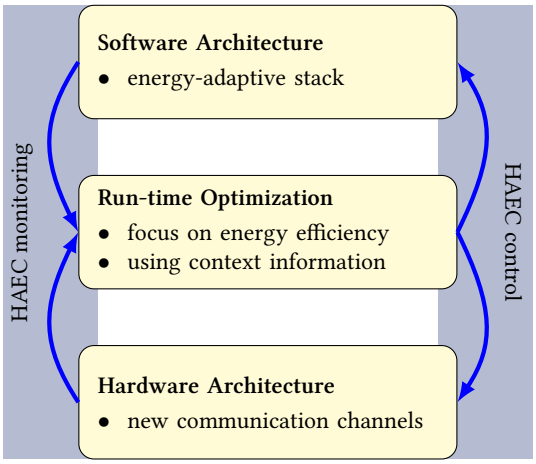


Figure 1.5: Energy optimization means energy and context awareness, as well as energy adaptivity under the global strategy of energy optimization. This spans up a dual control loop comprising hard- and software architectures.

Optimizing the usage of energy comes in several strategies. One is to maximize the *utility* to be achieved if a given fixed amount of energy is available. Utility can be defined as, e.g. the number of transactions per second in a database system or a web service, the execution time of an application in high-performance computing or the quality of service in a multimedia application. Another strategy is to minimize the energy required to obtain a given fixed utility. Many more strategies result from a combination and variation of these two. For example, one other strategy is to minimize the average energy requirement that suffices to enable a system to achieve a predefined, seldom required peak performance within very short time.

For control actions to be useful for energy savings, HAEC hardware and software must provide highly flexible choices between alternatives of differing energy characteristics. While HAEC-A takes care of such flexibility in hardware especially in the communication structure, HAEC-B must provide such flexibility in software. A common approach to software flexibility is to provide several implementations of one specification. In general, many such techniques have been developed in the disciplines of systems software, compiler construction and software engineering. But only a few of them address alternatives with differing energy characteristics (Innovation I-B.5). Examples of such general techniques are hotspot detection and tuning, usage of fundamentally different algorithms and so-calledspecialization. Once these techniques are combined with HAEC Loops, they allow a charac-

terization by means of currently popular terminology, such as self-adaptive software, autotuning and so forth. In analogy to hardware resources, we sometimes refer to functionality provided by software as *logical resources*. For example, sorting is a logical resource with several alternative implementations of different characteristics. One of the major challenges for HAEC-B will be to invent and evaluate mutually alternative logical resources and their energy characteristics.

The major challenge for monitoring of resources to be useful is the consideration of trade-offs between size, freshness, accuracy and overhead induced. Since at the current state of technology energy measurements are not available directly, techniques must be used to deduce the energy usage from other state variables (Innovation I-B.4). Monitoring is also needed for system characteristics other than energy, since such characteristics can become constraints for energy optimization. For example, monitoring of CPU load is needed since a fully loaded CPU may become a constraint for the selection of a logical resource requiring many CPU cycles. These challenges are addressed in multiple projects of HAEC-B, cf. Figure 1.6.

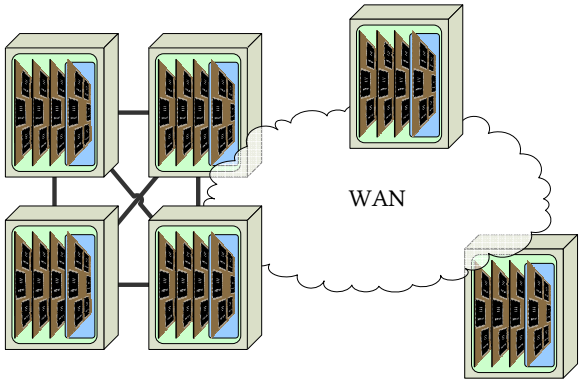


Figure 1.6: Energy optimization must be integrated in software and hardware architecture. Monitoring and controlling will be performed on all components of the system.

While the terminology of control technology served well so far for explaining the fundamental approach of HAEC-B, its usage for more technically detailed descriptions becomes cumbersome and non-typical, especially if several components of HAEC Loops are tightly intertwined. In such cases we use common terminology from informatics. For example, in resource monitoring the pre-processing of raw measurement data and supervision are often tightly integrated (Innovation I-B.2). Resource managers (for example CPU schedulers or disk drivers) are special, highly integrated control loops (although in general not with energy in mind).

Control algorithms to optimize the usage of energy require knowledge of the energy characteristics of physical and logical resources. In contrast to classical scheduling, the well-studied discipline of planning and managing resources, energy-aware scheduling adds an additional indirection: while in classical scheduling all resources are assumed to be just there, resources in energy-aware scheduling become available only if energy is spent to activate the resources. To cope with this challenge, HAEC-B will develop and use *energy/utility functions* as the second fundamental principle (Innovation I-B.3). Energy/utility functions characterize the utility of energy for some application, if used for a particular physical or logical resource in a specific context. Application and utility are used here in a fairly general sense.

As an example: for the application “transport data from source to destination within a certain time” the energy needed for compression (CPU cycles) and a slow network may be lower than the energy needed for a fast network without compression. Then the utility of using the energy for CPU and the slow network is higher than that of using the energy for the fast network. On a higher level, the

utility of energy used for compression and slow network or even for a fast network may be low, if the consumer does not need the delivery in such short time.

As there are many classical schedulers in computer systems, there will be many HAEC Loops in the HAEC Box. Examples range from low-level CPU schedulers up to the rearrangement of server farms. The HAEC Loops will be able to achieve local optima, but there are cases where cross-layer control is required. For example, if a part of a server farm is shut down, all lower-level HAEC Loops must follow suit accordingly. For these cases we envision a data plane that can be accessed (read from and written to) by HAEC Loops at all layers (Innovation I-B.1).

The evaluation will be based on very simple examples, such as a versatile, adaptive video decoder, and parallel skeletons, such as map/reduce algorithms. An important challenge for HAEC-B will be that the HAEC hardware is not available at the start of project and therefore must be simulated. The simulator will be provided by HAEC-A.

Contributions of the involved PIs

The fundamental principles as explained above may sound simple and straightforward. Having reduced the vast number of approaches and publications on energy-aware systems to these few principles can be considered as a first result of the cooperation of researchers in fairly diverse disciplines. Full understanding and application on these principles will be challenging and high-risk research. For example, collecting the data for energy/utility functions and finding a versatile representation that is still usable and tractable in diverse HAEC Loops is expected to be difficult and, to the best of our knowledge, has never been attempted before. As another example, having multiple schedulers for diverse resources that cooperate in achieving a common goal – not considering energy at all – has been tried a few times in the real-time disciplines field, but is still considered a research challenge. In addition, the highly adaptive optical and wireless chip-to-chip communication links, required for an efficient mapping of the specific computational tasks of the energy-aware software system onto the hardware, involve challenges within several disciplines, ranging from device modeling to information theory. HAEC will have to conduct novel and groundbreaking fundamental research in these and many more areas, which are summarized below and detailed in the individual project descriptions in Chapter 3. In addition, we know of no previous attempt to research and use these principles in a comparable integrated and holistic way.

This is exactly the goal of HAEC. To this end, a unique ensemble of PIs and expertise has been assembled. In the following we name the particular expertise of the PIs with respect to HAEC.

Prof. Ellinger (A01, A07). He has more than ten years of experience in modeling, design and characterization of circuits operating at frequencies from 1 GHz to 110 GHz in CMOS, SiGe BiCMOS and GaAs MESFET technologies. Corresponding applications involve wireless communication, optical communication, radar for positioning and adaptive antenna combining. Within the frame of the HAEC program, his research group will lead the analog IC design efforts with focus on high-speed and low-power operation.

Prof. Fettweis (A02, Z01). He has extensive experience in physical layer research, with a special emphasis on wireless radio network problems (wireless networks capacity), multi-antenna wireless modems (baseband algorithms) including RF impairments ("Dirty RF") also in particular for 60 GHz and IC implementation architectures. Together with his team he will investigate, design and optimize the physical layer for energy-efficient wireless board-to-board communication in the frequency range from 100 GHz to 300 GHz. The focus is on modulation schemes, baseband algorithms and low-latency

error correction schemes for single and multiple-link scenarios. This under the special HAEC channel characteristics, including limitations from the analog hardware and from the data converters.

Prof. Fischer (A02). He has a broad experience in the field of numerical optimization, in particular with regard to applications, modeling and to the design and analysis of algorithms. Together with his team he will model, investigate and solve optimization problems that arise from the design and control of the onboard wireless antennas with special emphasis on energy efficiency and performance and subject to limitations from the transmit channel, specific hardware and fabrication tolerances. Prof. Fischer and Prof. Fettweis have a proven track record of working jointly on optimization of wireless multi-antenna systems.

Dr. Franz (A08). She has experience in the field of data security and privacy. Her main research interests are steganography and privacy-aware application design. Experiences with establishing attacker models and applying security mechanisms for enforcing protection goals will be used for analyzing the security of the network coding schemes suggested for communication within the HAEC Box and for investigating possibilities for improving the security of these schemes.

Prof. Jorswieck (A03, A08). He is the head of the Chair for Communications Theory of TU Dresden. His main research interests are in the area of signal processing for communications and networks, applied information theory and communications theory. The group has experience in the computation of fundamental limits of single- and multi-user systems in various wireless and wired scenarios, in transmit and receive optimization for communication systems as well as coding and decoding for noisy and fading channels. Recently, the group started to investigate network coding on the physical layer for improving the efficiency of networks. The group will study the analysis, design and optimization of network codes for energy-efficient communication in the HAEC Box. Additionally, security issues of network coding will be addressed.

Dr. Müller (A04). He has extensive experience in programming methodologies of parallel systems as well as performance monitoring, analysis and optimization of parallel applications. He has led the development of several internationally recognized benchmarks and tools in this area. He and his team will use the developed high-precision measurement environment to analyze and model the energy consumption of single components running synthetic and application benchmarks. These models are an essential part of the HAEC Box simulator and of the energy/utility function.

Prof. Nagel (A04). He has extensive experience in performance analysis of computer architectures, communication systems and especially applications on high-performance systems (HPC) systems, which has required to develop innovative event tracing tools. With the HAEC Box simulator as a specially designed tool, models of different abstraction levels (communication, system, software) will be linked. The analysis of run-time scenarios on the simulator can then provide valuable feedback for the hard- and software design of the HAEC Box.

Dr. Plettemeier (A05). He has extensive experience in antenna design and computation of high frequency electromagnetic fields, centered on space exploration (spaceborne antenna systems and inverse scattering problems), wireless communications (compact integrated antennas and arrays, MIMO), electromagnetic compatibility (radiation coupling, hybrid computation methods) and radio over fiber systems (high data rate transmission). Current research topics focus on in-package solutions of adaptively steerable mm-wave antenna arrays and compact array solutions for satellite communications. The

role of Dr. Plettemeier and his team within HAEC is the design and optimization of reconfigurable in-package and on-chip antenna arrays in the frequency range from 100 GHz to 300 GHz. Main topics are single element and array design, optimization of beamforming and steering performance, interconnection scheme, polarization multiplex and link performance.

Prof. Schröter (A06). He has extensive expertise in compact and numerical device modeling, associated CAD tools, experimental characterization and semiconductor process technology. He and his research group will leverage this expertise for (i) performing an analysis of competitive process technologies for implementing energy-efficient high-frequency circuit blocks and (ii) developing methodologies for automated optimization of circuit blocks. These investigations will be based on advanced compact models and modeling tools.

Prof. Wolter (A07). He has extensive experience in the field of electronics and opto-electronics packaging involving such project-relevant topics as: integration of optical interconnects in electrical printed circuit boards, design and development of coupling optics for array opto-electronic devices, assembly technologies for fine pitch interconnects, e.g. flip-chip technology and 3D-integration of integrated circuits. He and his team will use this experience to design and develop an onboard optical interconnect for energy-adaptive inter-chip communication.

Prof. Aßmann (B01). He has extensive experience in model-driven software development (MDSD), component-based software engineering (CBSE), software integration methods, such as aspect-oriented programming or invasive software composition and self-adaptive workflow systems. He and his team will research a new technology for highly energy-adaptive software architectures based on MDSD and the autotuning of software architectures. These adaptable application software architectures can be used by control actions in HAEC Loops.

Prof. Baader (B02). He has extensive experience in designing logic-based ontology languages that are tailored towards the needs of specific classes of applications. He and his team will use this experience to design ontology languages and corresponding inference procedures that can extract high-level context information from low-level sensor/monitoring information. The recognized context can then be used to trigger hardware or software reconfigurations in HAEC.

Prof. Baier (B03). She has extensive experience with probabilistic model checking. She and her team will work on a compositional framework for modeling and analyzing energy-aware systems. The goal is to enable offline analysis of energy-related properties.

Dr. Dargie (B06). He has extensive experience in applying analytic models to quantify the energy consumption of randomly deployed wireless networks and wireless sensor networks. He has also employed various probabilistic schemes for context recognition. The models and schemes can be used to quantify the energy consumption of distributed service execution and to implement energy-aware adaptation strategies.

Prof. Härtig (B04). He has extensive experience with classical real-time scheduling of resources including CPU, disk, network and windowing systems. He and his team will lead the investigation of the definition of energy/utility functions and their usage in energy-aware scheduling, starting mostly with physical resources.

Prof. Lehner (B05). He has extensive experiences in data mining and data analysis. He and his team will employ techniques to analyze data streams and to condense them to so-called synopses, very small representations tailored towards the usage in HAEC Loops and the cross-layer data plane.

Prof. Schill (B06). He has extensive experience in middleware and distributed service architectures. He and his team will research the non-local challenges of adaptivity. These include the problems of coordinating independent local energy managers, as well as the opportunities that come with possibilities to migrate platforms in the cloud and to shut down underused ones. Using popular terminology, the project can be characterized as responsible for cloud-level energy management.

The close cooperation and interactions between the CRC partners allow a scientific breakthrough in the design of energy-efficient computing systems. Only with the holistic approach of simultaneous development of hardware and software components at different levels, energy efficiency can be addressed in a systematic way as a whole. At the hardware side, the projects focuses on research at levels from novel communication technologies to chip design to board and server design. At the software side, the research ranges from instruction level to operating system to monitoring up to model checking and energy-aware software technologies. A simulator will be developed to link hard- and software models at different levels of abstraction. This enables the analysis of energy-saving ideas at the system as a whole. The development of the HAEC Box as an energy-efficient server relies heavily on the interaction between research projects, whose interrelations are illustrated in a cooperation diagram on page 28. Overall case studies and demonstrators will further increase the added value of the cooperation throughout all project phases of the CRC.

HAEC demonstrators and case study scenarios

The three project phases of the CRC are illustrated in Figure 1.7. Within Phase I (years 1–4) single technology demonstrators will be built to illustrate and verify the achieved research results. The specification of each of these demonstrators will be based on boundary conditions given by the other demonstrators to which an immediate interfacing is planned. Hence, interactions between demonstrators will be already kept in mind in this early stage to ensure their interoperability later on. At the end of Phase I, the communication parameters will be available for an expert in computer design in order to start building a specification of the HAEC Box. Therefore we intend to create a new processor design chair at TU Dresden in order to approach this challenge from a scientific as well as from an engineering point of view. In Phase II (years 5–8) integrated technology demonstrators by collaboration between several projects are intended. In this period we expect to set up an Integrated Research Training Group (“Graduiertenkolleg”). For Phase III (years 9–12) a comprehensive evaluation is planned, providing an overall picture of the energy reduction that can be gained by the integration of all contributions made by the CRC. The goal is to show a significant power reduction clearly above 50%. Additionally, in this period we will evaluate and decide to set up a DFG Transfer Project to explore the chances for commercialization of the developed technology.

The technologies and methods developed within the CRC will be tested against real-life case studies. One currently planned case study scenario is *energy-adaptive multi-site video conferencing*, as it exposes high power demands yielding great potential to show the benefits of the HAEC design, architecture and the technologies. Moreover, Prof. Schill, as one of the principal investigators of the CRC, has significant experience in distributed service execution in this application domain, which ensures the feasibility of the case study and the availability of real-life data. HAEC will demonstrate for such a video conferencing system that its closed energy control loop will adapt the energy consumption

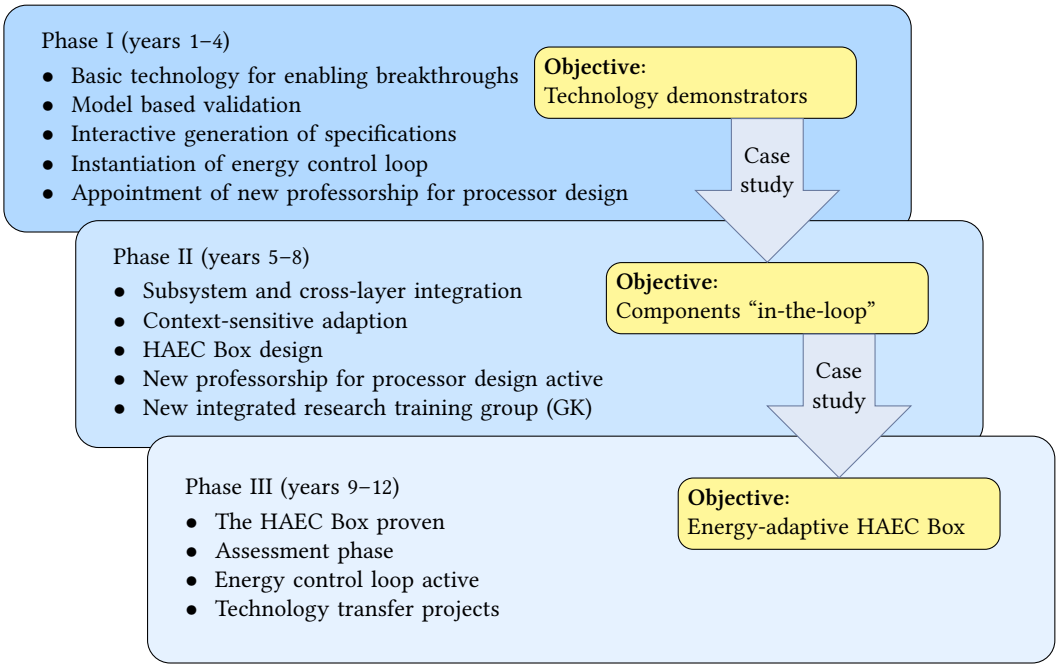


Figure 1.7: The three project phases of HAEC.

to changing user demands, and globally, reduce the energy consumption of the video conferencing system considerably, compared to a non-adaptive setting based on standard servers.

The problems that need to be addressed within this case study are real-time requirements (e.g. maximum latency), high scalability (e.g. with regard to bandwidth requirements, computing power and storage access), synchronization (multi-party audio and video) and transcoding (e.g. to support different stakeholders with different mobile devices). The goal of the case study is to show that these problems, which are shared by most energy-costly distributed applications, are addressed by the CRC. Both the individual contributions of projects within the CRC and the integration of multiple project results will be evaluated in the case study. The problems raised by the mentioned scenario are addressed by both project groups A and B in a complementary fashion.

Project group A (energy-adaptive high-speed computing platform) enables real-time requirements, scalability and synchronization by providing the technologies and architecture to perform the transmission and processing of video and audio data more energy-efficiently. For instance, the individual projects A01, A02, A03, A05, A06 and A07 reduce the power consumption of onboard, board-to-board and backplane communication. Projects A01, A05, A06 and A07 design and evaluate hardware components and projects A02 and A03 develop suitable transmission and network coding techniques for these communication links. These high communication demands are caused by the enormous amount of data that needs to be transferred in the case study scenario. Project A04 analyzes and provides methods to measure the energy efficiency of the video-conferencing system during runtime. To ensure that energy efficiency does not come at the cost of security, the important aspects of security of the HAEC Box concept in general and network coding schemes in detail are addressed in project A08.

Project group B (energy-adaptive computing management) also addresses all requirements in the given scenario. The contributions of this group will more be focused on the application side, complementing the computing platform provided by group A. For example, project B04 will connect the infrastructure developed by group A to higher application levels in terms of operating system extensions that allow to retrieve power consumption data or to allocate resources efficiently. Based on

this, other projects will contribute to the overall optimization. Project B01 enables the adaptation of the application architecture of video-conferencing applications as a whole to adapt to changing contexts, fluctuating system load or user demands. Projects B02 and B06 will provide the technologies to identify and reason about the relevant contexts. The analysis of the video-conferencing system is performed in projects B03 and B05. These analyses enable the optimization as, for example, performed in project B04. Again, the distribution of data, allocation of computing power and its adaptation to changing requirements is fundamental to target energy-costly applications and can exemplarily be evaluated in the video-conferencing scenario. Finally, project B06 provides local and global power-management strategies to reduce the power consumption of distributed servers when idle as well as when operating at peak capacity. The power-management strategies exploit context information to achieve their goal.

Another currently planned case study regarding group B is the web analysis system *Fedseeko* [WHSS10], which has been developed with the aim to create an all-embracing view of particular products of desire using product information from different online information sources (online malls, producers, consumer rating sites, etc.). The system consists of several web services for gathering, filtering, aggregating and integrating such information. These web services use a number of algorithms from different domains, such as information extraction, natural language processing, ontology matching and ontology learning. At present, Fedseeko is neither adaptive nor energy-aware. In the context of the CRC, the idea is to redesign some of the web services such that they can be reconfigured, migrated or dynamically bound-to to demonstrate some the usefulness of the adaptation and energy-aware strategies that will be developed.

Within the first year of the CRC, investigations will be conducted to verify the appropriateness of these case studies or to refine them towards even more representative scenarios.

The research specific to the case studies will be managed and scientifically supported by two Post-Docs assigned to the "Central Tasks" project Z01. They will be responsible for verifying the appropriate-ness of the case studies and for monitoring the progress throughout the CRC. Additionally, they will coordinate the collaboration between individual projects to ensure the execution of the case studies.

Ideas and innovations of HAEC

The main goal of the CRC is to enable integrated hardware/software system solutions for distributed networked applications to be optimized for high adaptivity and energy efficiency during design as well as deployment, without compromising in performance. This comprises the following two major goals:

Major goal A. Energy-adaptive computing platform (HAEC Box), being a major innovation towards low-power computing without compromising performance.

Major goal B. Energy-adaptive computing management, being a major innovation in low-energy computing management enabling to build and deploy highly energy-efficient networked applications.

Innovations on the path leading towards the realization of these main goals, which will jointly be created over the boundaries of individual projects through intense cooperation, are listed in the following table. Due to the fact that these innovations are achieved across boundaries, the numbering below does not relate to the numbering of the projects, but the innovations are listed/numbered in contextual order:

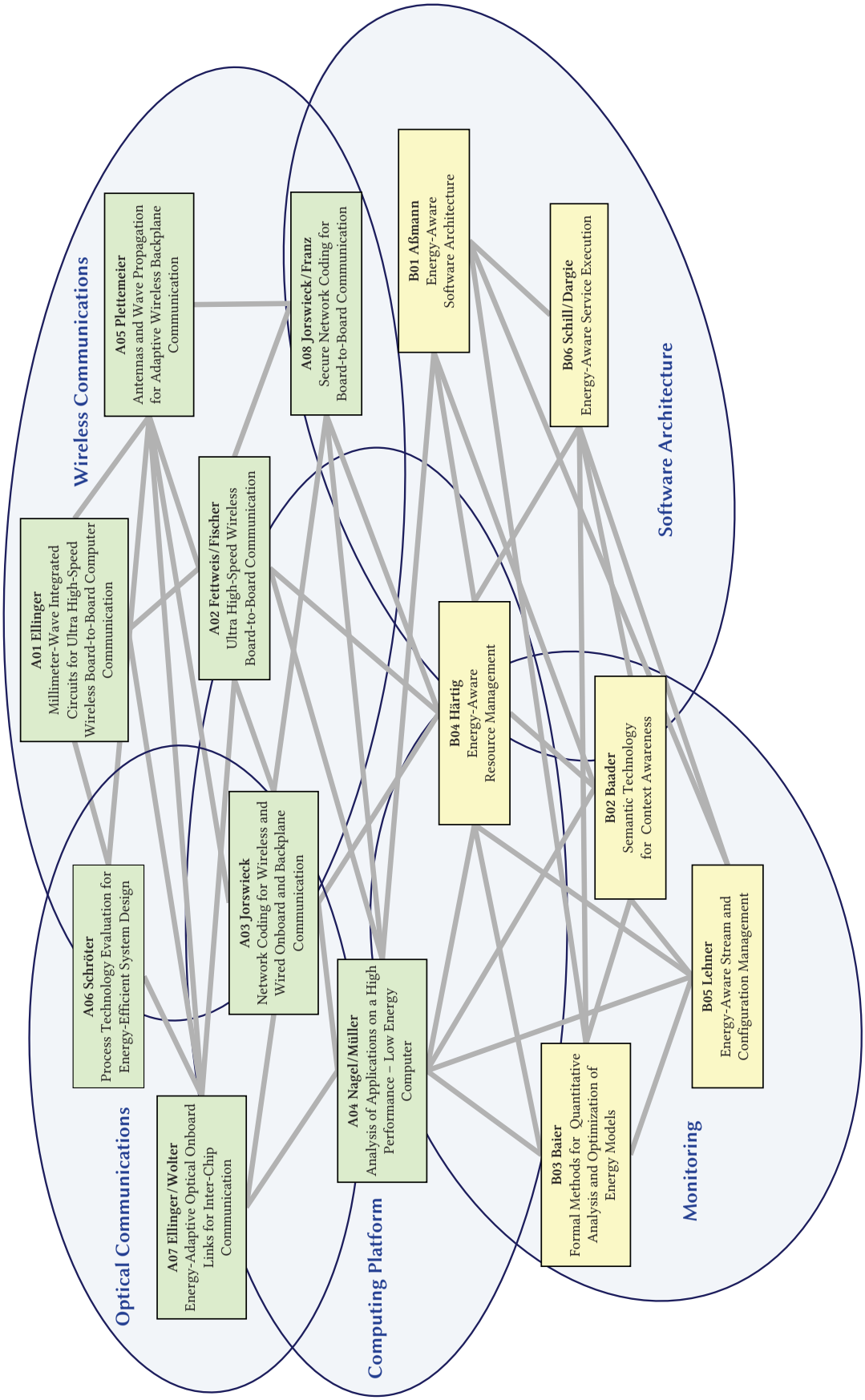
	Innovation	Explanation
I-A	Energy-adaptive computing (server and network) architecture	Architectural enablers for novel tree nodes including hyper-fat trees.
I-A.1	Unique hybrid connections and combination of communication technologies, global approach for system optimization	Unique combination of communication via E/O waveguide and wireless, enabling routing with low complexity.
I-A.2	Benchmarking of parameters such as speed (bandwidth, latency), power and distance	Unique possibility in one project to compare the pros and cons of all three communication approaches.
I-A.3	Hyper-fat tree architecture nodes enabled by wireless communication	Improve speed and latency and reduced power consumption on interconnections.
I-A.4	Energy-adaptive optical links	Optical links for inter-chip onboard communication with high interconnect density, high data rates and improved power consumption; adaptation of link parameters like data rate and power consumption with respect to actual link requirements.
I-A.5	Groundbreaking 100 Gbit/s low-power wireless links from one chip on one board to another chip on another board	Beam-steered wireless links allowing adaptive switching as at carriers in the frequency range from 100 GHz to 300 GHz.
I-A.6	Novel circuit architectures allowing operation close to the transit frequency of technology	E.g. oscillators with quadrature phase combining allowing 4 times the basic operation frequency and signal generation well above transit frequency.
I-A.7	Novel circuits for aggressively scaled silicon devices handling only small supply voltages and signal swings	Breakdown voltage doublers, etc.
I-A.8	Compact and numerical simulation models for advanced process technologies as well as automated design methodologies and associated CAD implementations for benchmark circuit design	Allows to perform cost-efficient technology comparisons and selection of most suitable circuit alternatives.
I-A.9	Novel packaging and assembling technologies	Addressing the CMOS III/V hybrid transceivers with high-speed 3D stacking and optical device-to-waveguide coupling for cost competitiveness and reliability.
I-A.10	Network coding for onboard and backplane communication	The static network nodes linearly combine packets and send them along multiple routes to their destination.
I-A.11	Security aspects of the network coding schemes	Analyze the security of network coding schemes suggested for communication within the HAEC Box and investigate possibilities to improve their security considering energy constraints.
I-A.12	Integrated memory access of logarithmic depth in the size of the hyper-fat tree	Approximate direct memory access with 0-copy chains, as in scalable crossbar switches.
I-A.13	Simulation model for running energy-adaptive software using a dynamic communication model	Benchmark the energy efficiency of an application running on a system based on the novel technologies above.

Table 1.3: Innovations and ideas (continued on next page).

	Innovation	Explanation
I-B	Closed energy control loop for computing and content distribution	Energy-awareness, energy-reactivity. Energy-optimization on all levels; crosscutting component and subsystem boundaries.
I-B.1	System-wide strategies for energy optimization	Energy-adaptivity crossing all levels of applications and subsystems, realized by monitoring and control interfaces of all software and hardware components.
I-B.2	Development of energy models and their employment for energy control	Energy models on all levels of abstraction: operating system, network middleware, application level.
I-B.2.1	Formal analysis of probabilistic energy/utility models	Compositional modeling approach and probabilistic model checking techniques for reasoning about energy/utility interfaces and quantitative analysis of energy-aware systems.
I-B.2.2	Context models based on semantic technology	Develop approaches for representing context information relevant for enhancing energy efficiency in a formally well-founded way. Integration of different context information into a coherent semantic view. Reasoning about context information based on this integrated semantic view.
I-B.3	Energy/utility functions and decision algorithms	Based on energy, utility and context models, decisions have to be made, based on energy/utility functions. Static precomputation of parametric energy/utility functions.
I-B.4	Energy monitoring technologies based on data synopses and anytime algorithms	Minimal-intrusive and distributed DSMS to monitor the whole SW stack; Development of energy-aware data synopses and anytime algorithms which follow the "need-to-know" principle.
I-B.5	Energy-adaptive software architectures (application and system software)	An application software architecture that adapts itself to user energy profiles and current energy context. It takes in monitoring, analysis information and computes optimization and control decisions. It works cross-layer (operating system, application and service management layer).
I-B.5.1	Energy-adaptive application software architecture	Architectural energy autotuning, based on specification of reconfigurable architectures with model-driven development, autotuning rewriting technology and energy-contract negotiation.
I-B.5.2	Distribution power-management strategies	Distributed and adaptive power-management strategies based on energy-aware service selection, service relocation, service migration and service re-binding.
I-B.5.3	Holistic energy-aware resource management	Systematic derivation of energy-aware resource management principles from a holistic energy/utility function.

Table 1.3: Innovations and ideas (continued from previous page).

Overview of research projects and cooperation within the CRC



From	To	Type of cooperation
A01	A02	Dirty RF and system aspects
A01	A05	Interface to antenna, possible integration on chip
A01	A06	Model validation and feedback as well as technology evaluation
A01	A07	High frequency circuit design
A02	A01	Dirty RF and system aspects
A02	A03	System and channel models
A02	A04	Specifications and geometry discussions
A02	A05	Beamsteering requirements
A02	A08	System and channel models
A02	B04	Hardware capability characteristics
A03	A02	Network coding requirements on physical layer communications
A03	A04	Interfaces communication model – simulator
A03	A07	Communication schemes and coding
A03	A08	Network coding constraints on security aspects
A03	B04	Hardware capability characteristics
A04	A02	Specifications and geometry discussions
A04	A03	Interfaces simulator – communication model
A04	A07	Specifications and geometry discussions
A04	A08	Interfaces simulator – communication model
A04	B01	Run energy-adaptive application on the simulator
A04	B02	Available sensing capabilities of the hardware
A04	B03	Run-time information and relevant performance properties
A04	B04	Application characteristics
A04	B05	Simulated sensor data
A05	A01	Requirements for circuit elements (amplifiers, phase shifters)
A05	A02	Antenna models and channel characterization
A05	A03	Input from RF link to channel model
A05	A06	Performance requirements for circuit elements, HF measurement expertise
A05	A07	Requirements for packaging and interconnection
A05	A08	Characterization of the RF link
A06	A01	Semiconductor device modeling for wireless applications and experimental device characterization
A06	A05	Models for active integrated circuit elements, HF measurement expertise
A06	A07	Semiconductor device modeling and experimental high-frequency characterization
A07	A02	Communication parameters and conditions
A07	A03	Communication parameters and conditions
A07	A04	Performance parameters, specifications and geometry discussions
A07	A05	Packaging and interconnection models
A07	A06	Model validation and feedback as well as technology evaluation
A08	A02	Security requirements on physical layer communications
A08	A03	Security requirements on network coding
A08	A04	Interfaces communication model – simulator
A08	A05	Security-based beamsteering characteristic requirements
A08	B04	Hardware capability characteristics

Table 1.4: Basic cooperation (continued on next page).

From	To	Type of cooperation
B01	A04	Load the simulator with workload language
B01	B02	Specification of the high-level contexts that need to be recognized
B01	B03	Compositional modeling techniques for energy-aware architectures including models for their energy / utility functions
B01	B04	Energy / utility functions; run-time optimizations; dependencies of operating system and application system architecture
B01	B06	Cross-layer strategies for application architecture and service management layer
B02	B01	High-level context produced by the ontology system
B02	B03	Logical approaches for reasoning about energy-awareness
B02	B05	Context information for adapting synopses and analytical models
B02	B06	High-level context produced by the ontology system
B03	A04	Quantitative analysis of the energy usage of board communication mechanisms
B03	B01	Compositional modeling techniques for energy-aware architectures including models for their energy / utility functions
B03	B02	Probabilistic modeling and verification techniques for the treatment of incomplete or vague information of the context
B03	B04	formal methods for specifying and analyzing the energy / utility functions of hard- and software components
B03	B06	Probabilistic model checking techniques for evaluating power-management strategies of service execution platforms
B04	A02	Resource management principles
B04	A03	Resource management principles
B04	A04	Resource management model for the simulator
B04	B01	Functional requirements for actuators and sensors in the operating system
B04	B02	Available sensing capabilities of the operating system
B04	B03	Evaluation of OS-level resource management strategies
B04	B05	Supplier for a wide range of system information, e.g. disk speed, memory bus utilization, page fault rate
B04	B06	Low-level contexts and control interface pertaining to hardware resources
B05	A04	Deliver online system information in order to improve the HAEC simulator
B05	B01	Raw data and pre-processed data for offline decision support
B05	B02	Pre-processors of sensor data
B05	B03	Provide configuration repository to store different system models
B05	B04	Provide higher-level system information
B05	B06	Partially processed low-level contexts
B06	B01	Cross-layer strategies for application architecture and service management layer
B06	B02	Specification of the high-level contexts that need to be recognized
B06	B03	Probabilistic models for different adaptation strategies
B06	B04	Specification of the low-level contexts and runtime configuration requests
B06	B05	Specification of the low-level contexts

Table 1.4: Basic cooperation (continued from previous page).

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1.2.3 Positioning of the Collaborative Research Center within the scientific field

The consortium combines competence in the fields of software and service architectures, hardware components and broadband networks to form a critical mass of knowledge to tackle the existing problems of energy consumption and energy efficiency in today's and future information and communication technology (ICT). A comparable interdisciplinary initiative is unknown to the best of the consortium's knowledge. Due to the interdisciplinary character of this CRC, the corresponding international scientific environment can only be selectively reviewed here.

Of particular importance are major blocking factors, which limit current research initiatives in the field of energy-efficient ICT and which can be overcome with this CRC. They are identified below.

Isolated component optimization

Nowadays, hardware components are mostly optimized isolated from the entire system. This can achieve sufficient power reduction results as long as the component behavior does not affect other system building blocks. Conversely, if the low-power behavior of one building block affects other system components, new cross-component optimization methods are required to enable a dedicated system performance at reduced energy consumption. There are numerous examples for locally optimized low-power building blocks that finally lead to increased power consumption of the entire system. For instance, low-power/sleep modes of embedded IC solutions potentially introduce large wake-up durations and keep other network components idle until woken up again. Furthermore, various Analog-to-Digital Conversion (ADC) circuits used in communication receivers are known to require several tens of thousands cycles to run properly once woken up. The long wake-up delay of system components is not only a problem in communications but also in multi-processor compute clusters and server farms, where the stochastic system load introduces non-deterministic power-down behavior of certain subsystems, which finally leads to instabilities of the entire system if not properly controlled. In extreme cases, the autonomous power-down behavior is known to potentially result in states where the entire system uses almost all resources for toggling between power down and wake up modes, leading to highly inefficient processing and high power dissipation.

Potential: The CRC will deliver a local as well as global energy optimization technology and architectures without compromising the provision of highest performance computing.

Multi-gigabit short-range connections

One main bottleneck for achieving high computing power is the interconnect network and its hardware switching between processors, memory, storage and I/O.

Potential: To enable low-power consumption together with flexible adaptive hardware switching, the CRC will investigate a novel approach of using a hybrid combination of wireless beamsteered broadband links together with onboard-embedded optical links. Wireless communication with data rates of 10 Gbit/s at a 60 GHz carrier are currently investigated by leading research groups, e.g. at

TU Dresden, CEA-Leti Grenoble, IHP, UC Berkeley, as well as Georgia Tech. Achieving rates beyond 10 Gbit/s at carriers above 100 GHz is a pioneering field of research, being addressed only within confidential projects at Intel Research. Corresponding embedded optical interconnects, including the respective hybrid electro-optical transceiver modules, are being developed at selected leading groups. On the network level, the joint activities in the areas of information theory allow to come up with information-theoretic bounds (min-cut max-flow bound) for data transmission. Network coding is a novel technique, which can achieve this bound in complex multicast networks. The idea to linearly combine packets at several coding nodes can be implemented on several layers, on the physical layer by analog network coding, or at application or service layers. The combination with smart physical layer optimization techniques applied to beamsteering and channel coding will show the significant gains in terms of spectral efficiency while keeping the power consumption constant. Within the CRC we propose to create radical new technologies for creating high-performance low-power computing architecture and computing management. Clearly, this has a high potential for innovations, but also bears a high research risk.

Energy-unaware software development

Progress has been made in energy optimization of hardware and in operating systems and other lower level software. A large body of work was and is being conducted on scheduling algorithms for dynamic voltage scaling hardware and on improvements for the energy consumption of embedded, real-time or interactive operating systems. While most of this work is concentrated on single resources, we intend to develop a holistic resource management model, which maximizes energy efficiency over the entire system. However, today's application software development is completely energy unaware in building new applications and services. This leads to the *energy-ignorant* paradigm: application software systems are built to maximize performance and not to allow for power adjustments. During the last decades the power consumption of software systems has not been a success criterion for most industrial applications. Energy was cheap and available in unlimited quantity. Only very special applications running in embedded or autonomous environments had to deal with constrained resources. Due to this *energy ignorance phenomenon* there is little understanding in the software community about the relation between applications and their energy consumption. Almost all commercial and most academic software development methods, tools and processes lack a notion of power consumption altogether. Even modern approaches, such as Model-driven Software Development (MDSD) or Component-Based Software Engineering (CBSE), do not yet incorporate considerations about energy efficiency.

Potential: The CRC will deliver novel methods and technology for energy-aware software application design and architecture.

Lack of energy consumption measurability and modeling

Current ICT service users as well as system designers are not aware of the energy consumption of subsystems or particular services. This is mainly due to the lack of instruments for energy monitoring, energy modeling, energy tracing and due to the lack of appropriate energy/utility functions. While users can usually customize an application, they are not able to describe their "energy profile" (describing how much energy they want to spend) or their "energy/utility profile" (describing how much energy they want to spend for which quality of service). A conscious decision between alternative services or subsystem configurations to save energy is therefore impossible.

Potential: The CRC will deliver novel methods on energy modeling, energy measuring and energy/utility modeling.

Energy-unaware distributed service execution

The service-oriented architecture has enhanced the way applications are developed and services are deployed, managed and executed. Application developers are no longer forced to develop applications from scratch; instead, they can dynamically compose services and bind to them at runtime. So far, much of the research focus has been on performance and stability aspects. Whereas, the distributed nature of services and knowledge of workflows present new opportunities for energy-aware service execution, these have not been exploited to the full extend.

Potential: Within the CRC, new strategies for energy-efficient service execution will be developed. In particular, advanced techniques of energy-aware service selection, service consolidation and selective switching of hardware resources will be applied to frugally use the energy of distributed servers. Moreover, runtime negotiation between service providers and service consumers as well as infrastructure providers and service providers will enable energy-aware adaptation. By closely coupling the decisions to be made with the energy usage feedback of lower layers, the distributed service execution and adaptation strategies will become an integral part of the overall energy control loop.

These main blocking factors will be addressed by the CRC. However, already a large number of research groups are active in the different fields covered by this consortium. In the following, national and international research activities that are highly related to this CRC are discussed.

CoolSilicon

The region of Dresden has been successful in the acquisition of the BMBF-funded Cluster of Excellence ("Spitzencluster") CoolSilicon. This program is fully dedicated to research on the design and development of low-energy consumption of information and communications technology electronics. Partners of CoolSilicon include TU Dresden, TU Chemnitz, eight Fraunhofer institutes, as well as more than 30 companies. As the industrial partners dominate the research, the main focus is on shorter term results, which could make a market impact within five years. However, many ideas of the CRC were spawned out of discussions that took place between partners of CoolSilicon, which clearly gives the CRC HAEC the unique chance of using the strong network of cooperating partners of CoolSilicon for discussing the practicability of the long-term visions and innovations that will result from the HAEC research. As an example, the project CoolComputing (under leadership of Globalfoundries) within CoolSilicon is focusing on the development of low-energy microprocessor chips. In particular the focus within CoolComputing is on researching new semiconductor device and mask technology, as well as including the prospect of enabling very fast power-up and power-down capability for driving the power consumption of the processors in accordance to the processing load requirements of the application. Clearly, microprocessors that embed the technology being developed within CoolComputing would ideally help the concept of the HAEC Box. The energy savings of CoolComputing would then come on top of the concepts of the CRC HAEC, i.e. adding to the energy savings. Possibly, additional power savings could be exploited by making use of the adaptive powering of the processors of CoolComputing as they are being adaptively connected through the dynamically switchable interconnection of the HAEC Box. This depends on the outcome of CoolComputing and the capabilities that are being researched within that project. Obviously, as partners are involved in CoolSilicon as well as in the planned CRC HAEC, a large benefit will be drawn from understanding and discussing details of our forthcoming innovations with leading-edge companies located in and around Dresden. This CRC HAEC with its visionary approach and long-term goals should therefore clearly excel by using the interactions being offered by CoolSilicon and the shorter term results coming out of the CoolSilicon program.

Wireless multi-gigabit short-range communication

Multi-gigabit systems in the 60 GHz band are also investigated by the Berkeley Wireless Research Center (BWRC), the University of California at Santa Barbara (UCSB) and the GEDC group at Georgia Tech, which are among the leading groups in that area. DFG is currently supporting a six-year Priority Program UKoLoS on "Ultra-Wideband Radio Technologies for Communications, Localization and Sensor Applications". The aim is to build a nation-wide network of 60 GHz UWB expertise able to reach out for international cooperation. Investigations on the commercial usability of wireless UWB communication in the 60 GHz band are the topic of the BMBF project "EASY-A – Enablers for Ambient Services & Systems, Part A – 60 GHzBroadband Links", where data rates up to 10 Gbit/s are considered. EASY-A is coordinated by the Leibniz-Institut für innovative Mikroelektronik (IHP) and shares with HAEC the principal designers and investigators of both the mm-wave IC front-end (A01) and the baseband signal processing (A02).

Achieving rates beyond 10 Gbit/s at carriers above 100 GHz is still a pioneering field of research. The aim of the BMBF project MILLILINK is the embedding of 40 Gbit/s wireless links at 200 GHz carrier frequency into optical networks, considering ranges of up to 1 km. In this scenario, for the generation of a 60 GHz baseband signal the optical signals are directly modulated by a photo-diode and no further digital baseband processing is considered. Sony has recently announced an integrated chip-solution for wireless board-to-board interconnects achieving a data rate of 11 Gbit/s at a carrier frequency of 56 GHz. The concept relies on inductive coupling between the transmitter and receiver and is therefore limited to distances below 14 mm.

The HAEC scenario strives for data rates of up to 100 Gbit/s with a coverage of several centimeters but still high energy efficiency (lowest energy per transmitted bit) using the frequency range of 100 GHz to 300 GHz. None of the above mentioned project focuses on the specific board-to-board mm-wave wireless communication.

Interference is recognized as one of the most limiting factors of current wireless communication systems. Therefore, a novel DFG focus program "Communications in Interference Limited Networks (COIN)" has started research on novel paradigms for efficient wireless communications. The distributed coding and data processing as well as cooperative novel scheduling and routing protocols as well as network coding will be studied in COIN.

Another challenge is the antenna design. Some universities and space agencies, e.g. NASA, ESA, CNES and DLR, show activities in the development of integrated mm-wave antennas for sensor, radar and radiometer applications and for short-range communication at 60 GHz. For instance at Caltech and NASA/JPL the research group of Dr. Siegel specializes in the development of a wide range of specialized sensor and source devices, components and instruments spanning the frequency range between 100 GHz and 10 000 GHz. Research work at Chalmers University of Technology in Göteborg/Sweden for example is partially related to the HAEC hardware. The Microwave Electronics Laboratory is working on various mm-wave projects, including 60 GHz MIMO systems and 220 GHz integrated receivers. In 2007, the group of Prof. Herbert Zirath in collaboration with FOI, Fraunhofer Institute IAF, Omnisys Instruments AB and SAAB within the project NanoComp presented a 220 GHz GaAs MMIC including an antenna. According to them, their work and applications include "integrated radiometers for space-borne earth observation satellites, radiometers/radars for security scanning, high data rate radio links for faster mobile Internet access". Currently there is only a standard for 60 GHz systems, ratified in 2009. The system designed in HAEC addresses highly adaptive communication within server nodes, not mobile systems. Both applications require high energy efficiency. Highly efficient mobile devices can extend battery life while highly efficient servers will reduce the power consumption significantly, thereby the burden upon the environment. The research group at Chalmers University of Technology and HAEC both address the power consumption related

with Internet access, but focus on different concepts and work on different system components. HAEC will organize an open cluster of national and international experts to frequently exchange ideas and experiences.

IC technology

Board-to-board mm-wave wireless communication. Power-efficient radio frequency integrated circuits fall in the scope of various international research projects. The Microsystems Technology Office at the US Defense Advanced Research Projects Agency (DARPA) runs the projects COSMOS and SMART. The COSMOS project aims at combining for a given application the best available technologies at lowest cost by fabricating high-speed III/V HBT and HEMT building blocks on top of finished CMOS wafers. Integrated surface-emitting panel architecture for mm-wave transceiver arrays are investigated in the project SMART. In the EU-FP7 project DOTFIVE, technically managed by the principal investigator of the device technology project A06, a SiGe HBT BiCMOS technology with 500 GHz operating frequency is presently being developed to address mm-wave applications. The DFG Cluster of Excellence "Ultra high-speed Mobile Information and Communication systems (UMIC)" at RWTH Aachen is an academic research center with strong links to wireless industry and mobile network operators, with RF Subsystem and System-on-Chip (SoC) Design being one of the main research areas. At TU Darmstadt the DFG Research Training Group "Tunable integrable components in microwave technology and optics" covers tunable, reconfigurable and easy to integrate microwave and optical components for smart frequency and space-agile next-generation sensor and communication systems. New components are developed for operation over a very broad frequency range. The EU-funded MIMAX project aims at MIMO transceiver development that allows a significant improvement concerning performance on the one hand and power consumption on the other, by using multiple-antenna techniques in the analogue domain to avoid power consumptive digital baseband MIMO processing. Tools for the design of power adaptive integrated circuits and processors are developed by Prof. Wolfgang Nebel (Carl von Ossietzky Universität Oldenburg) within the EU-FP6 project MAP_2 funded by the European Commission. Furthermore, there are the EU-funded projects FLEXWIN, IPHOS and OMEGA.

None of the above mentioned project focuses on the specific case of board-to-board millimeter-wave wireless communication, although the use of mm-wave carrier frequency for high data rate communication is an active field of scientific and engineering research. The majority of research programs for multi-Gbit/s data links still focus on 60 GHz carriers, which are very attractive for mass consumer markets, but still present unsolved technical challenges. The system scenario of HAEC differentiates from other programs and applications in the very short link range and the ultra-high data rate required. Relevant and useful overlaps are expected with exciting projects and programs at TU Dresden and IHP. IHP is very active in the field of mm-wave IC fabrication and design for wireless communication. The planned cooperation – possibly as an IHP Joint Lab at TU Dresden – will enable knowledge transfer and strengthen Germany's competitiveness in silicon-based mm-wave wireless communication.

Onboard optical links for inter-chip communication. High bandwidth on/off-chip interconnects are of central importance for integrated circuit design and hence fall in the scope of this CRC, where especially optical onboard (inter-chip) communication attract attention for mid-term perspectives and even optical on-chip (intra-chip) for long-term research agendas, cf. Intel. The most important advantages and promises of optics in this field are to enable higher bandwidth-length products and to allow higher aggregated data rates for a given interconnect density in comparison to electrical links. Hence, optical interconnects are considered to have the potential of cost and power savings

and recently a lot of research is attracted to this field. The most relevant and dominant activities on optical on-chip interconnects in the HAEC context are those at IBM Research and Intel Research, which pursue similar project goals. Furthermore, also at national level the significance of this research field was revealed, and there are the BMBF projects SiliconLights, MONALISA and MISTRAL as well as several DFG-funded projects, such as "Aktive und abstimmbare mikrophotonische Systeme auf der Basis von Silicon-On-Insulator (SOI)" at Technische Universität Hamburg-Harburg, "Schnelle Datenregeneratoren für die hochbitratige opto-elektronische Datenübertragung basierend auf Silizium-CMOS-Technologie", "Integrierte elektronische Datenentscheider für 40 Gbit/s Systeme in Silizium-Germanium-Kohlenstoff-Heterobipolartechnologie" and the Integrated Research Training Group "Mikro- und Nanostrukturen in Optoelektronik und Photonik" at Universität Paderborn, the DFG Center for Functional Nanostructures and DFG Graduate School "Karlsruhe School of Optics and Photonics (KSOP)" at Karlsruhe Institute of Technology (KIT), the DFG Graduate School "Erlangen Graduate School in Advanced Optical Technologies (SAOT)" and the DFG Integrated Research Training Group "Steuerbare integrierbare Komponenten der Mikrowellentechnik und Optik" at Technische Universität Darmstadt. Furthermore, the EU funds the projects WADIMOS, PLATON, BOOM and SOFI in this area. The above mentioned projects and research groups do not consider or explicitly enable energy adaptivity in the optical links, and they mainly focus on performance issues rather than investigating or improving the energy efficiency. However, some overlap occurs in the basic system architecture and system assembly, e.g. IBM's Terabus or Intel's approach. Furthermore, most of the research projects either focus on fiber-optics (backplane networks, long-haul systems) or integrating photonics into silicon, i.e. fabricating silicon or nano-based optical devices. Overcoming the main challenges for enabling highly integrated and energy-efficient optics into silicon technologies requires combined efforts, developing disjoint or similar approaches and tight cooperation. In particular, a cooperation with TU Berlin and IHP is highly desirable to investigate the challenges of the different research fields and to guarantee Germany's competitiveness in silicon-based optical communication. Specifically, the energy efficiency and the energy adaptivity of the optical links must be investigated and can further ensure Germany's leadership.

Computing

The power-management group at the department of computer science led by Prof. F. Bellosa (Universität Karlsruhe) investigates interfaces between hardware components and operating systems that finally enable server power management, I/O power management as well as dynamic frequency clock scaling. The group is involved in a joint research project ZeuS ("Zuverlässige Informationsbereitstellung in energiebewussten ubiquitären Systemen"/Energy-aware ubiquitous computing) of the universities of Karlsruhe and Mannheim, having the major objective to balance energy and quality based on predictable security and reliability of information flow processes. The project focuses on sensor networks also.

Under the Green-IT slogan, mainly data farms are addressed. With virtualization technologies, e.g. cloud computing, an enormous energy-saving potential could be exploited. Unlike data farms, HPC systems have to provide a steady high computing performance. The demand to add power metrics to performance results is demonstrated by the effort to create a list of the world's most powerful computers similar to the top 500 list (top500.org) but with added values for power consumption (green500.org). The Standard Performance Evaluation Corporation (SPEC) released the first power/performance benchmark in December 2007 (SPECpower_ssj2008). This benchmark focuses on the power consumption of a machine running server side Java under different load conditions, focusing on web hosting services. This small number of initiatives illustrates the need of appropriate

power benchmarking and monitoring techniques not only in the high-performance computing sector, techniques that are studied in the course of this CRC.

Simulations for performance prediction of computer systems have been used since the early days of computer science. The Barcelona Supercomputing Center via the development of the tool DIMEMAS, focuses on the impact of different networking parameters on the performance of an application. The NSF CSR project (University of Georgia, Athens, USA) "MPI-PPA: Improving Efficiency of Large-Scale Clusters Through Statistical Performance Prediction" tries to statistically predict the parallel speedup of scientific applications. The simulator to be developed in the course of this CRC will use the experiences of these tool developments. However, it goes far beyond the existing simulations incorporating an energy utilization function and a dynamic communication model to verify the impact on energy efficiency of the different HAEC hard- and software innovations.

Service execution

Interest in stable and efficient service execution and management has increased recently. While these topics are addressed in one way or another, it is difficult to state explicit overlapping issues. However, some of the methods and algorithms that are developed or investigated to tackle efficiency or performance challenges are interesting and can be reused to support energy-aware distributed service execution. For example, the DFG project "Analysis and modeling of complex networks" (DFG Research Center Matheon) employs stochastic models to make networks efficient. The stochastic modeling can give some insight into how the energy cost of distribute service execution can be analyzed using probabilistic models. A complementary approach to energy-aware software engineering and distributed service execution is the DFG SENSORIA project (Software engineering for service-oriented overlay computers), which investigates several techniques and methods to make service-oriented software development flexible and efficient. The EU-FP7 project GAMES aims to develop algorithms and web tools that optimize the relationship between energy consumption, quality-of-service, performance and computational resources (both physical and virtual) of IT service centers. Similarly, the EU-FP7 project EARTH aims to optimize the energy efficiency of mobile communication systems by developing deployment strategies and network management solutions. Though these projects aim to address the energy cost of IT infrastructures, it is rather early to critically look into the proposed multi-variable optimization strategies. However, due to the overlapping research interest, there is a potential for exchanging experience and ideas in the future.

In the framework of the DFG Scientific Priority Program 1140, the subproject "Entwicklung eines Ad-hoc Service Management für selbstorganisierende vernetzte mobileSysteme", several channel parameters between mobile users and backbone servers are exploited to support resource-efficient service delivery. Here as well, the energy consumption of the links and the servers is not explicitly taken into account, but the applied methods match well with projects from the software architecture group of this CRC. Specifically, these methods are based on the analysis of non-functional properties, such as power consumption, of complex systems on a set of well defined and easy-to-process variables. Hence, the research activities in these fields are worth mentioning here due to their potential impact on the CRC projects.

At the international level, the ARAGORN project under the European Commission's 7th Framework Programme applies methods originating from artificial intelligence to increase wireless communication system efficiency. The project proposes cross-layer network design, aiming at resource, e.g. energy, usage optimization. The EU-FP6 project MODELPLEX aims at providing software controlled system/device monitoring tools. Also, MODELPLEX will deliver a model-driven performance analysis technique, which can be employed for simulations in HAEC. The FP6 project MUSIC develops an open software platform for the development of self-adaptive mobile and distributed applications.

MUSIC is a good example for a variety of initiatives in the software sector where the energy aspect is not addressed explicitly, but enabling technologies are researched for adaptive autonomous, i.e. self-managing, applications and device engineering. Nevertheless, it is notable that software adaptation at runtime based on energy context variables as proposed in HAEC is a novel paradigm that is addressed by none of the projects mentioned earlier.

Data stream technologies

There are some national and international research projects in the field of data stream management. A notable German research effort is the previously DFG-funded PIPES project at Universität Marburg which is further developed by the RTM Realtime Monitoring GmbH. PIPES is a flexible and extensible infrastructure providing fundamental building blocks to implement a data stream management system, which can deployed in different fields of application. The Odysseus project from Universität Oldenburg, which also has to be mentioned here, provides a framework to easily develop data stream management systems. Furthermore, the project AnduIN from TU Ilmenau provides in-network query processors and a data stream management system for wireless sensor networks. All these projects provide data stream systems on a very macroscopic level whereas our research efforts within HAEC are focused on a single system which results in different and more specific requirements.

Internationally, the following data stream projects should be mentioned: AURORA and BOREALIS (cooperation between Brandeis University, Brown University and MIT), TelegraphCQ (UC Berkeley), STREAM (at Stanford University; it was stopped in 2006 though) and COUGAR (at Cornell University). More recent research activities are the Lahar project (University of Washington), which is focused on so-called Markovian streams, i.e. compact representation of imprecise, ordered data, as well as the DejaVu project (ETH Zürich) which explores scalable complex event processing techniques for streams of events.

However, none of these systems provide any guarantees with regard to the quality of the processing result. Furthermore, they are not adaptive in terms of the resource allocation required when aiming for a certain result quality. Based on the QSTREAM system (TU Dresden), we attempt to develop an optimized data stream system with regard to these two aforementioned criteria. Additionally, we place particular emphasis on the analysis side of data stream processing which should be accomplished by the application of data synopses.

We are not aware of other CRC or specific research projects focusing on this very issue as of now.

Software architecture and modeling

On the international level, the 7th framework EU IP SPEEDS develops a “hybrid rich component model” (HRC) by which real-time, security and dynamic aspects can be modeled. The component model is structurally based on SysML and treats the different qualities in views. Hence, it is amenable for another view on energy, for which it will be investigated in HAEC. The SPEEDS HRC component model is followed also in the ARTEMIS project CESAR, where it shall be integrated into a future reference technology platform for embedded systems development in Europe.

The EU project COMPLEX, coordinated by OFFIS institute, investigates energy management from the perspective of hardware/software co-design of embedded systems. In particular, they investigate model-driven approach to software development and overall system simulation for exploration and optimization of energy use. Although their focus is on design time guidance, in contrast to runtime optimization, research results of COMPLEX can be used for HAEC and vice versa. The BMBF project CoolSoftware, part of the BMBF Cluster of Excellence CoolSilicon, researches into energy-aware component models and will contribute its results to HAEC. It is discussed in detail in project B01.

Security of network coding

Investigations regarding security aspects within the CRC HAEC will focus on network coding, a novel paradigm that will be applied for onboard and backplane communication within the HAEC Box. Security aspects of network coding are currently also investigated in the EU-FP7 project N-CRAVE ("Network Coding for Robust Architectures in Volatile Environments"). N-CRAVE started in January 2008 and will end in December 2010. The main objective of this project is robust communication within extremely volatile environments considering changes of topology, accidental errors as well as possible attacks. The outcomes of this project are important for the CRC HAEC. However, the scenario considered within HAEC is only partly comparable to that of N-CRAVE. Within HAEC, we assume both wired and wireless onboard and backplane communication, while N-CRAVE focuses on volatile networks, such as sensor networks. In this CRC, we do not aim at developing new network codes but evaluate, adapt and utilize existing ones for enforcing our protection goals. We will consider results of N-CRAVE as possible inputs for HAEC. Particularly, we will investigate whether solutions proposed in N-CRAVE can be applied within our scenarios.

1.2.4 Integration of the Collaborative Research Center into the local scientific environment

The planned research program is based on proven excellence of the participating institutes of TU Dresden and will extend and complement existing research activities. The participating principal investigators all belong to TU Dresden, which has – based on an agreement between the TU Dresden and the Government of the Free State of Saxony in 2004, forming the starting point for shaping a successful profile for the university – defined six profile lines:

- Regenerative medicine and molecular bioengineering;
- Material sciences, biomaterials and nanotechnology;
- Computer engineering;
- Population, infrastructure and traffic;
- Water, energy and environment;
- Social change, culture and education.

These profile lines are defined as interdisciplinary topics and activity areas and provide an orientation to target the development of new and existing teaching and research areas. The profile lines intentionally avoid setting limitations with respect to structures and methods. Instead, they are designed to release the potential for innovation and synergy held within the interdisciplinary approach. The broad, interdisciplinary nature of the profile lines has placed the TU Dresden in a position to maximise the enormous scientific potential of the Saxon capital, Dresden, with its numerous non-university research and cultural institutions and extend this into clusters of research excellence. During this process, four focal points from the six profile lines have emerged in which Dresden research has already reached significant international visibility. The *DRESDEN-concept* ("Dresden Research and Education Synergies for the Development of Excellence and Novelty") has formalized cooperation between the university and research institutes in Dresden for creating synergies, e.g. sharing research and teaching capacities, in four defined Scientific Areas each run by a Scientific Area Committee (SAC):

- SAC-1: Biomedicine and bioengineering;
- SAC-2: Information technology and microelectronics;
- SAC-3: Materials and energy efficiency;
- SAC-4: Culture and knowledge.

The planned CRC belongs to the profile line "Computer engineering" and to SAC-2 "Information technology and microelectronics" and will strengthen TU Dresden's position in the application for the

Cluster of Excellence "Advancing Electronics Dresden". It is also a typical example for one of the core values of TU Dresden to strengthen interdisciplinary cooperation.

From the application-oriented point of view, the planned CRC is of utmost importance for Dresden and the surrounding region, the largest microelectronics hub in Germany and, indeed, Europe. This focus is documented by:

- The network Silicon Saxony, founded in 2000, is the largest microelectronics network in Europe currently comprising approximately 280 partners from industry, applied research and academics.
- The BMBF Cluster of Excellence CoolSilicon (initiated in 2008) is fully dedicated to research on design and development of energy-efficient information and communication technologies.
- The Fraunhofer Center of Nanoelectronic Technologies and the Nanoelectronic Materials Laboratory (NaMLab gGmbH) were founded in the last 5 years.
- The network, Organic Electronics Saxony e.V., founded in 2008 to strengthen organic electronics in Saxony. Saxony, and especially Dresden, is Europe's largest cluster for organic semiconductor R&D and manufacturing. More than eight research institutes and 15 companies with over 850 employees (2010) are active in this quickly growing, new technology.

Apart from microelectronics being historically rooted in Dresden region, also the topic of software development is another economical basis for Dresden, which is documented by:

- The CRC principal investigators Prof. Aßmann and Prof. Schill are members of Software Saxony (a subnetwork of Silicon Saxony), founded in 2006, with over 50 members from industry, applied research and academics from Saxony. Most of the members are located in Dresden.
- The yearly Innovation Forum of Software Saxony[2], organized by members of the CRC, such as Prof. Aßmann, takes place in spring 2010 in the premises of the computer science faculty and is attended by 300–500 visitors. In 2010, the Innovation Forum featured the tracks "Embedded Software", "Web and Business Software", "Factory Automation Software", "Visualistics' and "CoolSilicon", with additional student exhibition tracks[3].

A special value as foundation for this CRC is given by the BMBF Cluster of Excellence CoolSilicon, which has been established by the German Government in 2009. The CoolSilicon Cluster of Excellence is located in the heart of Silicon Saxony, stretching from Dresden over Freiberg to Chemnitz. Over 60 partners, led by TU Dresden, from industry and academia cooperate to develop concepts for low-power, high-performance ICT solutions: 19 chairs from four different technical universities – among them are eight PIs of this CRC –, eight research institutes, global players in microelectronics, such as Globalfoundries, AMD, Infineon, X-Fab and a multitude of small and medium size enterprises. Research within CoolSilicon covers three focus areas: micro-/nanoelectronics technology, communication systems and wireless sensor networks.

Within CoolSilicon application-oriented research is being conducted for increasing the energy efficiency of ICT. In HAEC, the focus is on basic research with very high risk, as can be seen by the idea of the HAEC Box and the software architecture design concepts. However, due overlapping partners between HAEC and CoolSilicon, cross-fertilization and strengthening of the research activities is expected. In particular, it is expected that transferring the results of HAEC research will help to develop the Dresden region from a pure chip manufacturing site to a system solution site which will massively improve the chances for further regional industrial development.

Finally the growing importance of Dresden in the CRC's research fields is documented by the decision to hold the most important European event for electronic system design and test, the IEEE DATE conference, bi-annually in Dresden since 2010. The most important semiconductor fair SEMICON is in Dresden since 2008.

[2] http://www.software-saxony.de/?tag=innovationsforum
[3] http://output.inf.tu-dresden.de

Apart from this large application-oriented research program several basic research activities are either presently still running or have been completed, forming a basis for this CRC. Examples include the CRC 358 "System Design Automation", the DFG Research Training Group "Nano- and Biotechnologies for Packaging of Electronic Systems" (GRK 1401), the young investigators group InnovaSens, funded by ESF/Saxony and several projects mentioned in Section 1.2.3, such as EARTH, DOTFIVE, COIN, MIMAX, to which HAEC PIs already contribute. That the topic of energy and material efficiency becomes more and more important as research driver at TU Dresden is documented by e.g. the newly submitted proposal for a DFG Research Training Group "Integrated design of interactive energy-efficient systems" of the department of Mechanical Engineering and the planned graduate school DIGS-E3 hosted by SAC-3 and SAC-2.

The CRC will help to strengthen the already existing cooperation between the Electrical Engineering and Information Technology department, the Computer Science department and Natural Sciences department at TU Dresden. The collaboration of the three participating departments guarantees a full completion of all tasks. Until now, several co-operations between these institutions were established, creating important synergy effects. Among the members of the CRC, energy efficiency has been the topic of many research projects. Thus, the CRC allows a continuation of current work. With the additional positive effects of the support from the other CRC members, the scientific output will substantially increase. Furthermore, additional new research topics can be dealt with and successfully completed. An overview of important examples of cooperation is shown in the following Table.

		Aßmann	Baader	Baier	Ellinger	Fettweis	Fischer	Härtig	Jorswieck	Lehner	Nagel	Franz (Pfitzmann)[4]	Plettemeier	Schill	Schröter	Wolter
CRC 358	closed					×		×							×	
EASY-A					×	×										
Comquad		×						×		×		×		×		
Conmore			×											×		
RTG INF-2								×			×			×		
eMuCo						×		×								
Precon		×								×				×		
SSONET												×		×		
CoolSilicon	running	×			×	×			×		×		×		×	×
Theseus										×				×		
UKoLoS						×			×							
QuaOS				×				×								
CIAGAS													×			×
RoSI	submitted	×	×							×		×		×		
QuantLA			×	×												
IKT 2020[5]										×	×		×			
EveryWare[6]		×						×		×				×		

Driven by the former CRC 358 "System Design Automation", in 1999, the university started a new interdisciplinary degree program "Informationssystemtechnik" (computer engineering) that equally

[4] Prof. Pfitzmann passed away on September 23, 2010. Dr. Franz will represent his group within the CRC.
[5] "HPC-Software für skalierbare Parallelrechner".
[6] FlexCloud, EDYRA, ZESSY.

features courses from the Electrical Engineering and the Computer Science area. This program is specifically designed to address the increasing demand for combined hardware/software information system solutions and their holistic design. The HAEC CRC fits perfectly into this profile and will further promote the structural development of TU Dresden in this direction. Furthermore, the CRC will also influence the master program "Nanoelectronic Systems" which is currently under development. This course will be one of the most valuable structural contributions of TU Dresden to CoolSilicon work program and results. It is designed to meet the needs of CoolSilicon partners and will cover nanoelectronics technologies, system and circuit design, with special focus on energy efficiency.

If TU Dresden succeeds in the federal excellence initiative and receives funding for the new Dresden International Graduate School of Emerging Materials for Energy Efficiency (DIGS-E3), the CRC will contribute to the PhD program "EEComp – Energy-Efficient Computing". Several HAEC PIs are planned to be involved as DIGS PIs so that a fruitful teaching, direct dissemination of research results and vice versa – the possibility to recruit the best brains as PhDs for the CRC are ensured.

In particular, in case this CRC receives funding, *the university has committed to establish a new chair for processor design* by the end of Phase I (years 1–4) since at the current time we believe that this area will have a key role within Phases II and III (years 5–12). The expert in processor design will analyze the potential of the new enabling technologies developed within Phase I of HAEC and develop new computer design concepts that exploit their capabilities. In Phase II (years 5–8) we expect to set up an Integrated Research Training Group ("Graduiertenkolleg") at TU Dresden.

1.2.5 National and international cooperation

Several HAEC PIs have already established cooperation with other research institutes and industry which will be intensified or renewed in the course of CRC.

Berkeley Wireless Research Center (BWRC)

The BWRC, now in its second decade, addresses the design, conception and implementation of the next-generation integrated wireless systems in state of the art CMOS (and related) technologies. The focus is on integrated circuit and system advances needed to enable a vision of truly ubiquitous wireless, including the design of energy-efficient high data-rate links at 60 GHz and above. This topic comprises on-chip antennas and RF (Ali Niknejad), RF and analog signal processing (Elad Alon) as well as high-speed digital design (Borivoje Nikolić). The group consists of circuit designers who interact with system engineers, e.g. David Tse, to design efficient communication systems. Operating at mm-wave frequencies using technologies with lossy substrates requires novel circuit design techniques as well as accurate high-frequency modeling of active and passive devices. Also, new system design methodologies will be needed to account for the limited performance of CMOS microwave circuits at 60 GHz along with the huge amounts of available bandwidth. As discussed with BWRC, a close cooperation for achieving faster and sustained success in research between the BWRC and the CRC HAEC is envisioned. On the HAEC side this includes in particular Dirk Plettemeier, Frank Ellinger, Gerhard Fettweis, Eduard Jorswieck and Michael Schröter.

University of California at Santa Barbara (UCSB)

The *Electrical and Computer Engineering (ECE) department* at UCSB enjoys world-class reputation and is known for its high-impact interdisciplinary research. Among others areas, research is carried out in communications and signal processing, electronics and photonics targeting high-speed and high-efficiency in a very diverse set of application scenarios.

The *High-Frequency Electronics Group*, led by Mark Rodwell, and the *Wireless Communication and Sensornets Laboratory*, led by Upamanyu Madhow, actively cooperate on mm-wave communication system research, addressing fundamental questions posed by the new field by acknowledging that the multi-Gbit/s data rates of mm-wave systems require rethinking the development of radio-transceiver hardware and signal processing with a co-design approach. Remarkable results were achieved through this interaction, for example, in the field of mismatch compensation of high-speed time-interleaved ADC design.

Cooperation between the ECE Department of UCSB and CRC HAEC at TU Dresden exists in the form of short- and long-term exchanges of researchers. Corrado Carta was a research fellow at the High-Frequency Electronics Group of UCSB in 2006–2008 and will be a senior scientist involved with project A01, with Frank Ellinger. The cooperation with the Wireless Communication and Sensornets Laboratory at UCSB has been established in 2010 by a three-month research visit of Stefan Krone – member of the scientific staff in Gerhard Fettweis' group – which has been funded by the German Academic Exchange Service.

Scientific Priority Program "Dependable Embedded Systems"

Computer hardware is constantly decreasing structure size, making it prone to external influence such as radiation-induced hardware faults. This is expected to become more significant in the future and requires new solutions for hardware and software fault-tolerance. The *Scientific Priority Program "Dependable Embedded Systems"* represents a DFG initiative to create such ideas for embedded multicore systems. The first funding phase of the SPP is going to commence by the end of 2010. Prof. Hermann Härtig is currently the only HAEC PI who also is a part of the SPP. As the principle requirements for multicore fault tolerance are also of importance for the HAEC Box, we clearly envision that further HAEC PIs may apply for future funding periods of the SPP.

National ICT Australia (NICTA)

NICTA is Australia's Information and Communications Technology Center of Excellence. Its main research themes cover embedded systems, networked systems, making sense of computer-generated data and managing the complexity of modern computer systems. Four PIs from the HAEC consortium currently collaborate with NICTA researchers: Prof. Hermann Härtig cooperates with Prof. Gernot Heiser, whose group works in the fields of embedded mobile systems and also researches energy efficiency and modeling techniques. The latter fields are of direct relevance for the HAEC project. Prof. Christel Baier's partners at NICTA are Prof. Rob van Glabbeek and Prof. Annabelle McIver. Rob van Glabbeek works on mathematical models and formal languages for the representation of distributed systems and the verification of statements about them. The expertise of Prof. Annabelle McIver is in the area of probabilistic logics and reasoning, tools for performance evaluation and applications of probabilistic systems. Prof. Franz Baader cooperates with Dr. Peter Baumgartner, who is a principal researcher at NICTA and manages their group "managing complexity", which employs formal methods for various applications as, for instance, situation-awareness. Together they have developed a logic-based framework for situation-awareness, which will be extended within the CRC HAEC. Prof. Gerhard Fettweis has cooperated with Prof. Gernot Heiser and Dr. Frank Engel on researching the design of IP blocks for a flexible software defined radio platform for global satellite positioning systems.

Artist Network of Excellence (NoE)

The EU-sponsored Artist NoE aims at spawning cooperation between leading researchers in the area of embedded systems. The NoE channels the efforts of leading European researchers and maintains

international collaboration programs, regular summer schools and workshops. From the HAEC partners, Prof. Hermann Härtig is affiliated partner in the Artist NoE's "Operating Systems & Networks" cluster and has collaborations with Prof. Alan Burns (University of York, UK) and Prof. Rolf Ernst (TU Braunschweig), who both work in the fields of real-time and embedded systems. Although focussing on embedded systems, the topics covered in this NoE are also relevant for operating system research within HAEC.

Furthermore, Prof. Christel Baier from the HAEC consortium is affiliated with the NoE through the cluster "Modeling and Validation" and contributes with her works in probabilistic and stochastic model checking. She has close cooperation to the Artist core members Prof. Boudewijn Haverkort (Embedded System Institute Eindhoven) and Prof. Wang Yi (Uppsala University). Both are experts in formal methods for the quantitative analysis of distributed systems.

BMBF Cluster of Excellence CoolSilicon

As already mentioned in Section 1.2.4 eight PIs, namely Profs. Fettweis, Ellinger (Leader Area Management Board 2), Plettemeier, Jorswieck, Aßmann, Nagel, Wolter, Schröter, are involved in CoolSilicon which aims at energy-efficient solutions for ICT and addresses application-oriented, HAEC-relevant research topics. Structurally CoolSilicon strengthens the regional collaboration with non-university research institutes like Fraunhofer and with industrial partners. So cooperation within and with CoolSilicon will mainly be important to find partners for validation and verification of CRC research results and to transfer them into applications.

Scientific Priority Program UKoLoS

UKoLoS stands for "Ultra-Wideband Radio Technologies for Communications, Localization and Sensor Applications". It is the 6-year priority program (Schwerpunktprogramm) SPP1202 launched by German Research Foundation (DFG; deutsche Forschungsgemeinschaft). UKoLoS aims at fostering national and international cooperation by establishing interdisciplinary research projects on highly innovative application areas. The three main focuses of: (i) communication; (ii) localization; and (iii) sensor technology.

Two principal investigators, namely Prof. Fettweis (A02, Z01) and Prof. Jorswieck (A03, A08), are involved in this exclusive framework which is comprising highly regarded national and international communications experts. In close cooperation Collectively with well-renowned scientists like Prof. Holger Boche (TU München), Prof. Robert Fischer and Prof. Johannes Huber (Friedrich-Alexander-Universität Erlangen-Nürnberg), Prof. Lutz Lampe (University of British Columbia (UBC), Kanada), Prof. Friedrich Jondral (Universität Karlsruhe (TH)), Prof. Martin Haardt (TU Ilmenau) and Prof. Reiner Thomä (Gottfried Wilhelm Leibniz Universität Hannover) they are contributing to the aim to build a nation-wide network of UWB expertise able to reach out for international cooperation.

In particular, Prof. Fettweis is involved in the "60 GHz UWB transmission with blind and semi-blind channel estimation affected by low ADC resolution and imperfect synchronization" project which is devoted to short-range ultra-wideband communication links. To address the challenging channel conditions the performance of blind and semi-blind channel estimation techniques coupled to iterative soft receiver processing is investigated. A topic that will be addressed specifically is channel estimation by exploiting of the already available redundancy introduced by channel codes.

"UWB for Wireless Sensor Networks: Cross-Layer Optimization" (UWB4WSN) is the project Prof. Jorswieck is involved in. In direct cooperation with Prof. Boche the team is developing generic tools for the joint optimization of the data acquisition and data communication entity with respect to suitable performance and distortion measures. With methods of sampling theory, the class of physical processes and signal processing operators are characterized which allow a stable reconstruction of

the parameters of interest taking into account quantization and communication errors. With methods of information and communication theory, the limits of coherent and non-coherent single- and multi-user transmission are studied. The analysis is performed with respect to various performance measures, such as higher-order statistics, zero-error capacity, wideband slope, minimum energy per bit, bit error rate, and (minimum) mean square error.

Technology access

On industry-side there are already contacts from the CRC to chip and server manufacturers which will be used to ensure technology access and feedback about the research approach. As mentioned before and described in more detail in project descriptions A01, A06 and A07 the cooperation with IHP will provide access to the needed BiCMOS technology during at least the first project phase. For later phases we consider it as an interesting option to cooperate with Globalfoundries which already has technologies with gate length of 28nm and below available. To this end, discussions with Globalfoundries Dresden have recently been started about the basic idea of the CRC and the need for demonstrators in later project phases. Globalfoundries is basically interested and mutual negotiations have been entered on how to get low cost wafer runs (or, possibly, even free access to them).

Strategic Advisors

IBM (Prof. Lehner and Prof. Fettweis) and AMD (Prof. Fettweis and Prof. Härtig, OS research center Dresden) have been contacted already at higher levels of their management to convey the general idea of energy-efficient servers and have expressed interest in the CRC. The cooperation will be formalized by AMD and IBM becoming Strategic Advisors of the CRC, see Chapter 4.

IBM, Böblingen. As a world leading IT corporation, IBM can supply the CRC HAEC with valuable feedback. To ensure that the boundary conditions of large server systems are understood by the CRC, it is of utmost importance to be guided by input from a world leading company in this field, as IBM.

TU Dresden is currently in negotiations with IBM Research & Development to set up an agreement to establish a review/an advisory process by conducting a review meeting twice a year with TU Dresden. To maximize the value of discussions, these review meetings will be held exclusively, without any other industry participants. If of higher value, as an exception, this review meeting can also be held at an IBM site in Böblingen or in Zurich.

It is intended to set up these review meetings for a three year period initially. After three years IBM and the CRC will review the value of this cooperation. Depending on this assessment the cooperation between the CRC and IBM might be extended into a development project cooperation. Since the CRC intends to add a transfer project within Phase III, the collaboration with IBM might become a perfect candidate for this.

Advanced Micro Devices GmbH (AMD). As a world leading corporation in delivering microprocessor products, in particular for high-performance and low-power server hardware, AMD can supply the CRC HAEC with extremely valuable feedback. To ensure that the boundary conditions of large server systems are understood by the CRC, it is of utmost importance to be guided by input from a world leading company in this field, as AMD. Since AMD sees high value in the research plans of the CRC, the company has agreed to establish a review/an advisory process by conducting a review meeting every half year at TU Dresden. To maximize the value of discussions by being open to analyze strategic and confidential input from AMD, these review meetings will be held exclusively, without any other industry participant, and the information being discussed will be under a non-disclosure

agreement. If of higher value, as an exceptional case, this review meeting can also be held at the AMD site in Dresden or in Austin, Texas.

AMD has committed to these review meetings for a three year period initially. After three years AMD and the CRC will review the value of this cooperation to decide how to take it further. The intention is to grow the cooperation between the CRC and AMD into a more comprehensive collaboration during this period so that possible additional concrete project cooperation might be initiated after the initial three year period (Phase I). Since the CRC intends to add a transfer project within Phase III, AMD is seen as a perfect partner to deepen the collaboration in that context.

As a person of contact AMD has named Chris Schläger and his deputy is Michael Hohmuth. Additionally, AMD has agreed to send a representative for the meeting with the reviewers of the CRC on Jan 13 2011, to be able to respond to questions.

1.3 Structural integration and impact at the host university

1.3.1 Staff situation

The CRC is a collaboration of researchers of the departments of Computer Science, Electrical Engineering and Information Technology and Natural Sciences, whose research interests and foci optimally complement one another for this project. The applicants' average age is just 47 years, indicating that the CRC in its current format can be sustained over the full project duration. This ensures a consistent research environment and allows the ongoing, long-term consideration of the research challenges encountered herein. Prof. Härtig (project B04) and Prof. Wolter (project A07) pass the normal retirement age during the third stage of the project. However, for such scenario, TU Dresden introduced the institution of senior professorship, which means that they would be potentially available over the whole course of the project.

Furthermore, recent term extension negotiations with four participating professors (Baader, Lehner, Nagel, Plettemeier) have been completed successfully, which is a strong argument for the scientific quality of the applicants and for the stability of the CRC project. Additionally, it shall be noted that young researchers have taken the project lead in a number of projects. In particular, this includes projects A04 (Dr. Müller), A08 (Dr. Franz) and B06 (Dr. Dargie). This fosters the sustainability of this CRC project's research foci.

With its current range of professors and project leaders, this CRC has a solid technical foundation. However, a few small subject-specific gaps still exist, which will have to be addressed in the short term. Specifically, project group B of the CRC could benefit from a specialist for processor design, who currently cannot be found within TU Dresden. For this reason, the department of Computer Science and the department of Electrical Engineering and Information Technology have decided to introduce a *new W3 professorship for processor design* to support this CRC. We believe that such an expert would be an ideal partner for a wide range of projects within this CRC. This professorship would embed perfectly in the AMD and IBM cooperation aimed to be established within this project. Both already showed strong interest in becoming partners of the project, cf. Section 1.2.5. Beyond the research scope of this project, the new professorship would also be an ideal nucleus for cooperation, especially for Prof. Ellinger, Prof. Wolter, Prof. Fettweis, Prof. Hochberger, Prof. Spallek, Prof. Härtig, Prof. Nagel, Prof. Lehner, Prof. Urbas and Prof. Schüffny.

During the first project phase, we further intend to implement a *new W1 professorship for Photonics* in a *joint lab with IHP* (Innovations for High-Performance Microelectronics). The department of Electrical Engineering and Information Technology of TU Dresden already enjoys an established cooperation with IHP GmbH in the field of RF and mm-wave circuit design. Within this context, the initiation of joint research efforts is being considered in the field of SiGe photonics, with the goal

of enabling the integration of SiGe LED and LASER devices into silicon technologies. The crucial advantage of the approach is the higher level of monolithic integration with the rest of the electronic circuitry, which allows eliminating the packaged interface between III/V optical devices and silicon integrated circuits. Both parties are committed to invest into the cooperation: a new research group is planned at IHP lead by an experienced researcher, which will be considered as head of a TU Dresden chair focused on SiGe photonics. The negotiations on this matter are already in progress. In terms of collaborations within the faculty as a whole, the new W1 professorship would be a perfect partner for Prof. Wolter, Prof. Ellinger, Prof. Lakner, Prof. Lehnert, Prof. Schröter, Prof. Czarske, Prof. Leo and Prof. Eng as well as with the newly founded Fraunhofer IZM – ASSID ("All Silicon System Integration Dresden"). On the industry side, there will be a close cooperation with Globalfoundries, AMD, X-Fab, MPD and RHe Microsystems.

Additionally, we intend to invite guest researchers (senior associates, scientific mentors and PhD students of high potential) throughout the whole project, in order for them to support us with their expert knowledge and to help us tackle individual research aspects. A list of possible candidates for this purpose is found in the description of the central project Z01.

1.3.2 Research infrastructure

Technikum Nöthnitzer Straße

The research at the Electronic Packaging Laboratory (IAVT) is based on the fundamental technologies for printed circuit boards and flat modules as well as thick/thin film technology, for which extensive technological and diagnostic equipment is available at around 1 200 m^2 lab area. Presently these labs are distributed in several buildings of TU Dresden and other rented locations. In order to centralize the research infrastructure into one interdisciplinary laboratory facility a concept for new technology building named "Technikum Nöthnitzer Straße" was submitted. This project is a joint project of Electronic Packaging Laboratory together with the Center of Microtechnical Manufacturing (ZμP), the Solid-State Electronics Laboratory (IFE) and the Chair for Polymeric Microsystems (Heisenberg-Professur Polymere Mikrosysteme). The new technology facility (planned for 2013) with 2 268 m^2 total area was granted from EU (EFRE) and will combine labs with cleanroom class ISO 6, 7 and 8. The new technology building with excellent labor conditions (clean room environment, low vibration and constant temperature) enables efficient and target-aimed realization of planned tasks (project A07). Thus this new infrastructure enhances the prospect of success for achieving of targeted results. The IAVT is also co-founder of the Competence Center for High-resolution Nondestructive Testing (nanoeva) where it jointly with Fraunhofer Institute for Non-destructive Testing (IZFP) accesses methods for the non-destructive testing in the volume with the high resolution. Access to following characterization techniques and equipment is available – microscopy techniques for surface characterization (AFM, AFAM, FIB, OCT, SEAM), acoustic techniques (Scanning Acoustic Microscopy) and radiation techniques (X-ray CT/Laminography/Digital Radiography, Acoustic Thermography).

High-performance computing and "Lehmann-Zentrum"

The Center for Information Services and High Performance Computing (ZIH) is a central scientific unit of TU Dresden, see project A04. It not only provides the computing infrastructure but also performs research in the design and development of efficient HPC applications jointly with application scientists. ZIH is active in the national (Gauß Allianz) and international HPC community with research and tool development. Researchers from the university can access two high-performance computing systems at ZIH with a combined total of more than 4 500 CPU cores. These HPC systems were installed in 2005/07, while a proposal for new hardware is currently in progress. With

the focus on data-intensive computing, the proposed system will combine the computing power of about 50 000 cores with a novel flexible filesystem infrastructure which can be tailored dynamically according to the user's need. This new HPC systems and ZIH will be part of the newly founded "Lehmann-Zentrum". In a new building (planned for 2013), together with the partners from the Center for Advanced Modeling and Simulation, the Center of Virtual Engineering, the Center "EveryWare" and the Media Center, this new scientific unit of the university will address IT-related research and development.

The productivity of the collaborations within this CRC will benefit from the immediate vicinity of Technikum, "Lehmann-Zentrum" and the departments of Electrical Engineering and Information Technology and of Computer Science.

1.3.3 Data management

The ZIH is currently building up an archival system for research data. The archive will be open to all members of the university and thus for any research activity that is carried out there. Starting with a version based on the IBM Tivoli Storage Manager the long time archive will later integrate a repository system (currently systems like Fedora Commons and dSpace are evaluated) allowing the storage of meta data (Dublin Core standard) and the management of access permissions. ZIH will provide support to the project groups of this CRC to preserve their data sustainably and to allow access to the data for future usage.

New data infrastructure (proposal 06/2010, Saxon State Ministry for Science and the Arts) will go beyond the existing systems. Centralized redundant data servers at two different locations with backup and archive systems will provide state of the art data integrity for the whole university. Key components for each location are:

- a NAS disk system with > 400 TB;
- a tape library with 2 PB, 10 tape drives, 64 TB disk cache, 9 TB database;
- 6 data servers (64 GiB RAM, 12 cores).

An additional HPC system with 1 920 cores with a fast connection to this storage system will be installed for data analysis and processing.

1.3.4 Gender equality

The teaching profile of TU Dresden in general shows that 53% of all graduates are women. In the scientific profile, i.e. in the profile concerning doctoral graduates, the percentage is below 40%. The percentage of women that habilitate is stable around 20%. Women occupy 14% of the W2/C3 professorships and 7% of the W3/C4 professorships. Compared to other universities in Germany this situation still offers room for improvement. To make progress on this the management of the university has set up a Gender Equality department and the senate was extended by a committee for "Equality and Diversity Management" headed by Prof. Ursula Schaefer who is at the same time Rector for Academic Affairs. The university aims at raising the levels of female doctoral graduates to 50% by 2014, the level of female habilitations to 30% by 2015 and the level of professorships to 15% by 2020. Integral elements of this plan are a particular financial support of talented female students directly in the individual departments.

Furthermore, the tasteMINT program draws the attention of school-leavers to the fields of Mathematics, Informatics, Natural Sciences and Technology. Other projects worth mentioning in context of MINT are the MINToring program and the Femtec.Network. Furthermore, the FINA project ("Frauen in Ingenieur- und Naturwissenschaften") was established to aim at increasing the focus of girls and young women to MINT fields already in pre-school and school. The general "mentoring-program" es-

tablished for offer a mentor-like guidance to interested students has also a particular focus on gender equality.

The table below illustrates the situation for the three departments that are involved in HAEC and shows that the current percentage of women should be target of improvement[7].

Natural Sciences and Mathematics	Total	Female (total)	Female (%)
Students	4 827	2 462	51
Scientists	604	246	40.7
PhDs	153	65	42.5
Habilitations	6	1	16.7
Professors	93	4	4.3

Computer Science	Total	Female (total)	Female (%)
Students	1 845	344	18.6
Scientists	194	30	15.5
PhDs	27	5	18.5
Habilitations	1	0	0
Professors	21	1	4.8

Electrical Engineering and Information Technology	Total	Female (total)	Female (%)
Students	2 158	201	9.3
Scientists	313	42	13.4
PhDs	32	2	6.3
Habilitations	2	1	50
Professors	27	1	3.7

In our current configuration we have 17 PI members, of which two are female, and 43 staff members, of which five members are female (including one non-scientific staff member). So, both on PI and overall level the CRC has 12% female members which is comparable to the overall number for PhD level, but three (four) times more than on professor level. We consider this as good starting point, but we support the goals of the university and plan to contribute own activities within HAEC, see project Z01.

1.3.5 Compatibility of family and scientific career

One of the goals of the CRC is to create an environment which enables the parents among its employees to conduct their research on the highest international level despite their additional family responsibilities. Dresden proves to be a particularly well-suited location for this objective. The available child care options in Dresden are much better than those of most university towns in the old federal states. This is especially true for the number of available places in kindergartens for children from the age of 3 as well as nursery places for children under age 3, for the hours of these institutions

[7] The values in the table are for the winter semester 2009/2010 (valuation date: December 1, 2009) and are taken from a preprint of the statistical report 2009 created by Directorate 3 for Development, Planning and Controlling. The table shows the total number of students, scientific assistants and professors. In the rows for PhDs and habilitations, the total number of dissertations and habilitations that have been completed in 2009 have been recorded.

and for the moderate fees. In total, in January 2010 there has been 289 daycare centers located in Dresden funded by the city or private investment. Two of them with a total number of approximately 250 places are managed by the Studentenwerk Dresden (student services organization). These provide full-time and part-time child care facilities for infants (6 months and older) of students, but there is also the possibility to register the children of members of the TU Dresden. The table below shows a selection of daycare facilities for children (KiTa) which are located in the surroundings of TU Dresden.

Additional support for students and collaborators of TU Dresden with children is provided by the "Campusnest" in form of short-term care. The joint initiative "Uni mit Kind" of the student services organization and TU Dresden has several offers (advisory service, special courses, etc.) for pregnant women and parents. On the basis of these and other activities for family-friendly conditions and gender equality, the TU Dresden received the certificate "familiengerechte Hochschule" first in 2007 and after a successful re-audit in 2010.

The Dresden International School (DIS) provides care for children between age 3 and 6 in the pre-school field and offers courses for grades 1 through 12 for school children with the curriculum being defined by the International Baccalaureate Organization. The 12th grade is concluded with the IB Diploma. English is the primary instructional language with German as the main second language. The DIS is thus highly attractive both for foreign researchers and also, of course, for German scientists planning to go abroad with their families for a longer period at some point in their career.

Based on this excellent situation the CRC will implement own measures to improve the situation for its members depending on their individual conditions, see project Z01.

Daycare facility	Total capacity	Capacity for children in the age of	
		0–3 years	3–6 years
KiTa of Studentenwerk Dresden	160	108	52
KiTa Beutlerpark of Studentenwerk Dresden	18	18	0
KiTa Fridolin	79	28	51
KiTa Villa Parkhaus	88	44	44
KiTa Biopolis[8]	25	13	12

1.3.6 Young researchers

The CRC will promote young researchers at different levels of their carrier. Master and Diploma students will be employed as student researchers, mainly for providing assistance for implementation work and experimental studies. However, the student researchers will get insights in the scientific goals of the CRC and might be interested in writing a doctoral thesis in the direction of HAEC. PhD students will be employed by the projects and get the opportunity to write their doctoral thesis on a topic related to the research carried out within their project. More senior research staff (PostDocs) will get the opportunity to gain experience in leading (part of) a project.

In June 2010, the three involved departments had the following number of students registered:

Department	Students	PhD students
Electrical Engineering and Information Technology	2 047	234
Computer Science	1 671	93
Natural Sciences and Mathematics	4 522	846

[8] Joint facility of the city of Dresden, TU Dresden and MPI-CBG, opened 2009 with a planned total capacity for 45 children in the age of 0–3 years and 45 children in the age of 3–6 years.

Approximately eight percent of the students usually stay at the university for a PhD. These students as well as graduate students from other universities (in Germany, but also in other countries) are the source of the prospective research associates. Local students can be assessed by first employing them as student researchers. Foreign applicants for positions will first be evaluated on the basis of their CVs, transcripts of records and reference letters. The best candidates are then invited for a presentation (usually on their master thesis) and subsequent discussion with at least two of the professors participating in the CRC. Arrangements for advancements of PhD students/research associates PhD students hired by the CRC will be integrated both in the research group of the supervising professor (to have access to the specific knowledge in this group) and in the CRC (to further collaboration and interdisciplinary). This second goal is achieved by:

1. offering specialized and advanced technical lectures for the members of the CRC – in particular, the professors will organize a joint lecture ("Ringvorlesung") on topics relevant for the CRC;
2. joint supervision of PhD students by two professors involved in the CRC;
3. offering courses that teach skills like scientific writing, preparation of scientific talks, time management, reviewing of scientific papers, etc.;
4. a joint research seminar, where guests, participating professors, Post-Doc and PhD students give talks related to the topic of the CRC;
5. scientific mentors, see project Z01;
6. workshops organized every two years, where also external experts are invited in order to get their feedback.

Early publication of research results (in international conferences and prestigious journals) will be ingrained in the culture of the CRC. During Phase I of the CRC an Integrated Research Training Group shall be prepared to start in Phase II.

Impact on teaching

In addition to the joint lecture ("Ringvorlesung") and the research seminar organized by the CRC, the topics of the CRC will also be integrated in existing lectures or newly designed ones. For example, Prof. Schill regularly offers the lecture "Multi-media Communication", in which aspects of one of our application domains (content distribution) are treated and where adaptation plays an important role. As it is, this lecture will already be of potential interest for some of the PhD students in the CRC, but it shall also be updated to integrate aspects of energy efficiency later on. Finally, several HAEC PIs will contribute to the new planned DIGS-E3 graduate program EEComp and this program will also be open for the CRC's PhD students, cf. Section 1.2.4.

1.3.7 Knowledge transfer and public relations

Knowledge transfer

The TU Dresden demonstrates excellence in research transfer, as proven by the first position by far in patent filing among German universities and a remarkable number of spin-offs. It acquired the highest amount of BMBF funding in 2009, and is one of the top university players in attaining EU funding in 2010. This is facilitated by several instruments such as its patent office, its industry partner programs, its involvement in regional networks and transfer structures.

Transfer structures. TU Dresden has established a successful system of different instruments to foster knowledge and technology transfer. One basic instrument, which already exists for several years, is the so-called Patent Office, which helps in filing inventions as patents and the supporting "Patentinformationszentrum". Furthermore, it maintains a commercial arm for professional project contracting

and project management, the GWT-TUD GmbH. Via this company, professors can perform transfer activities. TU Dresden also hosts Dresden Exists (Prof. Schefzcyk), one of the most successful organizations for helping TU Dresden members to start up companies. Dresden Exists actively maintains links to the "Technologie-Gründerfond Sachsen" [9]. In order to increase the conversion rate of intenders to real entrepreneurs the "HighTech Startbahn" project, a new professional catalyst, was initiated by TU Dresden in 2010. It will offer new start-ups a network, infrastructure and operational help, as well as fund raising access.

Patents and open-source software. It is envisaged that many of the innovations of the CRC can be patented, not only for hardware-, but also for software-related topics. These patents will play a major role in knowledge transfer and create industrial attraction for the CRC. To this end, the CRC will collaborate with the patent office of TU Dresden. Other software-related results, in particular standalone development tools for the HAEC software, can be distributed as open source software, depending on the strategic decisions of the groups. If possible, the HAEC software system itself shall be transferred in Phase III to a company for commercialization. If this is not possible, it will be released under a dual-license model or as open source.

Industry partner programs and networks. For close industry involvement, TU Dresden offers platforms for sponsorship and collaboration. Currently active are the Industry Partner Program (IPP) within the department of Electrical Engineering and Information Technology and the OUTPUT program of the department of Computer Science. These programs reach out to regional networks, but also to companies all over Germany. TU Dresden also maintains an active alumni network reaching out into industry.

Regional networks Silicon Saxony and Software Saxony. Several partners of the CRC have strong relationships to Silicon Saxony [10], the network of chip manufacturers and research institutes in Saxony. This network has an annual meeting, the Silicon Saxony day, where results can be demonstrated, either by exhibition or presentation.

Software Saxony and OUTPUT program. Prof. Aßmann and Prof. Schill are members of the software subnetwork of Silicon Saxony, Software Saxony, founded in 2006, with over 50 members, mostly companies. Results of the CRC can be disseminated via the bi-yearly meetings and yearly Innovation Forum of Software Saxony. This day usually takes place in spring and is attended by 300–500 visitors [11]. In 2010, the Innovation Forum featured the tracks "Embedded Software", "Web and Business Software", "Factory Automation Software", "Visualistics" and "CoolSilicon", with additional student exhibition tracks [12]. Additional tracks can be allocated, also for the CRC. The day is organized by the OUTPUT program of the department of Computer Science, a program for networking with industrial partners, also in 2010–2011 supported by the transfer project Output4Business of BMI.

Transfer network Open4Innovation. Open4Innovation is a new ESF project, funded by Sächsische Aufbaubank, steered by Prof. Aßmann, to build long-lasting transfer structures for IT in Saxony. From 2011–2013, so-called "innovation cycles" will be initiated among members of Software Saxony, which

[9] http://www.TGFS.de
[10] http://www.silicon-saxony.net
[11] http://www.software-saxony.de/?tag=innovationsforum
[12] http://output.inf.tu-dresden.de

will collaborate for establishing tailored innovation processes for group innovation and open innovation. Though Open4Innovation ends within Phase I of the CRC, it can be used to prepare structures for knowledge transfer to Saxonian companies.

CoolSilicon. Several PIs of the CRC (Profs. Fettweis (initiator), Ellinger (Leader Area Management Board 2), Plettemeier, Jorswieck, Aßmann, Nagel, Wolter, Schröter) are part of the BMBF Cluster of Excellence CoolSilicon, which is a huge project cluster (40 million Euros funding, 2009–2013) with more than 60 partners in the region of Saxony. Results of the CRC will be disseminated at the annual meetings of the CoolSilicon cluster and through existing and future collaborative application-oriented projects within this cluster. Furthermore, the network provided by CoolSilicon, organized as a permanent association (e.V.), initially coordinated by Prof. Fettweis and now by Prof. Mikolajick, forms a basis for approaching new transfer projects.

Object Management Group (OMG). Prof. Aßmann's group is member of the OMG and follows its standardization activities. For real-time software, already UML Profiles have been standardized (MARTE). We will watch the activities about energy-related standards to identify related requests for proposals (RFP).

Public relations and press

Scientific publications. The CRC will publish its results at renounced scientific conferences and journals. At the moment, many conferences take up the topic of energy-efficient management of software and systems, but there are also the first dedicated conferences, such as Green IT.

Deutschlandfunk. Deutschlandfunk has a rather excellent program on IT-related research and innovation (The Computer Club). It regularly emits reports, e.g. from the Dagstuhl computer science meeting center. The CRC will attempt to use this dissemination channel.

Dresden Future Forum. Every second year, T-Systems Multimedia Solutions organizes a Dresden Future Forum for its customers, to make them aware of future trends in web engineering and related fields. The last two events (held in 2008 and 2010) were moderated by the professional moderator Ranga Yogeshwar. Since T-Systems Multimedia Solutions is a member of Software Saxony, conducts several projects with the computer science group of the CRC and is interested in energy-efficient servers, e.g. for video on demand, the Dresden Future Forum can probably be used as national dissemination channel.

The CRC will disseminate events via the press office of TU Dresden. The CRC will actively maintain a web site and a blog, to keep interested readers up-to-date.

How to attract companies for the CRC

Transfer projects. The CRC plans "transfer projects" for Phase III and envisages knowledge transfer in Phases I and II by dissemination events, hardware and software patents, as well as further common research projects.

Further research projects will attract companies for collaboration with the CRC. Energy efficiency is one of the key topics in the EU IST work program 2011/12, probably also in the subsequent years. In many calls, ideas on tools, methods, architectures for energy-efficient management of servers, embedded systems, cars, homes are searched for. This brings the members of the CRC in a pole position

to acquire more research projects on the European level and broaden the results of HAEC to other domains, for instance aerial or automotive engineering. Similar considerations hold for the national level, for example, because energy-efficient cars form a central research objective of the national German government.

CeBit. Several partners of the CRC regularly exhibit at CeBit, mainly on the booth of TU Dresden (Prof. Aßmann, Prof. Lehner, Prof. Nagel). In Phase II, results of the CRC will be exhibited to attract companies for transfer projects in Phase III.

Conferences. CRC results will be presented at leading scientific and industrial electrical engineering and computer science conferences in Germany, Europe and world-wide. Conferences that will be targeted to have an own CRC booth include DATE (Design, Automation & Test in Europe; held in Dresden in 2010) and ISC (International Super Computing; which took place in Dresden in 2008 and is now hosted in Hamburg).

TechniSat. Dresden hosts the main development department of TechniSat with more than 300 employees. While TechniSat is a producer of consumer devices, it has interest in energy-efficient applications on standalone consumer devices, e.g. TV set top boxes, game boys. Energy-efficient video-on-demand servers might become important for their business in the future. The CRC intends to take up contacts at the Dresden department of TechniSat to transfer knowledge and prepare transfer projects.

RHe Microsystems. Innovative solutions in micro systems, substrate manufacturing and packaging are the core competencies of RHe Microsystems. The Company belongs to the Cicor group and is located on the periphery of Dresden. RHe has strong interest in development and production of sophisticated chip packages containing adaptively steerable antenna systems. Transfer projects and knowledge transfer are intended within the CRC.

Start-up companies. Several principal investigators have been involved in founding start-up companies: Prof. Fettweis – Systemonic AG (today NXP Semiconductors Germany GmbH), Radioplan GmbH (today Actix Ltd.), Signalion GmbH, In-Circuit GmbH, Dresden Silicon GmbH (today Signalion GmbH), Freedelity GmbH, RadioOpt GmbH, Blue Wonder Communications GmbH, InRadios GmbH; Prof. Schill – www.vidsoft.com; Prof. Schröter – www.xmodtech.com. Others have been mentors of BMWi-funded EXIST programs, e.g. Prof. Aßmann – www.mentalmotive.com, www.ubigrate.de. This expertise will be used, if appropriate, to found new start-up companies for HAEC technologies.

Strategic advisors. Apart from existing networks to industry a special collaboration will be established with strategic industry partners to convey the general idea of energy-efficient servers. This collaboration will be formalized by the "Strategic Advisors", cf. Chapter 4 and Section 1.2.5.