A Tunable Delay Cell with Digital Control
in a 45nm PD-SOI CMOS process

Essentially every circuit will present a delay from its input to output, which is called latency. Usually this delay is not easily controllable and also it is not fixed over very wide frequency ranges. There are several structures commonly used to add the possibility of delay tuning. One can mention an inverter chain with tunable capacitive load, current starved inverter, and vector modulator circuits. The first question to answer is the range of the generated delay. For example, in Fig. 1 from reference [1], it is possible to tune the delay in a range of 280 ps. The second question is how precise the controlling of the delay can be. Referring to the same figure, can we assure a delay of 254.1 ps? It is generally possible to use a Digital-To-Analog Converter (DAC) and digitally provide the controlling voltage. However, the higher the precision, the higher the number of bits of the DAC, and the bigger the area will be.

![Fig. 1. Shunt capacitor delay element a) scheme and b) typical characteristic delay in term of control voltage](image)

In this work (MA/DA) you will be responsible to analyze, design, and implement a low power tunable delay cell with a range of several (10 - 30 ps) and medium resolution (3-5 bit DAC). You are expected to compare different approaches, choose the most suitable one based on the specified criteria, carefully design it, and implement it. Your design is to be compared with the simulator results as well. The DAC implementation would also be in your responsibility. The used technology is a 45nm partially depleted SOI CMOS process.

For further reading please see below:

[1] [http://es.elfak.ni.ac.rs/Papers/Jovanovic-Stojcev_LinearCurrentStarvedDelayElement.pdf](http://es.elfak.ni.ac.rs/Papers/Jovanovic-Stojcev_LinearCurrentStarvedDelayElement.pdf)