A High Precision Transimpedance Amplifier with Offset Compensation in a 45nm PD-SOI CMOS process

For a very good current-steering Digital-To-Analog Converter (CS-DAC), many current sources have to be almost perfectly matched. To match several currents with a very high precision, employing a current mirror is normally not sufficient. Mismatch is typically the most severe error mechanism behind small differences in those current sources. To solve the issue, one way is to use a reference current and periodically compare other current sources with the reference. In case they are not matched to the required precision, a low-speed current DAC would be adjusted to ensure the matching. The comparison of two currents requires a differential transimpedance amplifier (TIA). To ensure that the amplifier is not adding additional error to the measurement of the input currents, its mismatch – which is normally present in the shape of offset – has to be canceled out.

Your task (MA/DA) is to study and compare different approaches to implement a TIA. Your work comprises the complexity of an offset compensation procedure and the possibility of implementation in an advanced CMOS node. The chosen circuit has to provide enough precision to compare two currents in a range of micro Amps. The chosen architecture has to be designed and simulated in the frequency and time domain. Large and small signal simulations have to be carried out. The offset compensation circuit has to be designed and stability measures have to be checked. Finally, the design parameters are to be compared with the simulation results.