Geometry scalable compact modeling of GaAs HBTs

Tobias Nardmann[3], Plamen Kolev[2], Nick Tao[4], Michael Schröter[1*]
[1]Chair for Electron Devices and Integrated Circuits (CEDIC), TU Dresden, 01062 Germany
[2]Qualcomm Technologies, San Diego, 92121, USA, [3]formerly with CEDIC (now with Infineon Technologies, Dresden, Germany), [4]formerly with Qualcomm Technologies, San Diego, 92121, USA
*Corresponding author: mschroter@ieee.org

***Abstract* - A set of test structures consisting of HBTs with different sizes and contact layouts as well as TLM structures for determining series resistances was fabricated in a GaAs HBT technology. Based on these structures, a fully scalable parameter set for the compact model HICUM was extracted that accurately describes the transistor behavior in a large range of bias and temperature conditions relevant for practical applications.**

Index Terms - Compact modeling, GaAs HBTs, HICUM, geometry scalable compact models

I Introduction

Despite continuing advances in various transistor technologies, GaAs HBTs continue to be important for realizing certain applications, especially cell phone power amplifiers. With the push towards higher integration, the need for physics-based, scalable transistor models has been recognized and some earlier attempts have shown promise [1]. However, these models are still not commonly available for III-V HBTs in general and GaAs HBTs in particular [2]. Compared to InP HBTs, for which geometry scaling has already been demonstrated [3], GaAs HBT technology is more mature and yields quite repeatable characteristics. Moreover, the relevant physical effects are well enough understood for scalable models to not only be possible, but well worth the time investment for parameter extraction. The latter is especially true when compared to the effort necessary for creating individual simple compact or table-based models for a multitude of different device configurations. Furthermore, a geometry scalable physics-based model parameter set allows to naturally include process tolerances and thus statistical modeling of a (mature) process technology.

In existing process design kits (PDKs) III-V HBTs are often described using AHBT [4], which is a dedicated III-V model that attempts to include the negative differential mobility (NDM) effect explicitly through a semi-empirical formulation. Unfortunately, AHBT is available only in ADS, which is a significant drawback for many users and applications. It seems to be less known to the III-V HBT modeling community that modern standard compact models, although their development mainly focuses on SiGe HBTs, include most, if not all, necessary physical effects for successfully describing III-V and in particular GaAs HBTs. For instance, efforts for including the NDM effect in MEXTRAM [5] and also in HICUM [6, 7] have been made. Additionally, standardization of these models across the semiconductor industry has made these models widely available in all circuit simulators and allows for a more flexible PDK. Thus, there is an incentive to use such standard models also for GaAs HBTs. Since HICUM/L2 has been continuously developed and demonstrated to be suitable for a variety of high-speed HBT technologies (e.g. [3, 8, 9, 10]) it has been employed in this work for describing GaAs HBTs as well.

The goal of this paper is to demonstrate that, with a limited number of test structures and the application of commonly used extraction methods along with some relatively simple scaling equations, a fully scalable parameter set for HICUM can be obtained for a commercial GaAs HBT technology.

II Technology, Structures and Extraction Strategy

The transistors and test structures were designed by Qualcomm Technologies and manufactured in WIN Semiconductor's 3rd generation (C3) GaAs HBT technology [11] with (f_T, f_{max}) = (40, 110) GHz.

Transistors in CBEBC configuration and GSG pads for AC measurements were available for the sizes given in Table 1. In addition, two double-finger and two four-finger devices were produced and measured. A full measurement set, consisting of all data needed for extraction, was obtained only for the single finger reference device with a drawn emitter area A_{Ed} = 3µm x 30µm. A reduced data set for extracting and verifying the device scaling was measured for all other HBTs. All measurement data for these devices were open-short-deembedded, with an individual open standard available for each transistor length, but for a constant reference width.

Table 1: Drawn emitter width (b_{Ed}) and length (l_{Ed}) dimensions available for measurement.

b_{Ed} / µm \ l_{Ed} / µm	5	10	20	30	45
2	x	x		x	x
2.5			x	x	
3	x	x	x	x	x
4			x	x	

Besides the transistors in GSG pads, DC test structures for determining the internal and external base sheet resistance as well as the collector sheet resistance (subcollector with and without BC mesa) were implemented and evaluated following the structures described in [12]. Finally, area- and perimeter-intensive junction structures were evaluated to facilitate an accurate separation of perimeter and area junction capacitance

and current components as well as of parasitic capacitances.

The extraction was performed in three major steps:

- Technology-specific parameters were determined first from special test structures and by applying special measurement conditions to HBTs. The results were used in the subsequent extraction steps for, e.g., determining the split of internal and external peripheral capacitances, the external collector resistance and the internal and external base resistance.
- Next, the parameters for the reference device (using initial results from geometry separation of all transistors for splitting diode currents) were extracted. The results of this step were used for all non-scalable parameters in the final step.
- Finally, the scaling parameters were determined from all available devices.

All results shown in this work correspond to model cards resulting from the third step, even though the second step produces a more precise model for the reference device since the scaling does not reproduce the best model for any one device due to process variations between transistors, especially those that were not all realized on the same die.

III Parameter Scaling

The drawn and effective (electrical) dimensions were nearly identical. For the GaAs HBTs considered here, simplified parameter scaling equations were implemented directly in an ADS model card rather than using an external program offering more sophisticated scaling formulations (e.g. [13]). As verified from the different transistor geometries, the mesa structure permits to omit some components of the standard model such as the substrate transistor components. Also, the BE injection current was found to be purely internal, while the recombination current was purely peripheral and no peripheral emitter junction capacitance was found.

For the investigated technology, 21 individual model parameters have been found to be dependent on geometry. Most scaling parameters, such as the perimeter-area separation, follow the expected trends seen also for other technologies (e.g., [3, 8, 14]). However, two exceptions should be highlighted here: the emitter resistance and the external base resistance.

The base resistance does not follow common geometry-scaling equations due to the particular combination of materials and layout. While a foreside via connection (cf. Fig. 1(a)) is well described in [15, 14], the presence of a contact resistance between the highly conductive base metal and the semiconductor impacts the current distribution and could not be modeled accurately enough with available equations. Thus, quasi-3D numerical simulations (e.g. [15, 14]) were used to determine the actual resistance. Subsequently, the geometry dependence was adjusted in several ways:

- Treating the foreside contact instead as a parallel base contact due to the highly conductive base metal.
- Adjusting the sheet and contact resistance to obtain a better agreement between the simulated and analytical results.
- Adjusting the results from the existing foreside equations by using a constant multiplier.

A comparison between device simulations and several analytical approximations is shown in Fig. 1(b). It was found that the equations in [14] multiplied by a constant is a reasonable approximation. A more accurate physics-based formulation is currently under investigation. Adjusting the contact resistance is similarly accurate.

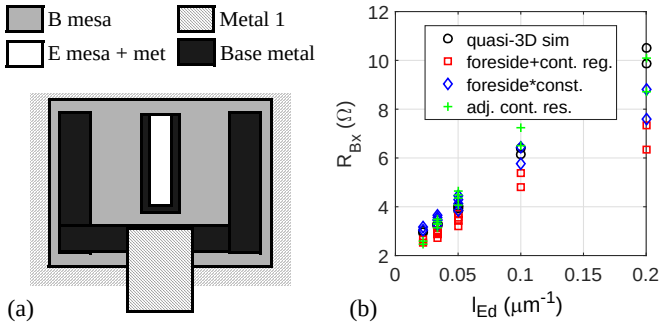

Fig. 1: (a) Sketch of the base contact and access layout. (b) Comparison of simulated base resistance with various analytical approximations.

The second atypically scaling parameter is the emitter resistance R_E. It is typically modeled as

$$R_E = R_{E0} + \frac{\rho_{EA}}{A_{Ed}} \tag{1}$$

with the model constants R_{E0} and ρ_{EA}. Inserting the drawn emitter dimensions for the emitter area A_{Ed} did not result in a good match with measured data. TEM pictures of multiple transistor geometries indicated that the M1-Emitter-interface was consistently narrower than the drawn emitter width and the emitter mesa beneath (cf. Fig. 2(a)). Consequently, (1) was reformulated as

$$R_E = R_{E0} + \frac{\rho_{EA}}{n_F \cdot l_{Ed} \cdot (b_{Ed} - \Delta b)} \tag{2}$$

with the width reduction Δb and n_F as finger number. A value of Δb = 0.7 µm was determined from both TEM pictures and nonlinear fitting of (2) to the data from all devices. Fig. 2(b) shows the results of fitting (1) and (2) to the available data.

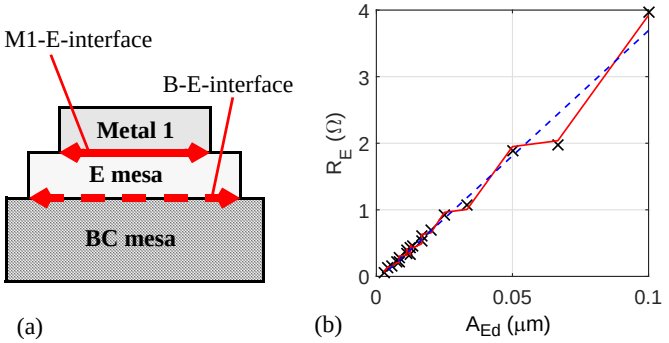

Fig. 2: (a) Sketch of metal 1, emitter mesa and base-collector mesa (not to scale), illustrating the interface width difference. (b) Extracted emitter resistance for each device (symbols) and scaling model with (solid line) and without (dashed line) Δb.

IV Model Comparison to Experimental Data

Below, measurement and model are compared for the most important characteristics, starting with the reference device and followed by an overview on scalability. For all comparisons the same process specific model parameter set was used. Notice that the measurement range was limited by thermal breakdown. In all figures, symbols represent measurements and lines model results.

A comparison of DC characteristics for various temperatures and voltages is shown in Fig. 3. Additionally, Fig. 3(b) shows the large error introduced by neglecting the thermal resistance when keeping V_{BE} constant.

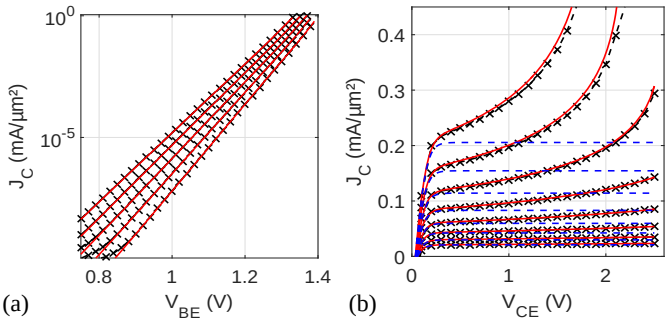

Fig. 3: Comparison between model and measurement for the reference device. (a) Collector current density for the reference device for T = [280, 300, 320, 340, 360] K at V_{BC} = 0 V. (b) Forward output characteristic with V_{BE} = 1.29... 1.36 V at T = 300 K. Dashed lines indicate results obtained with R_{th} = 0.

The comparisons of the transit frequency f_T and maximum oscillation frequency f_{max} for the reference device are showing in Fig. 4 quite good agreement even for a forward-biased BC diode, which is of interest for power amplifier and other large-signal applications.

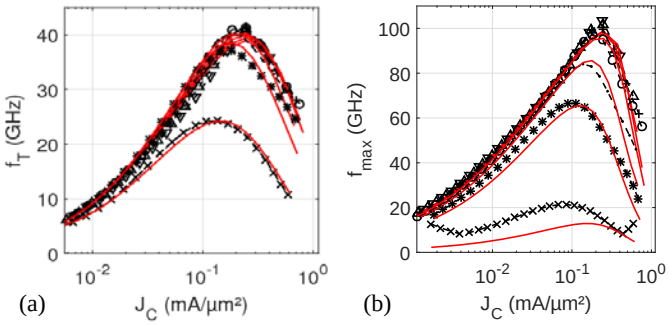

Fig. 4: Comparison of model (lines) and measurement (symbols): (a) f_T and (b) f_{max} for the reference device at T = 300 K, V_{BC} = [-0.75, -0.5, -0.25, 0, 0.5, 0.75, 1] V.

Fig. 5(a) demonstrates a possible impact of the NDM effect on f_{max}. Due to the nearly constant collector current, the main impact factors on the cut-off frequencies are self-heating, the change of the low-current transit time with V_{BC} and the NDM effect. The figure demonstrates that a large part of the f_{max} slope (and f_T, not shown) can already be modeled quite accurately through the two former effects, although a preliminary implementation of the NDM related collector transit time in HICUM following [6] leads to a slightly improved agreement in the forward active region at the cost of accuracy at lower CE voltages. Fig. 5(b) shows excellent agreement for the output characteristics up to current densities slightly beyond the cut-off frequency peak. The observed deviations are due to variations in I_B scaling.

Examples of model scalability are given in Fig. 6, showing I_C and f_T for devices with different emitter widths. The agreement for devices with different lengths is even better.

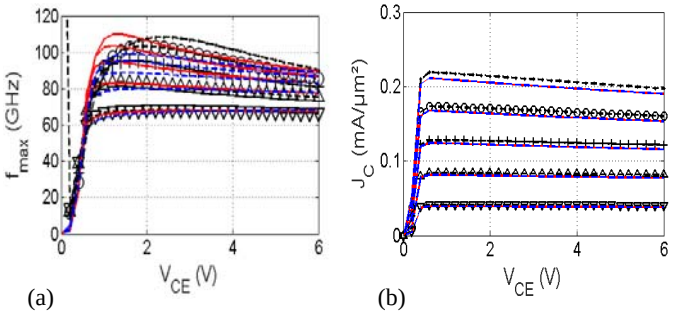

Fig. 5: (a) f_{max} and (b) J_C at constant I_B versus V_{CE} for T = 300 K. Red solid lines indicate model with NDM effect, blue dashed lines indicate optimized scaling model.

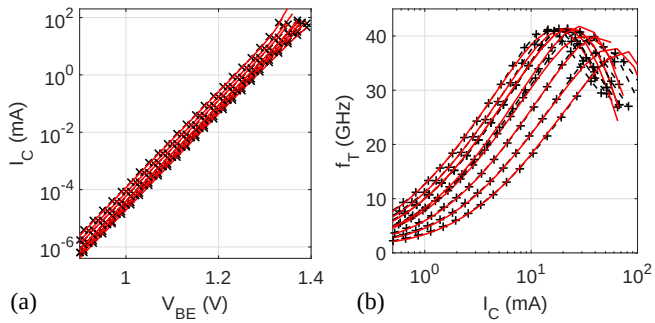

Fig. 6: (a) Collector current I_C and (b) transit frequency f_T extracted at f_0 = 5 GHz: comparison of model (lines) and measurement (symbols) for T = 300 K and different device sizes as given in Table 1 with l_{Ed} = 30 µm, N_F = 1...4.

Fig. 7 shows the S-Parameters at typical operating points for the largest available device using still the same process specific model parameters and scaling equations. Even for large devices with thermal variations between fingers, the model shows good agreement with the measurements, with the exception of deviations in S_{11} around 20 GHz, which has been observed only for multi-finger transistors and is attributed to a deembedding error, since open and short structures were available only for single-finger devices.

Using load-pull measurements, a verification of the model under large-signal conditions is given in Fig. 8. The HBT with A_{Ed} = 4 x 3µm x 20µm is from a different die than the devices used for parameter extraction. Excellent agreement is observed for the output power and power gain without adjusting the model parameters, thus demonstrating both the process stability and the applicability of the scalable model across the wafer. The difference of simulated to measured output power is below 0.36 dBm across the entire measurement range.

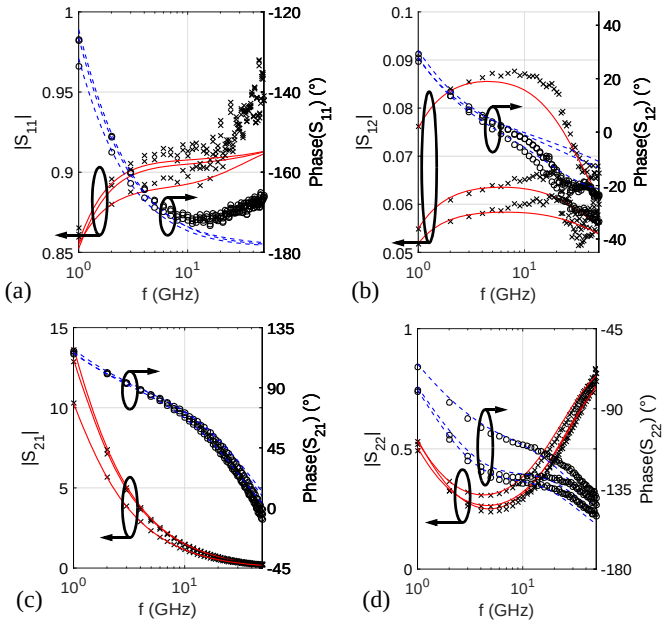

Fig. 7: S-Parameters for the device with A_{Ed} = 4 x 3µm x 30µm at T = 300 K, V_{BC} = [-0.5, 0, 0.75] V, and J_C corresponding to approximately the current density at $f_{T,peak}/2$.

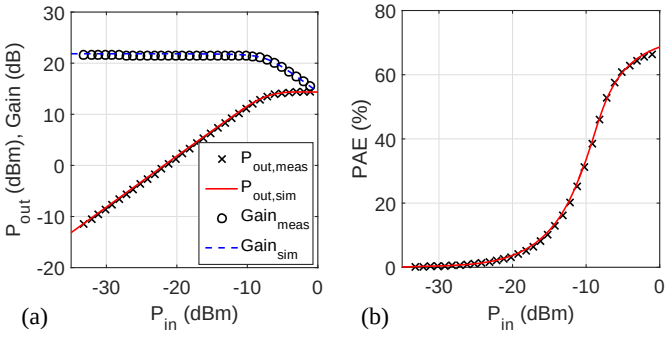

Fig. 8: (a) P_{out}, gain and (b) PAE as a function of input power at f_0 = 2.4 GHz, V_{CE} = 3.4 V, J_C = 50 µA/µm², T = 298 K, Z_l = (129.48+78.32j) Ω, Z_s = (15.84+8.34j) Ω, for a multi-finger transistor with A_{Ed} = 4 x 3µm x 20µm.

V Summary and Conclusions

GaAs HBTs with a range of different emitter widths, lengths and number of fingers have been described with the standard compact model HICUM/L2. Thanks to the fact that the process scales quite well, excellent agreement has been obtained over a wide range of geometries, bias and for temperatures between 280 and 360 K despite using simplified geometry-scaling equations and without including negative differential mobility (NDM) effects explicitly. Higher accuracy can be achieved with more detailed formulations for the NDM effect and more sophisticated scaling. Given these results, the following conclusions can be drawn:

- Commercially available GaAs HBT processes are sufficiently mature for using a fully geometry scalable modeling and parameter extraction approach as opposed to parameter fitting for a small set of individual devices.
- The test structures employed for SiGe HBT parameter extraction can also be used for GaAs HBT modeling.
- A standard compact model such as HICUM, which is available across all major circuit simulation platforms, is capable of providing a satisfactory agreement for circuit design purposes even without III-V material specific extensions.

VI Acknowledgments

The authors TN and MS would like to thank Qualcomm Technologies for funding this work, including wafer fabrication, and Wing Sy of Qualcomm Technologies for performing the load-pull measurements displayed in Fig. 8.

VII References

[1] Y. Zimmermann, P. Zampardi, M. Schröter, “Modeling and scaling of III-V HBTs using HICUM and TRADICA”, IEEE Top. Workshop on Power Amplifiers for Wireless Comm., San Diego 2003.

[2] P. J. Zampardi, “Silicon modelers are from Mars, GaAs modelers are from Venus”, IEEE BCTM, pp. 98-105, 2017.

[3] T. Nardmann, P. Sakalas, F. Chen, T. Rosenbaum, M. Schröter, “A geometry scalable approach to InP HBT compact modeling for mm-wave applications”, IEEE CSICS, paper W3.3, 2013.

[4] M. Iwamoto, D. Root, J. Scott, A. Cognata, P. Asbeck, B. Hughes, D. Avanzo, "Large-signal HBT model with improved collector transit time formulation for GaAs and InP technologies", IEEE MTT-Symp. Digest, pp. 635-638, 2003.

[5] R. van der Toorn, J. Paasschens, J. Dohmen, R. Pijper, N. Balm, “Compact Modeling of GaAs Heterojunction Bipolar Transistors using the new Mextram 3500 model”, IEEE BCTM, 4 pages, 2006.

[6] M. Schröter, T. Nardmann, G. Wedel, “A Closed-Form Solution for the Low-Current Collector Transit Time in Group IV and Group III-V HBTs”, IEEE Trans. Electron Dev., pp. 3346-3352, 2017.

[7] T. Nardmann, “Physics-based compact modeling and parameter extraction for InP heterojunction bipolar transistors with special emphasis on material-specific physical effects and geometry scaling“, PhD Thesis, Chair for Electron Devices and Integrated Circuits, TU Dresden, 2017.

[8] A.Pawlak, B. Heinemann, M. Schröter, “Physics-based modeling of SiGe HBTs with f_T of 450 GHz with HICUM Level 2”, IEEE BCTM, Miami (FL), pp. 134-137, 2017.

[9] P. Chevalier et al., "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications", Proc. of the IEEE, Vol. 105, No.6, pp. 1035-1050, 2017.

[10] M. Schröter et al., “SiGe HBT technology: Future trends and TCAD based roadmap”, Proc. of the IEEE, Vol. 105, No. 6, pp. 1068-1086, 2017.

[11] https://www.winfoundry.com/

[12] T. Nardmann, J.Krause, A. Pawlak, M. Schröter, “Determining the base resistance of InP HBTs: An evaluation of methods and structures”, Sol.-St. Electron, Vol. 123, pp. 68-77, 2016.

[13] M. Schröter, H. Rein, W. Rabe, R. Reimann, H. Wassener, A. Koldehoff, “Physics- and process-based bipolar transistor modeling for integrated circuit design”, IEEE J. of Sol.-St. Circ., Vol. 34, No. 8, pp. 1136-1149, 1999.

[14] M. Schröter and A. Chakravorty, *Compact hierarchical modeling of bipolar transistors with HICUM*, World Scientific, Singapore, 2010.

[15] M. Schröter, J. Krause, S. Lehmann, D. Celi, “Compact layout and bias dependent base resistance modeling for advanced SiGe HBTs”, IEEE Trans. Electron Devices, Vol. 55, No. 7, pp. 1693-1701, 2008.