Long-Term Large-Signal RF Reliability Characterization of SiGe HBTs Using a Passive Impedance Tuner System

Christoph Weimer[#$1], Eren Vardarli[#], Gerhard Fischer[*] and Michael Schröter[#$2]
[#]Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden, Dresden, Germany
[$]SemiMod GmbH, Dresden, Germany
[*]IHP, Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder), Germany
[1]christoph.weimer@tu-dresden.de, [2]michael.schroeter@tu-dresden.de

***Abstract* -- This paper contributes to the exploration of dynamic operating limits of SiGe HBTs. The bipolar transistor breakdown voltages BV_{CBO} and BV_{CEO} are experimentally determined and discussed. DC, small-signal and large-signal simulations are performed, demonstrating the HICUM/L2 model and extracted model parameters to be in good agreement with measurements far beyond BV_{CEO}. A long-term RF stress test is performed, proving SiGe HBTs to be extremely robust and reliably operable far beyond BV_{CEO} within the investigated stress test duration. Only extremely nonlinear large-signal RF operating conditions cause a degradation of RF parameters.**

***Index Terms* --- SiGe HBT, HICUM, RF reliability, load-pull.**

I Introduction & Motivation

The continuous improvement of the peak cut-off frequencies of modern high-speed Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs) is being achieved by increasing the collector doping which inherently decreases the statically defined transistor breakdown voltages [1, 2]. Breakdown voltage (BV) related constraints strongly affect radio-frequency (RF) circuits such as power amplifiers which require large output voltage swings to obtain high output power density. To experimentally explore the maximum permissible collector-emitter (CE) voltages, previous device-level SiGe HBT reliability studies have focused on direct-current (DC) stressing the devices under test (DUTs) [3]. Moreover, for characterizing device degradation, the research focus was on the static base current at low base-emitter (BE) voltages which is increased due to generation/recombination centers caused by high-energy charge carriers at the emitter-base spacer oxide [4, 5]. Whereas the investigation of the I_B increase at low V_{BE} and of the underlying physics is insightful from a device characterization point of view, it does not satisfactorily address reliability related concerns during RF circuit design: What is the maximum applicable voltage amplitude of transient $v_{CE}(t)$ swings in dynamic large-signal (LS) transistor operation? Which are the LS operating conditions that the transistor withstands without degrading? When does a degradation of RF-relevant transistor characteristics ($\underline{Y}$-parameters) occur (rather than just the DC I_B)? This paper contributes to exploring operating limits and to gaining an understanding of SiGe HBT reliability that is practically useful for RF circuit design.

There exist two frequently employed static breakdown voltages which are illustrated in the following. (A) The open-emitter collector-base BV BV_{CBO} essentially is the static BV of the (reverse-biased) base-collector (BC) junction. Since the DUT is embedded here in a ground-signal-ground (GSG) layout with grounded emitter (cf. Fig. 4(a)), BV_{CBO} = 4.8 V was measured with RF probes by forcing V_{BE} = 0 V, as shown in Fig. 1(a). (B) The open-base CE BV BV_{CEO} represents the static BV of the CE path. BV_{CEO} is illustrated in Fig. 1(b) by sweeping V_{CE} and *(i)* contacting only the RF probe on the collector side (I_B = 0) or *(ii)* forcing a constant low V_{BE} and observing the I_B zero-crossing.

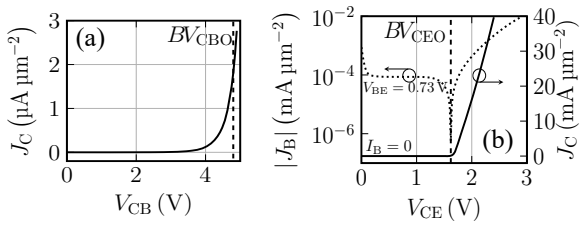

Fig. 1: Measured characteristics for illustrating the static breakdown voltages: (a) J_C at forced V_{BE} = 0 V for illustrating BV_{CBO} = 4.8 V; (b) J_B and J_C at forced V_{BE} = 0.73 V and at forced I_B = 0 for illustrating BV_{CEO} = 1.6 V.

Fig. 1(b) demonstrates that BV_{CEO} is practically meaningful for a large source resistance (i.e. I_B = const.), which causes holes generated by impact ionization in the BC space charge region to be back-injected into the emitter, thus amplifying the avalanche current by the DC forward current gain B_f. The other possible bias condition of a relatively high transistor input impedance (i.e. V_{BE} = const.) enables impact-ionization-generated holes to flow out of the base terminal, resulting in what is commonly referred to as base current reversal. Hence, one can determine BV_{CEO} for the V_{CE} at which this base current reversal occurs provided a relatively low V_{BE} is forced such that the mobile electron density is significantly lower than the collector doping concentration. The operating limit here is given by base pinch-in [6]. In PDKs, BV_{CEO} typically defines the upper limit of transient $v_{CE}(t)$ swings. However, this limit is arbitrary and too conservative because the transistor characteristics do not degrade apart from possibly I_B at low V_{BE} [7].

This work demonstrates that both the quiescent V_{CE} and the transient $v_{CE}(t)$ can significantly exceed BV_{CEO} without degrading the HBT RF performance. The goal is to explore the actual limits for RF LS operation, enabling enhanced circuit performance by utilizing the maximum device performance.

This paper is a continuation of the study [8] which demonstrated that *(i)* extreme static stress and dynamic stress with maximized $v_{CE}(t)$ swings do not lead to degradation of $\underline{Y}$-parameters measurable during reasonable stress times and *(ii)* the $\underline{Y}$-parameters of the SiGe HBT degrade under strongly nonlinear operating conditions which imply significant gain compression and thus output power saturation. The degradation-accelerating stress conditions in [8] (stress phase ac_3) were selected to make significant degradation measurable within a reasonable stress time, but did not enable to identify the onset of stress-related gradual changes in the transistor RF characteristics. Hence, the present study aims at identifying the absolute limits of large-signal transistor operation until which no $\underline{Y}$-parameter degradation can be detected, and beyond which systematically measurable degradation can be observed.

Section II describes a DC, small-signal and LS HICUM/L2 modelcard verification within the typical and the extended V_{CE} range. Section III presents an RF stress test which demonstrates the robustness of SiGe HBTs and establishes experimental evidence for the degradation of RF parameters under extreme RF stress. All data were obtained at an ambient temperature of T_{amb} = 298 K using IHP's SG13G2 process with (f_T, f_{max}) = (330, 500) GHz. The DUT is a single high-speed SiGe HBT in CBEBC contact configuration with an emitter window size of A_{E0} = 0.12 µm · 2.65 µm. All simulations were performed with HICUM/L2.

II TRANSISTOR CHARACTERIZATION

A. DC and small-signal transistor characterization

Fig. 2 shows the cut-off frequency f_T over a wide V_{BC} range as well as the output characteristics within the V_{CE} range typically used for model parameter extraction.

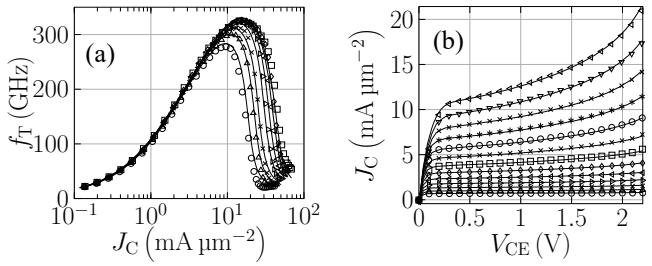

Fig. 2: (a) f_T measured at f_{meas} = 15 GHz versus J_C for V_{BC}/V = (0.5, 0.4, 0.3, 0.1, -0.1, -0.3, -0.5) and (b) output characteristics for V_{BE} = 0.8...0.92 V in steps of 10 mV. Symbols: measurements; lines: HICUM simulations.

The design of circuits with dynamic $v_{CE}(t)$ swings beyond the statically defined voltage BV_{CEO} requires an accurate compact model within the entire practically usable range of V_{CE} and V_{BE}. The HICUM modeling capabilities[9, 10] in the extended V_{CE} region are demonstrated in Fig. 3. The maximum usable V_{CE} is limited by avalanche multiplication. Once impact ionization has caused a sufficiently high avalanche current at high V_{CE}, the junction temperature increases as a result of self-heating, eventually leading to a positive feedback between impact ionization and self-heating, which causes an infinite slope of I_C and thus limits V_{CE}.

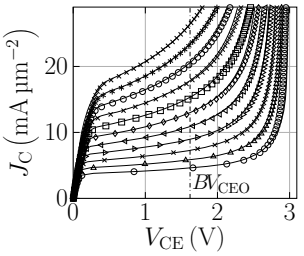

Fig. 3: Output characteristics (forced I_C, sensed V_{CE}) for V_{BE} = 0.86...0.96 V in steps of 10 mV. Symbols: measurements; lines: HICUM simulations. The dashed-dotted line marks BV_{CEO}.

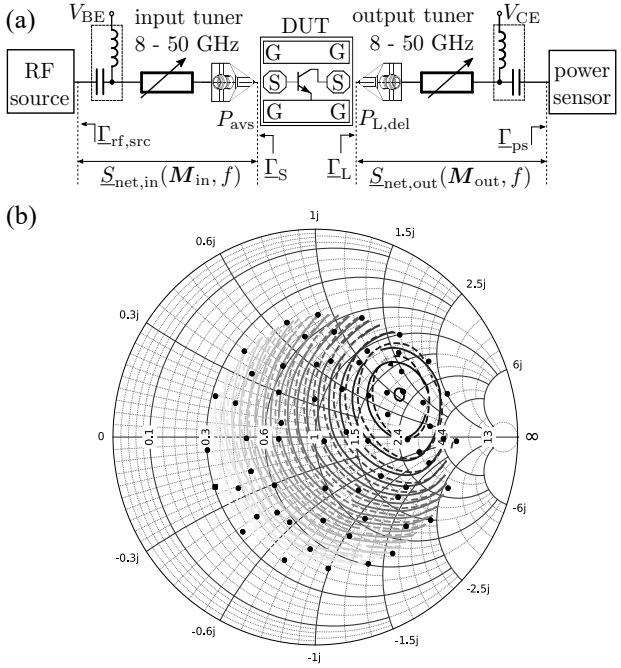

Fig. 4: (a) Schematic impedance tuner based setup for LS transistor characterization, (b) constant-power contours obtained from load-pull with fixed source reflection coefficient, J_C = 18.4 mA µm^{-2}, V_{BE} = 0.92 V, V_{CE} = 2 V, P_{avs} = -4.15 dBm, f_0 = 10 GHz, $\underline{\Gamma}_{S0}$ = 0.38∠52.8°, ($P_{L,del,max}$/dBm, $P_{L,del,min}$/dBm, ΔP_L/dB) equal to (9.98, 3.62, 0.32) from the measured (solid contour lines) and (9.82, 3.08, 0.34) from the HICUM-simulated (dashed contour lines) output powers.

B. Large-signal transistor characterization

The LS measurements and the RF stress tests were performed at the calibrated DUT reference planes with a passive impedance tuner system as schematically depicted in Fig. 4(a). The fundamental frequency of this stress test is f_0 = 10 GHz. Fig. 4(b) shows closed constant-power contours obtained from load-pull measurements and simulations for the fundamental load reflection coefficients $\underline{\Gamma}_{L0}$ depicted by the points scattered across the Smith chart.

Fig. 5(a) shows a power sweep with fixed fundamental source and load reflection coefficient $\underline{\Gamma}_{S0}$ and $\underline{\Gamma}_{L0}$, respectively. Note that even though the quiescent V_{CE} as well as the transient $v_{CE}(t)$ (significantly) exceed BV_{CEO} = 1.6 V and the V_{CE} range typically used for parameter extraction,

the agreement between measurement and simulation is very good. Fig. 5(b) depicts load ellipses, i.e. $i_C(t) = f(v_{CE}(t))$, for increasing available powers from the source P_{avs}, demonstrating that the DUT is stressed dynamically by the RF operating conditions.

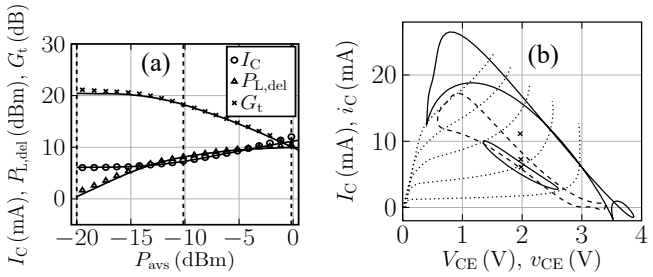

Fig. 5: (a) Power sweep with fixed source and load reflection coefficient $\underline{\Gamma}_{S0} = 0.38\angle 52.8°$ and $\underline{\Gamma}_{L0} = 0.56\angle 17.8°$ at $V_{BE} = 0.92$ V, $V_{CE} = 2$ V, $J_C = 18.4$ mA µm^{-2}, $f_0 = 10$ GHz. Comparison between measurements (symbols) and HICUM simulations (lines). The dashed vertical lines mark the P_{avs} of the load ellipses shown in (b). (b) Simulated output characteristics for $V_{BE} = 0.86...1.1$ V in steps of 60 mV (dotted lines) and dynamic load ellipses for the increasing P_{avs}/dBm = (-20, -10.15, -0.17) (solid, dashed, solid load ellipse). The crosses mark the static I_C for the increasing P_{avs}.

III RF STRESS TEST

To dynamically stress the DUT such that gradual degradation-related changes in the $\underline{Y}$-parameters can be observed, the source and load reflection coefficients $\underline{\Gamma}_{S0}$ and $\underline{\Gamma}_{L0}$ are fixed and the power available from the source P_{avs} is gradually increased, thereby increasingly driving the transistor into gain compression and increasing the nonlinearity, as illustrated in Fig. 6(a). The stress test was periodically interrupted to measure selected characteristics for monitoring possible degradation-related changes. Fig. 6(b) shows DC forward current gain curves $B_f = f(J_C)$ measured after specific cumulative stress times. Extreme dynamic operation first leads to a significant increase of B_f which may be explained by a deactivation of traps related to impurities from the fabrication process [11]. When applying extreme P_{avs}, B_f decreases again as a result of trap generation at the emitter-base spacer oxide [5]. Fig. 6(c) shows the measured $\mathrm{Re}\{\underline{Y}_{21}\}$ over t_{stress}. During the stress phase with $P_{avs} = 7.5$ dBm, $\mathrm{Re}\{\underline{Y}_{21}\}$ increases at low V_{BE} (e.g. 0.77 V). Since at this bias the impact of series resistances such as R_{Bx}, R_{Cx} and R_E is negligible, the increase is attributed to additional electron injection across the BE junction. Fig. 6(d) shows the measured $\mathrm{Im}\{\underline{Y}_{11}\}$ over t_{stress}. At $V_{BE} = 0$ V, $\mathrm{Im}\{\underline{Y}_{11}\}$ is dominated by the junction capacitances and does not change even under the most extreme dynamic stress conditions. Only at higher V_{BE}, when $\mathrm{Im}\{\underline{Y}_{11}\}$ is dominated by the BE diffusion capacitance, a systematic stress-related increase can be observed. This change hints toward the degradation of the mobile charge storage behavior, which is consistent with the observation for $\mathrm{Re}\{\underline{Y}_{21}\}$ above.

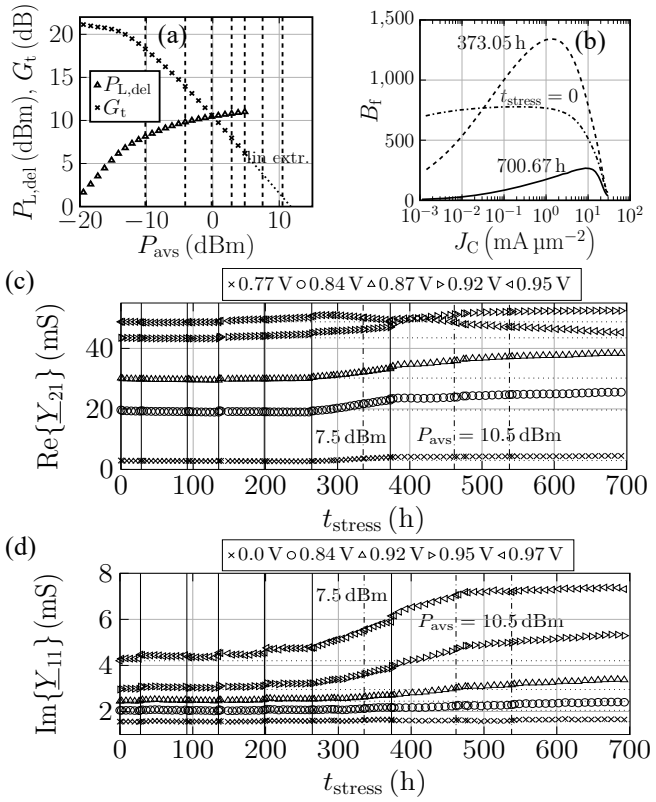

Fig. 6: (a) Illustration of the increasing P_{avs} (marked by the vertical dashed lines) applied during the consecutive stress phases (the same conditions as in Fig. 5). (b) Measured DC forward current gain characteristics with $V_{CE} = 0.5$ V at specific cumulative stress times. (c) $\mathrm{Re}\{\underline{Y}_{21}\}$ and (d) $\mathrm{Im}\{\underline{Y}_{11}\}$ with $V_{CE} = 0.5$ V (embedded data, measured at $f_{meas} = 10$ GHz) over t_{stress}. The legends specify the V_{BE} values. The *solid vertical lines* separate the stress phases. A re-calibration was performed prior to each stress phase. The *dashed-dotted vertical lines* mark re-calibrations without a change of the stress conditions. The *dotted horizontal lines* show the respective $\mathrm{Re}\{\underline{Y}_{21}\}$ and $\mathrm{Im}\{\underline{Y}_{11}\}$ values measured prior to the first stress test.

IV SUMMARY

Results of a long-term RF stress test demonstrate that SiGe HBTs can, within the test duration, be reliably operated far beyond the static breakdown voltage BV_{CEO}. Moreover, it has been found that only extreme RF operating conditions which drive the SiGe HBT into deep gain compression can cause measurable degradation of RF parameters ($\underline{Y}$-parameters). For continuing this SiGe HBT reliability study and enabling a physics-based analysis, the next logical step is to stress transistors with different emitter widths to find out whether the reported degradation effects are area- or perimeter-related. This investigation is presently under way.

ACKNOWLEDGEMENT

This project was partially funded by the German National Science Foundation (DFG project SCHR 695/17). The authors would like to express their gratitude to Rohde & Schwarz for providing a ZVA50 for the long-term RF tests.

REFERENCES

[1] P. Chevalier et al., "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," Proc. of the IEEE, vol. 105, no.6, pp. 1035-1050, 2017.

[2] M. Schröter et al., "SiGe HBT technology: Future trends and TCAD based roadmap", Proc. of the IEEE, vol. 105, no. 6, pp. 1068-1086, 2017.

[3] G. G. Fischer, G. Sasso, "Ageing and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions," Microel. Reliab., vol. 55, no. 3, pp. 498-507, 2015.

[4] J. D. Cressler, "Emerging SiGe HBT reliability issues for mixed-signal circuit applications," IEEE Trans. Dev. and Mat. Reliab., vol. 4, no. 2, pp. 222-236, 2004.

[5] J. D. Cressler, "New developments in SiGe HBT reliability for RF through mmW circuits," IEEE IRPS, pp. 1-6, 2021.

[6] M. Rickelt and H.-M. Rein, "A novel transistor model for simulating avalanche-breakdown effects in Si bipolar circuits", IEEE J. Solid-State Circuits, vol. 37, 2002, pp. 1184-1197.

[7] P. Cheng et al., "Reliability of SiGe HBTs for Power Amplifiers—Part II: Underlying Physics and Damage Modeling," IEEE Trans. Dev. and Mat. Reliab., vol. 9, no. 3, pp. 440-448, 2009.

[8] C. Weimer et al., "An Experimental Load-Pull Based Large-Signal RF Reliability Study of SiGe HBTs," IEEE BCICTS, 4p., 2021

[9] M. Jaoul et al., "A compact formulation for avalanche multiplication in SiGe HBTs at high injection levels", IEEE Trans. Electron Dev., vol. 66, no. 1, pp. 264-270, 2019.

[10] M. Schröter, et al., "HICUM/L2: Extensions over the last decade," 2020 IEEE BCICTS, 2020, pp. 1-4.

[11] B. Ardouin et al., "Advancements on reliability-aware analog circuit design," Proc. ESSCIRC, pp. 46-52, 2012.