An Experimental Load-Pull Based Large-Signal RF Reliability Study of SiGe HBTs

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***Abstract* -- Results of a large-signal RF reliability study of SiGe HBTs are presented. The study consists of consecutive stress phases with different stress conditions. First, the DUT is stressed statically, which leads only to the widely reported excess base current at relatively low injection levels. Second, the DUT is stressed dynamically with voltage swings that significantly exceed the statically defined open-base collector-emitter breakdown voltage. The DUT withstands this type of stress, which proves SiGe HBTs to be extremely robust. Third, experimental evidence is established for significant degradation of the admittance parameters that occurs only under extreme nonlinear large-signal operation. Further experimental evidence suggests that the observed degradation occurs inside the internal HBT.**

***Index Terms* --- SiGe HBT, HICUM, RF reliability, load-pull.**

I Introduction

The peak cut-off frequencies of modern high-speed Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs) have been continuously improved [1]. This has been achieved through increasingly higher collector doping, which alleviates high-current related effects, but inherently decreases the statically defined open-base collector-emitter (CE) breakdown voltage BV_{CEO}. In process design kits (PDKs), BV_{CEO} is often (arbitrarily) specified as the upper usable V_{CE} limit and thus interpreted by many circuit designers as the upper limit of what the transistor withstands in terms of dynamic voltage swings. To experimentally explore SiGe HBT reliability at the device level, previous investigations have primarily focussed on direct-current (DC) stressing the devices under test (DUTs) *(i)* with a strongly reverse-biased base-emitter junction *(ii)* in bias points where $V_{CE} > BV_{CEO}$ at different collector injection levels (e.g. [2]). In particular, the so-called mixed-mode stress occurs when the SiGe HBT is simultaneously subject to high collector-base voltages and moderate to high collector current densities. It causes an excess base current at low injection levels in static forward- and inverse-mode transistor operation. The underlying reason is high-energy charge carrier caused interface trap generation at the emitter-base spacer oxide and at the shallow trench isolation, respectively [3, 4]. In summary, the DC base current has been the main degradation indicator in previous SiGe HBT reliability studies.

The following two concerns remain: *(i)* In radio-frequency (RF) operation the dynamic $i_C(t)$ and $v_{CE}(t)$ swings can temporarily traverse regions in the output characteristics that cannot be reached in DC operation [5]. They are an attribute of dynamic large-signal transistor operation and thus expose the transistor to a type of stress that is different from classical DC stress. *(ii)* The DC base current, especially at low injection levels, is only of little relevance to analog high-frequency circuit blocks such as power amplifiers. Hence, it is an unsatisfactory indicator of device degradation during RF circuit design and prevents the exploitation of the full performance potential of the technology.

The fundamental questions are: *(i)* Do SiGe HBTs degrade with respect to applications, for which the low-injection excess base current is practically irrelevant? *(ii)* Does a degradation mechanism, other than the low-injection excess base current, exist prior to the destruction of SiGe HBTs, especially under extreme RF stress?

Given this reasoning, this work contributes to the exploration of the operating limits of SiGe HBTs as follows. In section II, a DC, small-signal and large-signal HICUM/L2 modelcard verification is performed, confirming its suitability for assessing and defining dynamic stress conditions. In section III, the stress conditions are defined and the stress test consisting of consecutive phases with different DC and RF stress conditions is performed. In addition to the DC base current, all admittance parameters of the DUT are periodically measured to monitor device degradation. Section IV summarizes this paper.

II HICUM/L2 modelcard verification

The results reported in this paper have been obtained at an ambient temperature of $T_{amb} = 298$ K using IHP's SG13G2 process with (f_T, f_{max}) = (300 GHz, 500 GHz) and $BV_{CEO} = 1.7$ V. The DUT is a single high-speed SiGe HBT in CBEBC contact configuration with an emitter window size of $A_{E0} = 0.12\ \mu m \cdot 5.15\ \mu m$ embedded in a ground-signal-ground (GSG) layout with grounded emitter. The corresponding modelcard was extracted with a Python-based in-house parameter extraction framework [6]. Selected measured and simulated figures of merit of the DUT are shown in Fig. 1.

The large-signal measurements and stress tests were performed at the calibrated DUT reference planes using a passive load-pull system as schematically depicted in Fig. 2(a). The fixtures of the experimental setup were characterized over the entire impedance tuner bandwidth from 8 GHz to 50 GHz. Given the fundamental frequency $f_0 = 10$ GHz of this study, the reflection coefficients at the DUT reference planes were calculated up to the fifth harmonic (50 GHz) by cascading the measured $\underline{S}$-parameters of the fixtures. The netlist used for load-pull simulations takes the harmonic reflection coefficients of the

setup [7] along with the electromagnetically simulated GSG layout into account. An accurate description of the fundamental and harmonic reflection coefficients at the DUT reference planes is necessary to simulate with sufficient accuracy the time-domain $i_C(t)$ and $v_{CE}(t)$ swings of distorted signals.

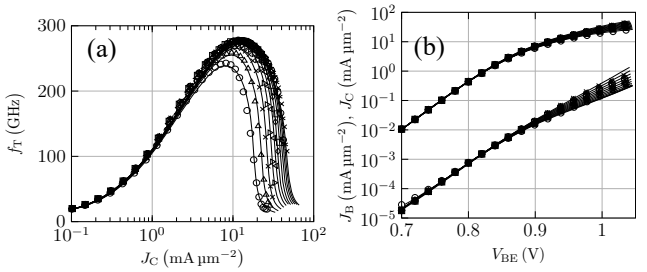

Fig. 1: (a) Transit frequency measured at f_{meas} = 15 GHz versus collector current density and (b) Gummel characteristics for V_{BC} = 0.5...-0.5 V in steps of -0.1 V. Symbols: measurement data; lines: HICUM/L2 simulations.

The load-pull technique has been chosen for this study because it enables to dynamically stress the DUT under varying load conditions and thus different dynamic $i_C(t)$ and $v_{CE}(t)$ swings. Fig. 2(b) shows closed isopower contours obtained from load-pull measurements and simulations for the fundamental load reflection coefficients $\underline{\Gamma}_{L0}$ depicted by the points scattered across the Smith chart. The available power from the source was fixed at P_{avs} = -6.88 dBm at f_0 = 10 GHz. The innermost constant-power contour indicates the Smith chart area in which maximum power is delivered to the load.

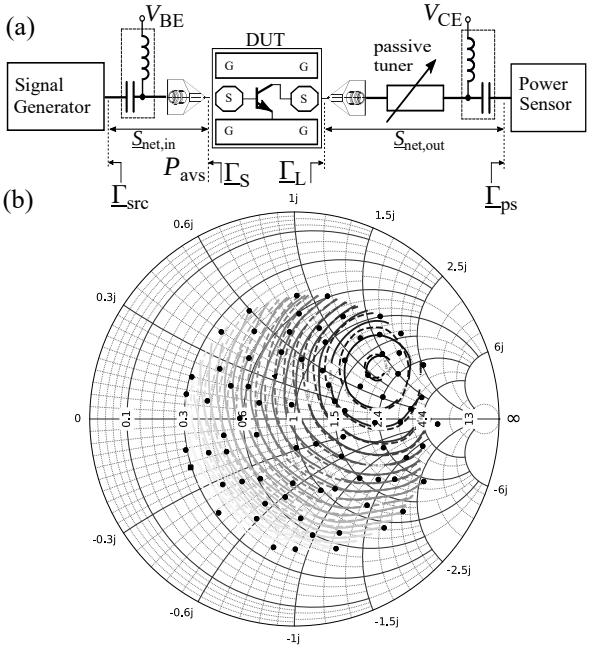

Fig. 2: (a) Schematic passive load-pull setup (b) constant-power contours obtained from load-pull with J_C = 9 mA µm^{-2}, V_{BE} = 0.9 V, V_{CE} = 2.0 V, f_0 = 10 GHz, P_{avs} = -6.88 dBm and ($P_{L,del,max}$/dBm, $P_{L,del,min}$/dBm, ΔP_L/dB) equal to (a) (9.54, 2.96, 0.33) from measured data (solid contour lines) and (b) (9.79, 3.57, 0.31) from HICUM/L2 simulation data (dashed contour lines).

In Fig. 3(a), the fundamental load reflection coefficient is fixed to $\underline{\Gamma}_{L0} = 0.44\angle 13.8°$ and P_{avs} is swept. Under nonlinear operating conditions, due to gain compression, the output power of the DUT saturates and the even harmonics which contain a DC offset component lead to the expansion of the DC collector current. All phenomena are accurately reproduced by the simulations. Note that the CE bias voltage $V_{CE} \geq 2$ V exceeds BV_{CEO} = 1.7 V in the large-signal measurements and simulations. In dynamic operation, the voltage BV_{CEO} thus is temporarily significantly exceeded.

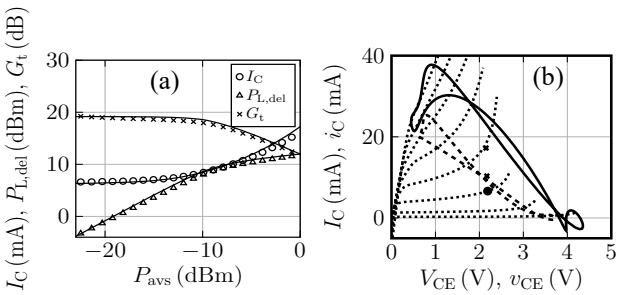

Fig. 3: (a) Power sweep with fixed fundamental load reflection coefficient $\underline{\Gamma}_{L0} = 0.44\angle 13.8°$, f_0 = 10 GHz, J_C = 9.9 mA µm^{-2}, V_{BE} = 0.9 V, V_{CE} = 2.2 V: comparison between measurement (symbols) and HICUM/L2 simulations (lines). (b) Simulated output characteristics for V_{BE} = 0.8...1.15 V in steps of 50 mV (dotted lines) and dynamic load ellipses for P_{avs} of -6.88 dBm (dashed line) and 0 dBm (solid line). The filled dot marks the quiescent I_C, the crosses mark the expanded I_C for both P_{avs}.

Fig. 2(b) and Fig. 3(a) are limited to power considerations. However, for analyzing dynamic stress conditions, time domain analysis is preferable because it directly shows the regions of the output characteristics that are dynamically traversed by the signal swings. Thus, the simulated load ellipses for two P_{avs}, which operate the transistor under increasingly nonlinear conditions, are given in Fig. 3(b). The reliability concerns arising from such extreme dynamic operation are inconclusive and thus subsequently examined.

III Consecutive Stress Tests

Fig. 4 shows output characteristics obtained by forcing I_C and sensing V_{CE} so as to capture the strong avalanche effect related breakdown region while avoiding thermal runaway.

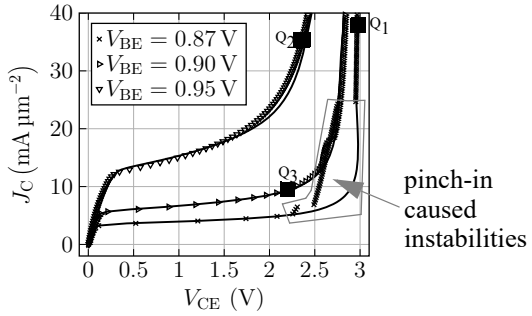

Fig. 4: Output characteristics (forced I_C, sensed V_{CE}) with the quiescent bias points $Q_{1...3}$. Quiescent bias points: (J_C / (mA µm^{-2}), V_{BE}/V, V_{CE}/V) = (38, 0.87, 3), (35, 0.95 2.4), (9.5, 0.9, 2.2). Symbols: measurement data; lines: HICUM/L2 simulations.

The employed HICUM/L2 model comprises a unified avalanche model formulation valid at different collector injection levels [8]. At moderate collector injection (V_{BE} = 0.87 V here), pinch-in caused instabilities distort the measured output characteristics toward higher V_{CE}. The appearance of these instabilities suggests that the measure-

ments are close to the actual transistor breakdown, which depends on the collector injection level and V_{CE}.

The DUT was stressed during five consecutive phases with different stress conditions, whose quiescent bias points $Q_{1...3}$ are depicted in Fig. 4. The time intervals during which the DUT was stressed statically in the quiescent bias points Q_1 and Q_2 are denoted as dc_1 and dc_2, respectively. dc_1 was applied to operate the transistor close to its *static* breakdown. dc_2 (with Q_2) was applied to verify that no damage other than DC base current degradation occurs, making the measured degradation in ac_3 (with the same Q_2) attributable to dynamic stress.

Then, the DUT was subject to dynamic stress at the fundamental frequency $f_0 = 10$ GHz. During the stress interval ac_1, the quiescent bias point was Q_3 with $P_{avs} = -6.88$ dBm, while presenting $\underline{\Gamma}_{L0} = 0.68\angle 22.5°$ to the output of the DUT, causing the load ellipse shown in Fig. 5(a). The output conductance g_{CE} in Q_3 is still relatively low, making this quiescent point a reasonable choice for power amplifier design with large signal swings. The $\underline{\Gamma}_{L0}$ of stress phase ac_1 represents favorable load conditions for high output power.

During the stress interval ac_2, the quiescent bias point was Q_3 with $P_{avs} = -3.86$ dBm and $\underline{\Gamma}_{L0} = 0.7\angle -25.5°$ with the corresponding load ellipse given in Fig. 5(b). The $\underline{\Gamma}_{L0}$ of stress phase ac_2 peaks the transient $v_{CE}(t)$ swings.

During the stress interval ac_3, the quiescent bias point was Q_2 with $P_{avs} = 7.15$ dBm and $\underline{\Gamma}_{L0} = 0.631\angle 9.5°$ with the load ellipse given in Fig. 5(c). The strongly nonlinear transistor operation in stress phase ac_3 causes a significant expansion of the static collector current due to even harmonics. The static I_C expands to regions of the output characteristics that cannot be reached in a DC measurement without device destruction. This is further proof that dynamic stress is essentially different compared to static stress. The extreme stress conditions of phase ac_3 were applied specifically to accelerate degradation of the DUT, thereby making the damage unambiguously measurable within days which can potentially occur over several years of operation.

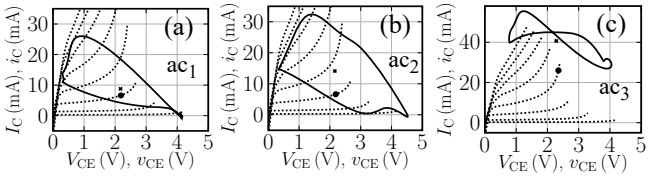

Fig. 5: Simulated dynamic load ellipses (solid lines) for various dynamic stress conditions (with $f_0 = 10$ GHz) over simulated output characteristics (dotted lines) for $V_{BE} = 0.8...1.15$ V in steps of 50 mV. The circles mark the collector currents of the quiescent bias points. The crosses mark the shifted DC collector currents due to even harmonics occurring in nonlinear transistor operation.

The stress tests were periodically interrupted to measure selected characteristics for monitoring possible degradation-caused changes. Fig. 6(a) shows the periodically measured forward base current. The static stress phases dc_1 and dc_2 affect only I_B at low injection levels and eventually lead to a saturation of the trap generation at the emitter-base spacer oxide. Dynamic stress, which starts with stress phase ac_1, affects I_B at all injection levels, suggesting additional trap generation. In stress phase ac_3, I_B decreases again at all injection levels, which is believed to be attributable to the extreme I_C expansion and the resulting significant self-heating induced junction temperature increase, causing annealing of interface traps.

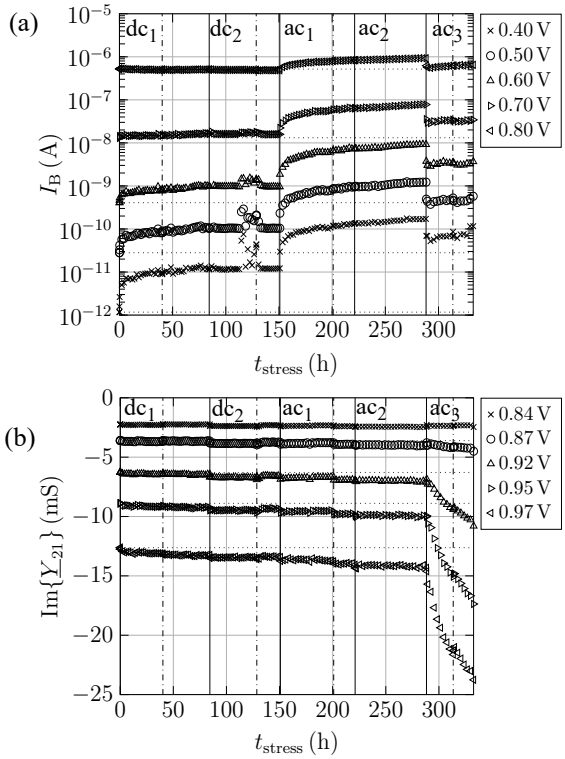

Fig. 6: (a) I_B and (b) Im{$\underline{Y}_{21}$} (embedded data) measured at $f_{meas} = 10$ GHz at specific cumulative stress times with $V_{CE} = 0.5$ V and the V_{BE} values specified in the legends. The *solid vertical lines* separate the stress phases. A re-calibration was performed prior to each stress phase. The *dashed-dotted vertical lines* mark re-calibrations without a change of the stress conditions. The *dotted horizontal lines* represent the respective Im{$\underline{Y}_{21}$} values measured prior to the first stress test.

Fig. 6(b) shows Im{$\underline{Y}_{21}$} for the five stress phases. Note that peak f_T is obtained at approximately $V_{BE} = 0.92$ V. A possibly degradation-caused change in Im{$\underline{Y}_{21}$} starts in stress phase ac_1. It occurs, however, only at high injection levels and is very small, which proves SiGe HBTs to be extremely rugged. Any possibly degradation-caused changes smaller than 10 % should only be very carefully commented on because of the inherent high-frequency measurement uncertainty. To verify that the observed changes are in fact due to degradation, the extreme stress conditions of phase ac_3 were applied which cause significant permanent damage to the DUT given the sharp decrease of Im{$\underline{Y}_{21}$}. The changes in Im{$\underline{Y}_{21}$} are consistent across different calibrations of the vector network analyzer. *Morever, this degradation effect has been reproduced on different dies*. Note that the degradation decreases toward lower injection levels. Since it has been confirmed that the zero-bias base-emitter and base-collector depletion capacitances do not change, stress phase ac_3 causes only the diffusion capacitance, i.e. the mobile charge transport, to degrade. A similar result has been obtained for Im{$\underline{Y}_{11}$} and Im{$\underline{Y}_{12}$}. Thus, f_T degrades due to the applied dynamic stress, as demonstrated below.

In a first attempt to find the reason for the observed degradation, one might hint at the relatively high DC collector current in stress phase ac_3. To exclude the possibility of electromigration-caused increased metallization resistances of the base and collector metal stack, a DC stress test of the SHORT de-embedding structure was performed. The simultaneously forced DC currents $I_{B,mstack,forced} = 20$ mA and $I_{C,mstack,forced} = 60$ mA for stressing the base and collector metal stack were higher than the simulated peak values of the dynamic base and collector current of stress phase ac_3. No changes in the real and imaginary parts of the impedance parameters of the SHORT structure have been measured. This is exemplified in Fig. 7(a) by $\mathrm{Re}\{\underline{Z}_{22,short}\}$ measured at different cumulative stress times.

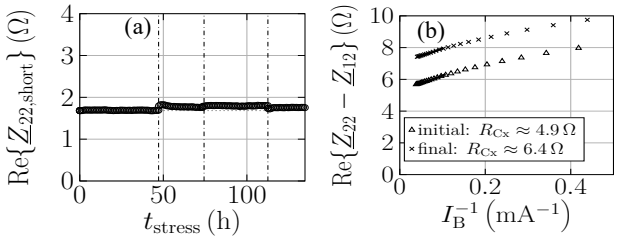

Fig. 7: (a) $\mathrm{Re}\{\underline{Z}_{22,short}\}$ measured at specific cumulative stress times at $f_{meas} = 10$ GHz. (b) Extraction of R_{Cx} with $V_{CE} = 0$ V at $f_{meas} = 10$ GHz before and after the stress test.

The SHORT structure comprises all metal layers from the top metals down to the second lowest metal layer *metal2*. One might now argue that the collector fingers (on the lowermost metal layer *metal1*) of the CBEBC configuration with $l_{E0} = 5.15$ µm are relatively long. Electromigration might cause their resistance to increase, in which case the observed degradation would be attributable to a layer that belongs to the transistor, but it would not be inside the internal HBT. Thus, the external collector resistance R_{Cx} was extracted from the measurement performed prior to the stress tests and from the measurement after $t_{stress} = 332$ h 37 min using the $\underline{Z}$-parameter method [9]. The measured difference of 1.5 Ω does not explain the significant degradation in f_T depicted in Fig. 8.

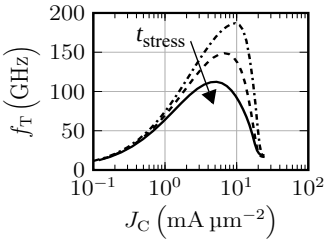

Fig. 8: Transit frequency (embedded data) versus collector current density measured at $f_{meas} = 10$ GHz with $V_{CE} = 0.5$ V prior to the stress tests and subsequent to specific cumulative stress times t_{stress} = (0, 301 h 27 min, 332 h 37 min) in descending order.

Hence, the underlying reason for the observed degradation must occur inside the internal HBT and is believed to be the degradation-modified mobile charge storage behavior. Further research is presently under way.

The extreme stress conditions of phase ac_3 were selected specifically to accelerate degradation of the DUT. The goal was to prove that extreme dynamic nonlinear operating conditions cause a type of stress that is essentially different from static stress and can cause significant degradation affecting all admittance parameters. In particular, strongly nonlinear large-signal transistor operation, which causes a significant expansion of the DC collector bias current as a result of even harmonics, can potentially limit the reliable long-term device and thus circuit RF operability.

IV Summary

This work contributes to the exploration of RF operating limits of SiGe HBTs. Stress tests consisting of consecutive phases with different DC and RF stress conditions prove SiGe HBTs to be extremely robust and, within the investigated stress times, reliably operable far beyond conventionally defined static operating limits. Moreover, it has been demonstrated that extreme nonlinear large-signal operating conditions can cause severe degradation which significantly affects all admittance parameters and thus gain and speed. Experimental evidence suggests that the observed degradation occurs inside the internal HBT.

The excellent agreement of HICUM/L2 simulation and measurement data for DC, small-signal and large-signal over a wide range of load reflection coefficients and available powers from the source confirms the compact model and extracted model parameters to be an adequate vehicle for assessing dynamic stress conditions.

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