Characterization of Dynamic Large-Signal Operating Limits and Long-Term RF Reliability of SiGe HBTs

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***Abstract* - The dynamic (RF) large-signal operating limits of advanced SiGe HBTs are systematically explored and discussed. Experimental results of long-term RF stress tests performed with a passive load-pull system are presented and analyzed. The experimental data demonstrate that SiGe HBTs are extremely robust and can be operated statically and dynamically far beyond the open-base collector-emitter breakdown voltage without noticeable degradation during the long stress times. The results suggest that only extremely non-linear large-signal operating conditions cause significant degradation of the admittance parameters. RF stress tests of HBTs with different emitter widths suggest that the measured degradation is area-related and can be attributed to the minority carrier charge storage and transport.**

Keywords: SiGe HBT, electrical stress, RF reliability, load-pull, breakdown.

I. Introduction

Present and future radio-frequency (RF) applications require electronic circuits to provide high output power at high frequencies. For achieving high *dynamic* output power, transistors need to be operated with large current and voltage swings. Realizing such large signal swings becomes increasingly challenging due to the inherent trade-off between high RF performance (i.e. high cut-off frequency) and low breakdown voltages. As a result, thorough investigations of the long-term RF reliability become an indispensable part of the transistor characterization. This work presents experimental reliability investigations of Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs), which have become attractive for a variety of mm-wave applications [1, 2].

Widely reported conventional static stress tests (e.g. [3, 4]) *(i)* with a strongly reverse-biased base-emitter (BE) junction or *(ii)* with moderate to high collector current densities at high V_{CB} do not satisfactorily address reliability related concerns during the design of RF circuits. In particular, RF power amplifiers require maximum *dynamic* signal swings to boost the output power density of a transistor. The reliability concerns posed by RF large-signal (LS) non-linear transistor operation have remained unclear so far and can only be addressed by *dynamic* stress tests, as discussed in this paper.

Moreover, the frequently discussed (e.g. [3, 4]) stress-related *static* low-injection excess base current, causing a decrease of the static forward current gain at low V_{BE}, is of little relevance to many RF circuit building blocks based on LS operation, such as power amplifiers. To characterize RF circuit related degradation, measurements of *(i)* the dynamic LS behavior and *(ii)* the admittance parameters of HBTs are much more useful than direct-current (DC) measurements. In particular, the admittance parameters enable to attribute possible degradation-related changes to conductances and capacitances. Given this rationale, systematic RF reliability investigations consisting of RF LS stress and periodic measurements of the admittance parameters of SiGe HBTs have been performed in [6, 7]. These investigations indicated no noticeable degradation of the $\underline{Y}$-parameters during reasonable stress times (of several tens/hundreds of hours) when the device is subjected to dynamic stress with maximized $v_{CE}(t)$ swings in different operating points with $V_{CE} > BV_{CEO}$ and across different fundamental load reflection coefficients $\underline{\Gamma}_{L0}$. Degradation of the the $\underline{Y}$-parameters was observed only under strongly non-linear operating conditions which imply significant gain compression and thus output power saturation as well as a considerable increase of the static I_C.

This paper is organized as follows. Section II discusses concepts and preconditions relevant to long-term HBT reliability measurements. Section III.*A* recapitulates existing results, whereas section III.*B* continues the study [7] by applying the same RF stress methodology as in [7] to HBTs with identical emitter length l_{E0} but different emitter widths b_{E0}. Conclusions are provided in Section IV.

The experimental setup used for LS transistor characterization and RF stress tests is shown in Fig. 1. The RF switches enable to flexibly alternate between the RF LS path (from the RF source to the power sensor/spectrum analyzer) and the vector network analyzer (VNA) path (for performing DC and small-signal measurements). Here, the device under test (DUT) is a single SiGe HBT of IHP's high-speed process SG13G2 in CBEBC contact configuration embedded in a ground-signal-ground (GSG) layout with grounded emitter.

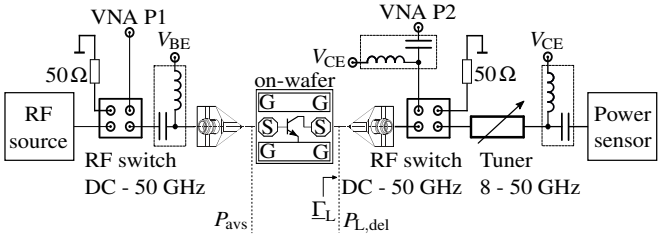

Fig. 1: Schematic passive load-pull setup with RF switches enabling alternating between RF stress and $\underline{S}$-parameter measurements.

The alternation between RF LS stress and DC and small-signal measurements is fully automated by means of a Python-based object-oriented measurement instruments remote control framework [8]. The simulations were performed using a Python-based toolkit [9].

II. RF RELIABILITY CONSIDERATIONS

A. Static bipolar transistor breakdown voltages

Fig. 2 illustrates the static breakdown voltages BV_{CEO} and BV_{CBO} which are commonly referred to for estimating the operating limits of bipolar transistors. BV_{CEO} is obtained at $I_B = 0$ by sweeping V_{CE} and measuring I_C. Hence, BV_{CEO} is practically meaningful for a large source resistance (I_B = const.), so that holes generated by impact ionization in the base-collector (BC) space charge region are back-injected into the emitter, thus amplifying the avalanche current by the DC forward current gain. On the other hand, BV_{CBO} is the static breakdown voltage of the BC junction and thus is defined for an open emitter. Since the DUT is available only in RF GSG pads, BV_{CBO} is approximated here at $V_{BE} = 0$ and by sweeping $V_{CE} = V_{CB}$ while measuring I_C.

In addition, Fig. 2 depicts measured output characteristics with forced V_{BE}. For $V_{CE} > BV_{CEO} = 1.6$ V, at moderate V_{BE} the maximum attainable static V_{CE} is limited by avalanche multiplication. Once impact ionization has caused a sufficiently high avalanche current at high V_{CE}, the junction temperature rises due to self-heating. The resulting positive feedback between avalanche multiplication and self-heating eventually causes an infinite slope of I_C and thus limits V_{CE} at moderate V_{BE}. At very high V_{BE}, self-heating dominates across the whole V_{CE} range, causing such a significant I_C increase that V_{CE} can, if at all, only slightly exceed BV_{CEO}.

Furthermore, Fig. 2 shows the simulated load ellipse of the stress phase ac_2 of the study [6], demonstrating that sufficiently large input powers can cause *dynamic* $i_C(t)$-$v_{CE}(t)$ swings far beyond BV_{CEO} up to $v_{CE}(t)$ ($\approx v_{CB}(t)$) $\approx BV_{CBO}$. Conventional static stress tests are insufficient for evaluating the reliability concerns which arise from such extreme dynamic LS transistor operation because the transient $v_{CE}(t)$ can reach values much larger than the maximum DC-measured V_{CE}.

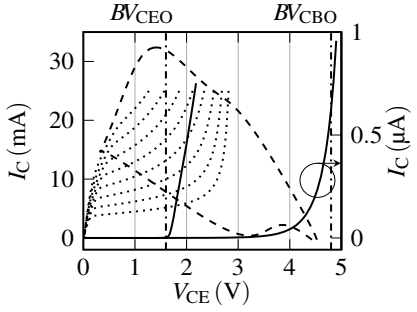

Fig. 2: Illustration of $BV_{CBO} = 4.8$ V (right dash-dotted line), and of $BV_{CEO} = 1.6$ V (left dash-dotted line). The dotted lines show measured output characteristics ($V_{BE} = 0.9$ V...1.04 V in steps of 20 mV) of a DUT with $b_{E0} = 0.12$ µm, $l_{E0} = 5.15$ µm. The dashed line represents the simulated load ellipse with maximized $v_{CE}(t)$ swing applied during an RF stress test [6]. Only the right solid line belongs to the right *y*-axis

B. Breakdown effects in dynamic operation

When evaluating device reliability under RF LS operating conditions, the dynamic behavior of the physical breakdown phenomena must be considered. Here, self-heating is a key factor. Fig. 3 depicts the absolute value of the thermal impedance $\underline{Z}_{th}$ as a function of frequency in different operating points. $\underline{Z}_{th}$ was characterized by means of the admittance parameter method using the technology SG13G2 [10]. Fig. 3 demonstrates that the absolute value of $\underline{Z}_{th}$ tends to zero for practical operating frequencies which are typically larger than 1 GHz for modern SiGe high-speed technologies.

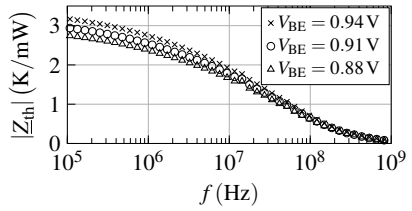

Fig. 3: Frequency-dependent characterization of the absolute value of the thermal impedance $\underline{Z}_{th}$ using the process SG13G2 [10]. Data obtained at $T_{amb} = 323$ K, $V_{CE} = 0.75$ V.

Considering the self-heating modeling with an adjunct single-pole network implemented in many compact models, the absolute value of $\underline{Z}_{th}$ reads

$$\left|\underline{Z}_{th}\right| = \frac{R_{th}}{\sqrt{1 + 4\pi^2 (\tau_{th}/T)^2}} \tag{1}$$

with the thermal resistance R_{th}, the thermal time constant $\tau_{th} = R_{th}C_{th}$, the thermal capacitance C_{th} and the period duration T. If the period duration T becomes significantly smaller than the thermal time constant τ_{th}, self-heating cannot follow the dynamic signal swings anymore and thus $|\underline{Z}_{th}| \approx 0$. Hence, self-heating is only relevant when choosing the operating point, but is no practical concern for dynamic LS swings. This reasoning suggests that the maximum permissible CE voltage is different depending on whether quiescent V_{CE} or transient $v_{CE}(t)$ are considered. An efficient way to visualize and quantify this difference is to look at output characteristics with and without self-heating, e.g. using HICUM/L2 [5]. Fig. 4 analyzes the impact of self-heating and avalanche multiplication on the output characteristics.

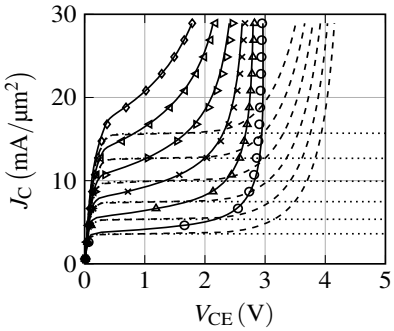

Fig. 4: Output characteristics of a DUT with $b_{E0} = 0.12$ µm, $l_{E0} = 2.65$ µm for $V_{BE} = 0.86$ V...0.96 V in steps of 20 mV. Symbols: Measurement data. Lines: Simulation data with SH on (*flsh* = 2) and AVL on (solid lines), SH off and AVL on (dashed lines), SH off and AVL off (dotted lines).

The dashed output characteristics in Fig. 4 represent the case where avalanche multiplication (AVL) is turned on and self-heating (SH) is turned off. Given the above rationale, these are the actual output characteristics "seen" by an RF signal with $f > 1$ GHz, provided that impact ionization occurs instantaneously. This proves that the maximum DC-measured V_{CE}, with which conventional DC stress tests are typically performed, are far away from the actual RF operating limits. In static operation, the positive feedback between AVL and SH in the model yields an excellent agreement of the simulated output characteristics (solid lines) with measurement data.

C. Large-signal verification in extended operating regions

When fully exploiting all operating regions of SiGe HBTs in RF LS operation, the dynamic signal swings exceed "conventional limits" such as BV_{CEO} as well as the V_{CE} range typically used for model parameter extraction. Hence, in addition to a DC verification of the modelcard in operating regions $V_{CE} > BV_{CEO}$ across a wide range of V_{BE}, a thorough LS modelcard verification is of interest.

Fig. 5 depicts power sweep measurements and simulations at fixed fundamental load reflection coefficients in operating points with $V_{CE} > BV_{CEO}$.

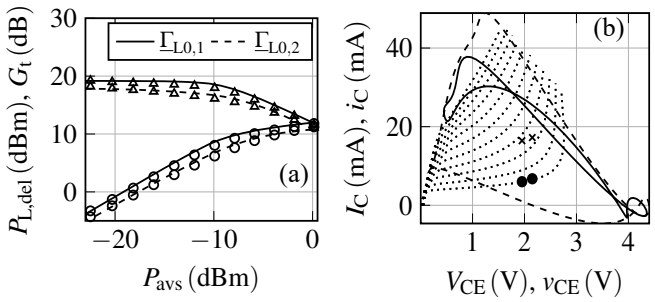

Fig. 5: (a) Power sweep (symbols: measurements; lines: simulations) at $f_0 = 10$ GHz. (b) Simulated load ellipses for $\underline{\Gamma}_{L0,1}$ and $\underline{\Gamma}_{L0,2}$ at $P_{avs} = 0$ dBm superimposed on simulated output characteristics with $V_{BE} = 0.9$ V...1.1 V in steps of 20 mV (dotted lines). Solid lines: $V_{BE} = 0.9$ V, $V_{CE} = 2.2$ V, $\underline{\Gamma}_{L0,1} = 0.45\angle 13.8°$. Dashed lines: $V_{BE} = 0.9$ V, $V_{CE} = 2.0$ V, $\underline{\Gamma}_{L0,2} = 0.63\angle 61.9°$. The filled dots mark the quiescent operating points. The crosses mark the expanded I_C in nonlinear operation. DUT: $b_{E0} = 0.12$ µm, $l_{E0} = 5.15$ µm.

Fig. 6 shows closed constant-power contours obtained from load-pull measurements and corresponding simulations for the fundamental load reflection coefficients $\underline{\Gamma}_{L0}$ depicted by the points scattered across the Smith chart. The innermost constant-power contour indicates the Smith chart area in which maximum power is delivered to the load. The variation of the fundamental load reflection coefficient was performed in a quiescent bias point with $V_{CE} = 2.0$ V > $BV_{CEO} = 1.6$ V at the available powers from the source $P_{avs} = -9.92$ dBm and $P_{avs} = 0.14$ dBm at a fundamental frequency $f_0 = 10$ GHz.

The agreement between the measured and simulated output powers is very good across a wide range of load reflection coefficients $\underline{\Gamma}_{L0}$ as well as available powers from the source P_{avs} despite the fact that the quiescent and the transient CE voltages (significantly) exceed BV_{CEO} and the V_{CE} range typically used for model parameter extraction. Hence, this thorough verification of the carefully calibrated modelcard demonstrates that HICUM/L2 is an excellent means for exploiting extended operating regions of SiGe HBTs and thus for enhancing the transistor performance.

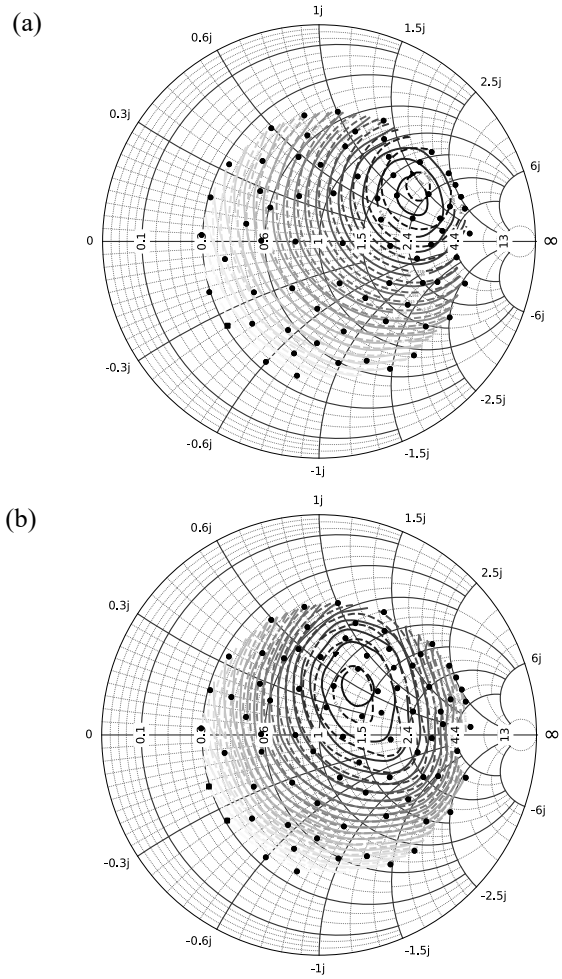

Fig. 6: Constant-power contours obtained from load-pull in the operating point $J_C = 14.5$ mA/µm^2, $V_{BE} = 0.92$ V, $V_{CE} = 2.0$ V, $f_0 = 10$ GHz in dependence on P_{avs} with the contour specifications ($P_{L,del,max}$/dBm, $P_{L,del,min}$/dBm, ΔP_L/dB). The solid contours are based on measurement data, the dashed contours are based on simulation data. (a) $P_{avs} = -9.92$ dBm, measured: (8.71, 1.66, 0.35), simulated: (8.99, 1.64, 0.37); (b) $P_{avs} = 0.14$ dBm, measured: (12.1, 8.23, 0.19), simulated: (11.79, 7.53, 0.21). DUT: $b_{E0} = 0.12$ µm, $l_{E0} = 5.15$ µm.

D. Base current degradation

The static base current injected across the emitter periphery is implemented in HICUM as [5]

$$i_{BEps} = I_{BEpS}\left[\exp\left(\frac{v_{B*E'}}{m_{BEp}V_T}\right) - 1\right] + I_{REpS}\left[\exp\left(\frac{v_{B*E'}}{m_{REp}V_T}\right) - 1\right] \quad (2)$$

with the peripheral BE saturation current I_{BEpS} and current ideality factor m_{BEp} and the peripheral BE recombination satura-

tion current I_{REpS} and current ideality factor m_{REp}. V_T is the thermal voltage. $v_{\mathrm{B*E}}$ is the voltage drop between the peripheral base node B^* and the internal emitter node E′. I_{REpS} is the parameter that is modified in the literature for modeling the degradation-caused low-injection excess base current [3, 4]. The reason is that the interface traps generated at the emitter-base spacer oxide by high-energy charge carriers can be physically related to the recombination saturation current of the peripheral base current [5]. All other parameters in (2) remain unchanged [3, 4].

In the dynamic stress tests [6, 7], RF LS transistor operation with large *dynamic* $i_{\mathrm{C}}(t)$-$v_{\mathrm{CE}}(t)$ swings causes this low-injection excess base current. An increase of I_{REpS} in (2) by two decades enables to reproduce the observed base current degradation, as shown in Fig. 7(a). However, as demonstrated in Fig. 7(b), even this strong increase of I_{REpS} has no impact at all on the RF LS transistor performance and associated figures of merit such as the output power and transducer power gain.

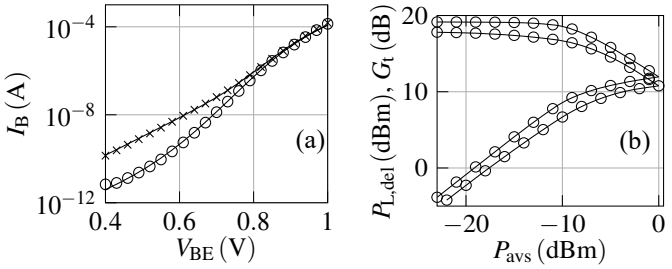

Fig. 7: (a) I_{B} versus V_{BE} at $V_{\mathrm{BC}} = 0$ V measured prior to stress (circles) and at the end of stress phase ac_1 in [6] (crosses) as well as HICUM simulations (lines) with $I_{\mathrm{REpS,0}}$ (initial I_{B} curve) and $I_{\mathrm{REpS,1}}$ (degraded I_{B} curve). (b) LS load-pull simulations with the same conditions as in Fig. 5 but with varying I_{REpS}: (initial) $I_{\mathrm{REpS,0}}$ as in Fig. 5 (circles) and degraded $I_{\mathrm{REpS,1}}$ (lines). $I_{\mathrm{REpS,1}}/I_{\mathrm{REpS,0}} \approx 100$. DUT: $b_{\mathrm{E0}} = 0.12$ µm, $l_{\mathrm{E0}} = 5.15$ µm.

As demonstrated, the low-injection excess base current has practically no impact on the performance of certain RF circuit building blocks, such as power amplifiers, which cause this type of degradation. In other words, the excess base current does not lead to circuit degradation. Calling it degradation causes confusion and prevents circuit designers from exploiting the full performance potential of SiGe HBTs.

E. Static stress tests of metal stacks

Obtaining the transistor admittance parameters requires to deembed the influence of pad and metal connection lines from the measured data. Thus, prior to performing the typical open-short deembedding, it must be verified that the metalization, especially the metal stack connecting the collector and emitter terminal of the DUT to the upper metal layers, does not degrade at the dynamic current densities the transistor is subjected to during stress. The most relevant concern is electromigration in the metal stacks, especially under strongly nonlinear operating conditions which cause high DC and dynamic collector current densities. In [6] the SHORT structure was DC-stressed at $T_{\mathrm{amb}} = 298$ K and no electromigration-caused increase of the metalization resistances was observed. In reality, the die temperature is higher than 298 K due to the self-heating of the transistor and the partial conduction of the heat also into the contact metal. An elevated temperature increases the risk of electromigration in the metal stacks during long-term operation. Thus, another DC stress test of the SHORT structure was performed at the elevated chuck-controlled temperature of $T_{\mathrm{amb}} = 330$ K. The DC conditions of the stress test at $T_{\mathrm{amb}} = 330$ K are specified in Table 1.

Table 1: Summary of the DC conditions of the stress test with the SHORT structure at $T_{\mathrm{amb}} = 330$ K.

Phase	$I_{\mathrm{B,stack}}$	$J_{\mathrm{B,stack}}$	$I_{\mathrm{C,stack}}$	$J_{\mathrm{C,stack}}$
I	5 mA	9.9 mA/µm²	5 mA	9.9 mA/µm²
II	5 mA	9.9 mA/µm²	20 mA	39.6 mA/µm²
III	10 mA	19.8 mA/µm²	30 mA	59.4 mA/µm²
IV	20 mA	39.6 mA/µm²	50 mA	99 mA/µm²

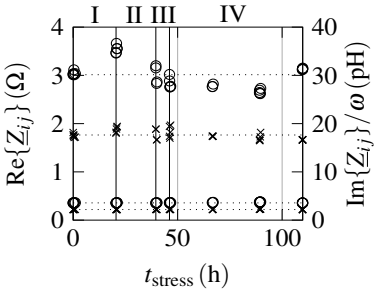

Fig. 8: Periodic measurements of the stress test with the SHORT structure at $T_{\mathrm{amb}} = 330$ K. The lower crosses/circles represent the ohmic/inductive part for $ij = 12$. The upper crosses/circles represent the ohmic/inductive part for $ij = 22$. The dotted horizontal lines represent the respective values measured at $t_{\mathrm{stress}} = 0$.

The DC stress test results are represented in Fig. 8 by the periodically measured metalization resistances and inductances along the metal stack on the collector side. No degradation can be observed in the metalization resistance/inductance from both *(1)* the emitter terminal to the ground contact ($ij = 12$) and *(2)* the RF pad on the collector side along the collector metal stack to the ground contact ($ij = 22$). The very small arbitrary fluctuations in the data in Fig. 8 are measurement uncertainty. Hence, this test delivers further proof that the GSG layout is not damaged, which enables to attribute the measured degradation to the transistor and permits open-short deembedding. Consequently, all admittance parameters shown in the next section have been deembedded.

III. RF RELIABILITY CHARACTERIZATION

A. Consecutive DC and RF stress tests

In the stress test presented below, operating points, available powers from the source and fundamental load reflection coefficients were varied. The stress test consists of five consecutive DC and RF stress phases with the conditions summarized in Table 2. The operating points of the stress phases are shown in Fig. 9. The simulated load ellipses of the RF stress phases are shown in Fig. 10.

Table 2: Summary of the DC and RF stress conditions at f_0 = 10 GHz. DUT with b_{E0} = 0.12 µm, l_{E0} = 5.15 µm.

Phase	Type	OP	$\underline{\Gamma}_{L0}$	P_{avs} (dBm)
I	DC	Q_1	-	-
II	DC	Q_2	-	-
III	AC	Q_3	$0.68\angle 22.5°$	−6.88
IV	AC	Q_3	$0.70\angle -25.5°$	−3.86
V	AC	Q_2	$0.63\angle 9.5°$	+7.15

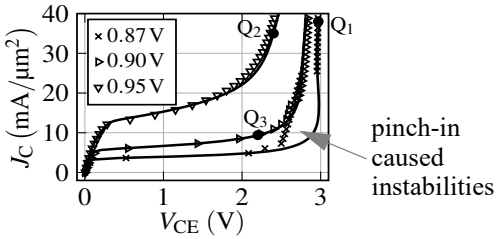

Fig. 9: Output characteristics (forced I_C, sensed V_{CE}) with the quiescent bias points $Q_{1...3}$. Quiescent points: (J_C / (mA/µm^2), V_{BE}/V, V_{CE}/V) = (38, 0.87, 3), (35, 0.95, 2.4), (9.5, 0.9, 2.2). Symbols: measurements; lines: simulations. DUT: b_{E0} = 0.12 µm, l_{E0} = 5.15 µm.

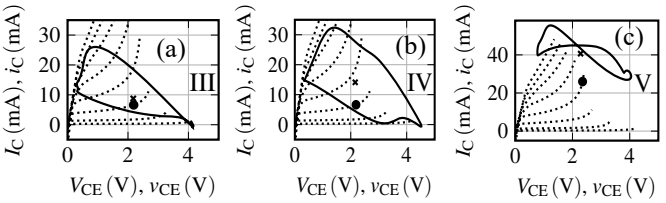

Fig. 10: Simulated dynamic load ellipses (solid lines) for various dynamic stress conditions (with f_0 = 10 GHz) over simulated output characteristics (dotted lines) for V_{BE} = 0.8...1.15 V in steps of 50 mV. The filled dots mark the collector currents of the quiescent bias points. The crosses mark the expanded DC collector currents in non-linear transistor operation. Data of a DUT with b_{E0} = 0.12 µm, l_{E0} = 5.15 µm.

I_B, I_C, Im{$\underline{Y}_{11}$}, and Re{$\underline{Y}_{21}$}, which were periodically measured during short interruptions of the stress, are plotted versus the cumulative stress time t_{stress} in Fig. 11. f_T curves measured before and after stress are depicted in Fig. 12. This stress test demonstrates that SiGe HBTs withstand extreme DC and RF stress conditions. The low-injection excess base current is the only degradation measurable until the end of stress phase IV. The $\underline{Y}$-parameters remain unaffected by the DC and RF stress until the end of phase IV. The stress conditions of phase V represent a transistor breakdown experiment. The quiescent bias J_C = 35 mA/µm^2 at V_{CE} = 2.4 V ($> BV_{CEO}$ = 1.6 V) and P_{avs} = 7.15 dBm cause significant degradation of all $\underline{Y}$-parameters *until the eventual destruction* of the DUT.

The stress conditions of phase V are much more extreme than any RF LS operating conditions a SiGe HBT would encounter in practical circuits. Given the demonstrated robustness of SiGe HBTs, these stress conditions were selected specifically to make significant damage measurable during a reasonable stress time.

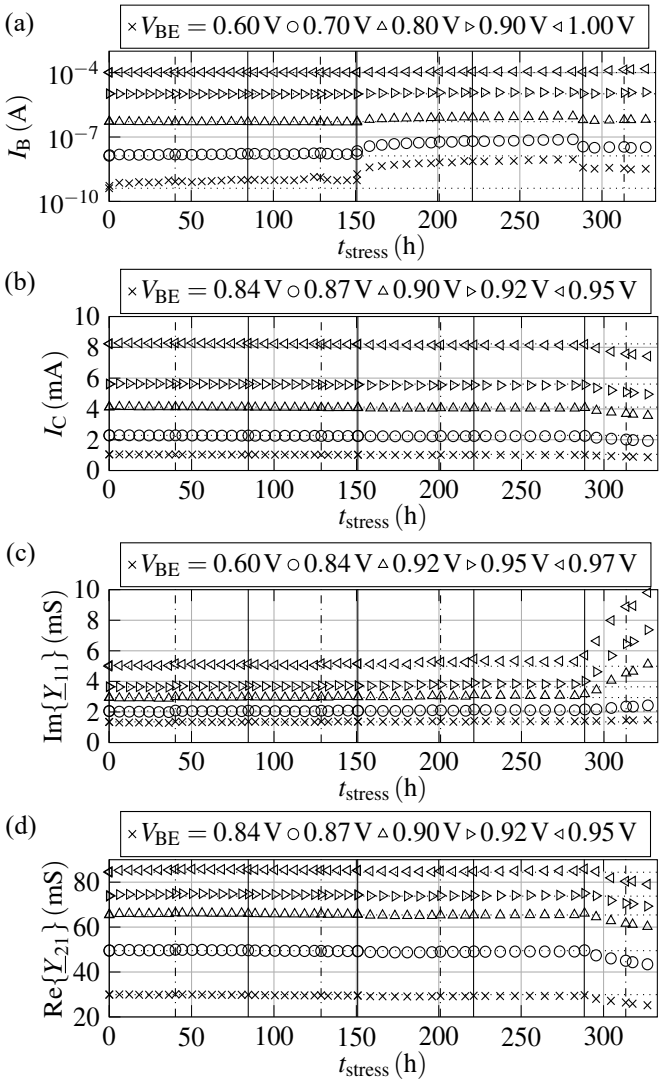

Fig. 11: (a) I_B (b) I_C (c) Im{$\underline{Y}_{11}$} (d) Re{$\underline{Y}_{21}$} measured periodically at V_{CE} = 0.5 V (f_{meas} = 10 GHz) at specific cumulative stress times. The *solid vertical lines* separate the stress phases I - V (from left to right) specified in Table 2. A re-calibration was performed prior to each stress phase. The *dash-dotted vertical lines* mark re-calibrations without a change of the stress conditions. The *dotted horizontal lines* represent the respective values measured prior to the first stress test. DUT: b_{E0} = 0.12 µm, l_{E0} = 5.15 µm.

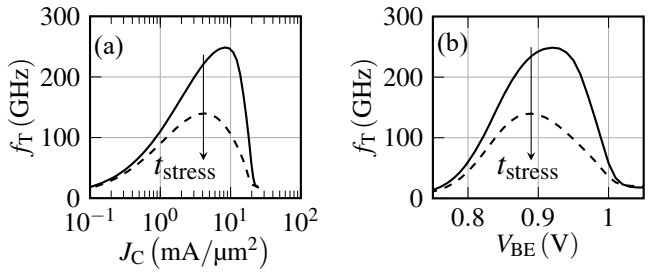

Fig. 12: f_T versus (a) J_C and (b) V_{BE} measured at f_{meas} = 10 GHz, V_{CE} = 0.5 V before the stress test (solid lines) and after t_{stress} = 332.6 h (dashed lines). b_{E0} = 0.12 µm, l_{E0} = 5.15 µm.

This stress test suggests that SiGe HBTs are so robust that their absolute limits are in impractical operating regions. However, there must be some gradual degradation under somewhat less extreme operating conditions. Finding those was the next task. Finally, the extreme stress conditions of phase V provided the insight that in highly non-linear HBT operation the static J_C expands into operating regions where electro-thermal breakdown causes significant degradation and eventually device destruction. Using the potentially damaging effects of highly non-linear HBT operation motivates the study commenced in [7] and continued below.

B. RF stress tests with varying emitter widths

The RF stress methodology of this *non-destructive* stress test commenced in [7] is to fix the fundamental load reflection coefficient $\underline{\Gamma}_{L0}$ in a quiescent bias point with a lower, realistic J_C at $V_{CE} > BV_{CEO}$ and to gradually increase P_{avs}, thereby gradually driving the transistor into gain compression and expanding the static I_C. This approach permits to identify the absolute limits of RF LS transistor operation and the onset of gradual stress-related changes in the periodically measured transistor characteristics.

The RF stress methodology is applied to three SiGe HBTs with the identical emitter length $l_{E0} = 2.65$ µm but different emitter widths b_{E0}/µm = {0.12, 0.17, 0.25} in the same quiescent $J_C = 18$ mA/µm^2 at $V_{CE} = 2.0$ V. The $\underline{\Gamma}_{L0}$ of each DUT was obtained by means of load-pull measurements in the given quiescent bias point and $f_0 = 10$ GHz, $P_{avs} = -4.88$ dBm. The selected $\underline{\Gamma}_{L0}$ cause the transducer power gain of the three devices to compress at a comparable P_{avs}, leading to the onset of the J_C increase at approximately the same P_{avs}. Fig. 13 shows a power sweep as well as simulated load ellipses for the DUT with $b_{E0} = 0.12$ µm, $l_{E0} = 2.65$ µm. These RF stress conditions (up to $P_{avs} \approx 5$ dBm) cause only the low-injection excess base current but no degradation of the $\underline{Y}$-parameters. Fig. 14(a) shows that in hard output power saturation the smallest device has to withstand the highest output power density. Fig. 14(b) depicts that the static J_C expands significantly as the gain compresses. The P_{avs}, with which the three devices are stressed, are listed in Table 3, Table 4 and Table 5.

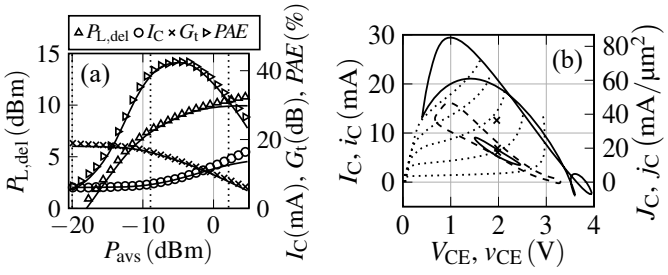

Fig. 13: (a) Power sweep (symbols: measurements; lines: simulations) with $f_0 = 10$ GHz, $\underline{\Gamma}_{L0} = 0.51\angle 13.2°$, $J_C = 18$ mA/µm^2, $V_{CE} = 2$ V (b) simulated load ellipses at P_{avs}/dBm = {-20, -8.92, 2.13} superimposed on simulated output characteristics with $V_{BE} = 0.86$ V...1.1 V in steps of 60 mV (dotted lines). The crosses mark the static I_C. $b_{E0} = 0.12$ µm, $l_{E0} = 2.65$ µm.

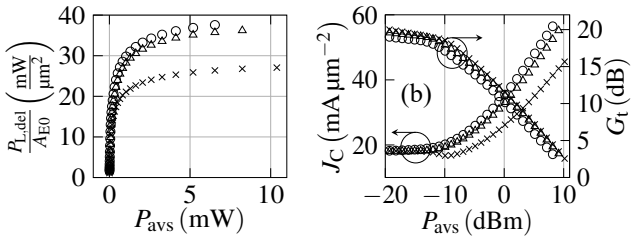

Fig. 14: (a) $P_{L,del}/A_{E0}$ (b) J_C and G_t versus P_{avs} with the quiescent bias $J_C = 18$ mA/µm^2, $V_{CE} = 2$ V with (b_{E0}, $\underline{\Gamma}_{L0}$): (0.12 µm, $0.51\angle 13.2°$) (circles), (0.17 µm, $0.42\angle 26.2°$) (triangles), (0.25 µm, $0.42\angle 26.2°$) (crosses). $l_{E0} = 2.65$ µm.

Table 3: Stress conditions, DUT I ($b_{E0} = 0.12$ µm, $l_{E0} = 2.65$ µm): $J_C = 18$ mA/µm^2, $V_{CE} = 2$ V, $f_0 = 10$ GHz, $\underline{\Gamma}_{L0} = 0.51\angle 13.2°$.

Phase	Type	P_{avs} (dBm)
I	DC	-
II	AC	−8.92
III	AC	2.13
IV	AC	5.13
V	AC	8.13

Table 4: Stress conditions, DUT II ($b_{E0} = 0.17$ µm, $l_{E0} = 2.65$ µm): $J_C = 18$ mA/µm^2, $V_{CE} = 2$ V, $f_0 = 10$ GHz, $\underline{\Gamma}_{L0} = 0.42\angle 26.2°$.

Phase	Type	P_{avs} (dBm)
I	AC	−13.00
II	AC	−10.96
III	AC	−8.92
IV	AC	2.13
V	AC	5.13
VI	AC	8.13
VII	AC	9.13

Table 5: Stress cond., DUT III ($b_{E0} = 0.25$ µm, $l_{E0} = 2.65$ µm): $J_C = 18$ mA/µm^2, $V_{CE} = 2$ V, $f_0 = 10$ GHz, $\underline{\Gamma}_{L0} = 0.42\angle 26.2°$.

Phase	Type	P_{avs} (dBm)
I	AC	−8.92
II	AC	2.13
III	AC	5.13
IV	AC	8.13
V	AC	10.13

Fig. 15(a) and (b) show the periodically measured zero-bias depletion capacitances C_{jE0} and C_{jC0}, respectively. C_{jC0} exhibits a practically perfect measurement reproducibility. C_{jE0} is more difficult to measure because of its larger measurement uncertainty (±1fF) to which the irregular fluctuations shown in Fig. 15(a) can be attributed. Hence, the zero-bias depletion capacitances do not degrade. The same conclusion is true for the test [6] described in section III.*A* (plots not shown for brevity).

Fig. 15(c) depicts the relative changes of Re{$\underline{Z}_{22}$} and Re{$\underline{Z}_{12}$}. The most critical series resistances in the CE path R_E and R_{Cx} can be extracted from small-signal measurements. At a very large forward bias (here $V_{BE} = 1.22$ V) and $V_{CE} = 0$ V, the internal conductances and capacitances can be neglected and the $\underline{Z}$-parameters are dominated by the series resistances R_E of the emitter and R_{Cx} of the external collector [11, 12]. Hence, Re{$\underline{Z}_{12}$} ≈ R_E and Re{$\underline{Z}_{22}$} ≈ $R_E + R_{Cx}$. Regardless of

the particular method used to extract the series resistances from $\underline{Z}$-parameters, of primary importance for this work is the degradation-related change of the measured $\underline{Z}$-parameters. As demonstrated in Fig. 15(c), the changes in $\mathrm{Re}\{\underline{Z}_{22}\}$ and $\mathrm{Re}\{\underline{Z}_{12}\}$ are irregular and smaller than 5 %. This falls within the measurement uncertainty. Hence, neither R_E nor R_Cx degrade. The same conclusion is true for the test [6] described in section III.*A* (plots not shown for brevity).

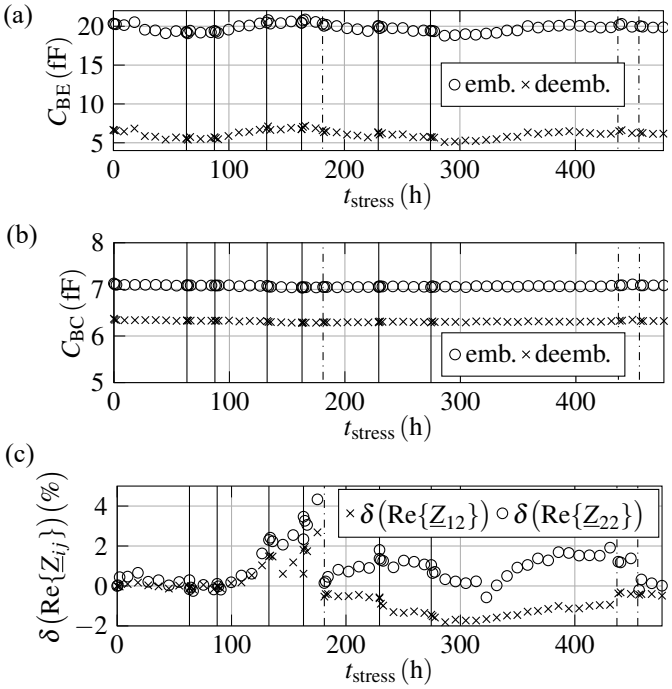

Fig. 15: (a) C_BE at V_BE = 0 V, (b) C_BC at V_BC = 0 V and V_CE = 0.5 V, f_meas = 10 GHz before and after deembedding versus t_stress. (c) Relative changes with respect to the pre-stress measurements: $\delta(\mathrm{Re}\{\underline{Z}_{12}\})$ and $\delta(\mathrm{Re}\{\underline{Z}_{22}\})$ versus t_stress at V_BE = 1.22 V, V_CE = 0 V and f_meas = 10 GHz. The *solid vertical lines* separate the stress phases I - VII (from left to right) specified in Table 4 for the DUT with b_E0 = 0.17 µm, l_E0 = 2.65 µm. *Dash-dotted vertical lines*: re-calibrations.

The periodically measured I_B, I_C, $\mathrm{Im}\{\underline{Y}_{11}\}$, and $\mathrm{Re}\{\underline{Y}_{21}\}$ are plotted over the cumulative t_stress in Fig. 16. The I_B versus t_stress of the two stress tests shown in Fig. 11(a) and Fig. 16(a) have a similar degradation behavior. The most significant stress-related increase is observable at low injection levels. The $\mathrm{Im}\{\underline{Y}_{11}\}$ versus t_stress of the two stress tests shown in Fig. 11(c) and Fig. 16(c) also have a similar behavior. At V_BE = 0.6 V, $\mathrm{Im}\{\underline{Y}_{11}\}$ is mainly composed of the BE and BC depletion capacitances and does not exhibit changes larger than the measurement uncertainty. Only at high V_BE where $\mathrm{Im}\{\underline{Y}_{11}\}$ is dominated by the BE diffusion capacitance, a significant increase of $\mathrm{Im}\{\underline{Y}_{11}\}$ can be observed in both tests.

The collector current I_C in Fig. 16(b) increases with t_stress for all injection levels, but the increase at low injection is relatively larger. This can be better seen from $\mathrm{Re}\{\underline{Y}_{21}\}$ in Fig. 16(d) which increases at low and decreases at high injection levels. This is in contrast to the *destructive* device test in Fig. 11(d), where $\mathrm{Re}\{\underline{Y}_{21}\}$ decreases at all injection levels until device destruction.

The stress-related changes in I_C and $\mathrm{Re}\{\underline{Y}_{21}\}$ affect the measured f_T curves. The f_T curve measured prior to device *destruction* shown in Fig. 12 is significantly decreased due to stress, whereas f_T measured at the end of the *non-destructive* test (cf. Fig. 16) shown in Fig. 17 is horizontally shifted when plotted over V_BE and practically unchanged when plotted over J_C. This $f_\mathrm{T}(V_\mathrm{BE})$ and $f_\mathrm{T}(J_\mathrm{C})$ behavior resulting at the end of the *non-destructive* stress test suggests that, in particular, the $I_\mathrm{C}(V_\mathrm{CE})$ relation is modified due to extremely high RF LS stress.

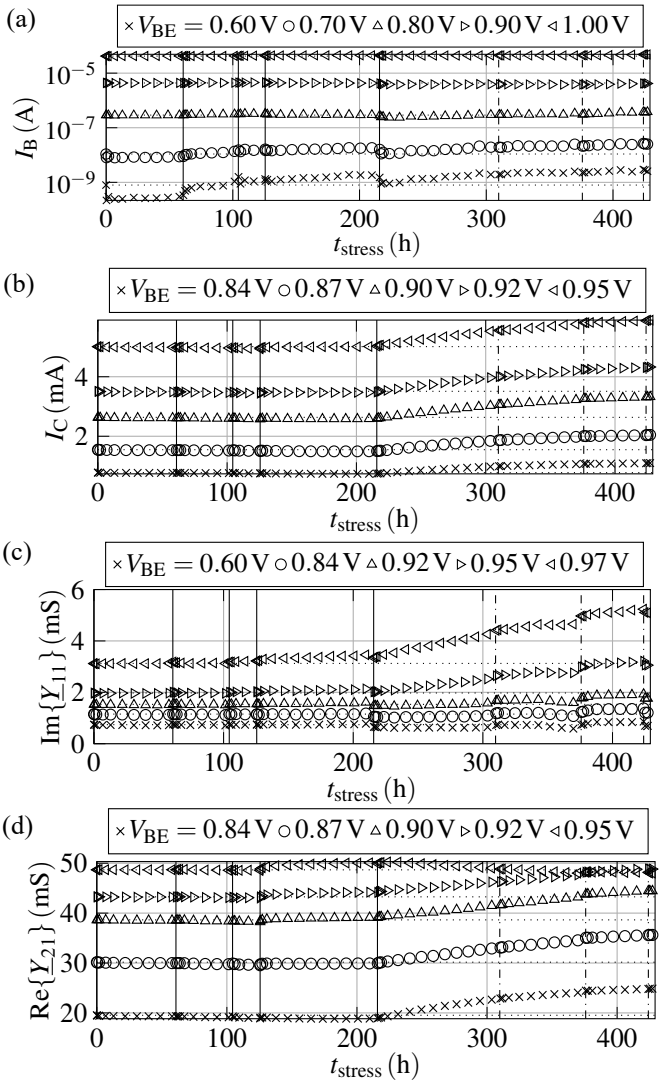

Fig. 16: (a) I_B (b) I_C (c) $\mathrm{Im}\{\underline{Y}_{11}\}$ (d) $\mathrm{Re}\{\underline{Y}_{21}\}$ measured at V_CE = 0.5 V (f_meas = 10 GHz) at specific cumulative stress times. The *solid vertical lines* separate the stress phases I - V (from left to right) specified in Table 3. A re-calibration was performed prior to each stress phase. *Dash-dotted vertical lines*: re-calibrations. *Dotted horizontal lines*: pre-stress measurements. DUT with b_E0 = 0.12 µm, l_E0 = 2.65 µm.

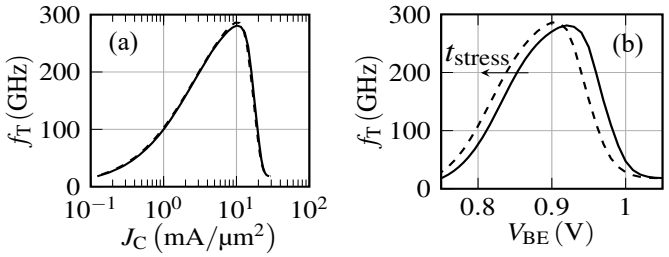

Fig. 17: f_{T} versus (a) J_{C} and (b) V_{BE} measured at f_{meas} = 10 GHz, V_{CE} = 0.5 V before the stress test (solid lines) and after t_{stress} = 429.2 h (dashed lines). b_{E0} = 0.12 μm, l_{E0} = 2.65 μm.

Similar trends in the I_{C} versus t_{stress} of the *non-destructive* stress test can be observed for the DUTs with different emitter widths, as shown in Fig. 18. For all DUTs the low-injection I_{C} is most significantly increased until it eventually saturates. This I_{C} degradation behavior suggests to investigate the width scaling behavior of I_{C} before stress and after stress using the saturated I_{C} values. The stress-related vertical shift of the width scaling line of $I_{\mathrm{C}}/A_{\mathrm{E0}}$ given in Fig. 19 indicates that the measured degradation is predominantly area-related. The systematic vertical shift of the scaling lines of I_{C} and of the diffusion capacitance, represented in Fig. 19 by the length-normalized $\mathrm{Im}\{\underline{Y}_{11}\}$, may be attributed to a change in material parameters possibly due to stress-related lattice strain.

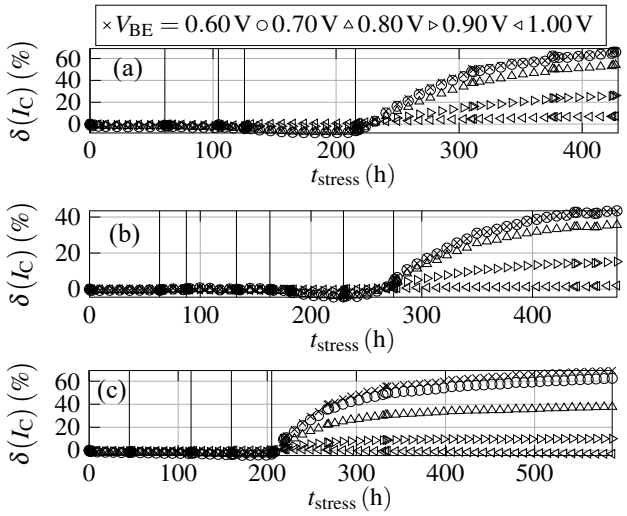

Fig. 18: Relative changes with respect to the pre-stress measurements: $\delta(I_{\mathrm{C}})$ versus t_{stress} in selected bias points for the emitter widths b_{E0} (a) 0.12 μm (b) 0.17 μm (c) 0.25 μm. l_{E0} = 2.65 μm. The *solid vertical lines* separate the stress phases (from left to right) specified in (a) Table 3 (b) Table 4 (c) Table 5.

IV. Summary

Concepts relevant to long-term RF reliability have been discussed. The robustness of SiGe HBTs has been demonstrated by RF stress tests with different RF large-signal operating conditions far beyond static operating limits. Only extremely nonlinear large-signal HBT operation is found to degrade the DC and RF characteristics, indicating excellent long-term reliability of SiGe HBTs. It is shown that neither depletion capacitances nor series resistances degrade. RF stress tests of HBTs with different emitter widths indicate that the systematically measured degradation is area-related and can be attributed to minority carrier transport and storage. Further investigations regarding the exact physical reason of this degradation are necessary.

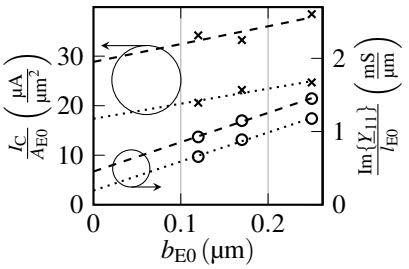

Fig. 19: Width scaling of the low-injection (V_{BE} = 0.7 V) $I_{\mathrm{C}}/A_{\mathrm{E0}}$ (crosses) and of the high-injection (V_{BE} = 0.94 V) $\mathrm{Im}\{\underline{Y}_{11}\}/l_{\mathrm{E0}}$ (circles) before the RF stress tests (dotted lines) and after approximately 280 h of RF stress during the last degradation-causing stress phase (dashed lines). V_{CE} = 0.5 V.

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