Post-print version (generated on 22.12.2022)
This publication is available at:
https://tu-dresden.de/ing/elektrotechnik/iee/ge/die-professur/beschaeftigte/richard-schroedter

SPICE Compact Model for an Analog Switching Niobium Oxide Memristor

Richard Schroedter*, Ahmet Samil Demirkol*, Alon Ascoli*, Ronald Tetzlaff*,
Eter Mgeladze†, Melanie Herzig†, Stefan Slesazeck†, Thomas Mikolajick†‡

*Chair of Fundamentals of Electrical Engineering, Technische Universität Dresden, Dresden, Germany
†NaMLab gGmbH, Dresden, Germany
‡Chair of Nanoelectronics, Technische Universität Dresden, Dresden, Germany

***Abstract*—In this paper, we present a compact SPICE model of an analog switching memristive device based on niobium oxide and investigate the functionality of the same as a synapse element through its compact model by utilizing it in a simulation of an 8x8 resistive crossbar array. Considering especially the von Neumann bottleneck for neural network computing tasks, memristive crossbar arrays offer a potential in-memory computing solution performing highly parallel matrix-vector multiplication and reducing the energy consumption. In particular, multi-level switching memristive devices with intrinsic self-compliance are predestined for crossbar operations. Based on experimental results of a bi-layer Ti/Al_2O_3/Nb_2O_5/Ti stack, a compact physical model was recently derived, assuming an underlying Poole-Frenkel emission mechanism. High model accuracy in terms of I-V behaviors, dynamic route map and power exponent plots were demonstrated by fitting the nonlinear I-V relation and the state function to measurement data, verifying analog gradual switching for the voltage driven extended memristor. In this paper the SPICE implementation for the core memductance accompanied by a parallel and series resistor is introduced and its application for sense analysis via analog and multi-memristor circuit exploitation is presented. Adopting the SPICE model, the switching dynamics is investigated and discussed for performing synaptic potentiation and depression behavior in a potential crossbar application.**

***Index Terms*—Compact physical SPICE model, analog gradual switching niobium oxide memristor, bi-layer Al2O3/Nb2O5 stack, Poole-Frenkel emission, synaptic memristive behavior for crossbar application**

I. Introduction

In-memory computing based on analog switching memristive crossbar arrays is highly attractive for implementing beyond classical von Neumann architectures used in neuromorphic computing applications. Artificial Neural Networks (ANN) require a huge amount of data processing based on matrix-vector multiplications, which can be accelerated using analog memristive computing through Kirchhoff's law for the weighted summation of currents with low energy consumption. Many memristive switching nanodevices have been studied [1], while metal-insulator-metal (MIM) stacks with multiple oxide layers can offer beneficial features for an efficient crossbar application like an intrinsic current compliance and high nonlinearity for selector operation [2], [3]. While previous work on niobium oxide memristive devices at NaMLab gGmbH has shown versatile characteristics like filamentary bipolar resistive threshold switching [4] and local activity for oscillator or neuristor applications [5], the MIM stack is now optimized for robust analog multi-state switching behavior [6], [7]. Beside studies on physical mechanisms and experimental verification, the availability of compact models is essential to enable a robust simulation of the devices validating the applicability of them in crossbars for accelerating neural network computing. SPICE models enable simple access to verification and analysis of the memristive behavior [8] and can be extended to full crossbar simulation performing inference operation of ANNs [9]. Prior work modeled the thermally induced abrupt threshold switching behavior in NbO_x devices from NaMLab gGmbH [10]. Our recently proposed compact modeling approach [11] for the bi-layer analog switching in a modified niobium memristor showed high agreement with Poole-Frenkel emission mechanism, but was missing the synaptic simulation as well as a SPICE implementation. In this paper we provide a novel compact SPICE model for an analog switching memristor based on a bi-layer Ti/Al_2O_3/Nb_2O_5/Ti stack and demonstrate its synaptic behavior and applicability in the simulation of an 8×8 crossbar array.

This work was supported by the German Research Foundation (DFG) under the Project No. 441898364.

II. Analog switching memristor

The presented modeling is based on an interfacial switching memristor device fabricated at NaMLab gGmbH. The memristor is fabricated as a bi-layer stack of 2 nm Al_2O_3 and 10 nm stoichiometric Nb_2O_5 sandwiched between 30 nm Ti electrodes, see inset in Fig. 2. Based on 2×1 cm Si coupons with 1.5 nm SiO_2 and sputtered Ti bottom electrodes (BE), the Al_2O_3 layer is sputtered from an Al_2O_3 target and the Nb_2O_5 layer is reactively sputtered from metallic Nb target at 5×10^{-3} mbar and a mass flow ratio of Ar to O_2 of 3.75. Circular top electrodes (TE) with 50 µm diameter are comprised of 30 nm Ti and 30 nm Pt. All fabrication is performed at room temperature where the layer thicknesses are monitored via X-Ray reflectometry and ellipsometry. For both layers the relative permittivities of 28 for Nb_2O_5 and 8 for Al_2O_3 have been deduced from the electrical measurement data, leading to a total permittivity of 19.76 for the layer thicknesses of

Post-print version of the article: R. Schroedter, A. S. Demirkol, A. Ascoli, R. Tetzlaff, E. Mgeladze, M. Herzig, S. Slesazeck, T. Mikolajick, "SPICE Compact Model for an Analog Switching Niobium Oxide Memristor", *2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, Germany*, pp. 1-4, 2022.
DOI: 10.1109/MOCAST54814.2022.9837726
© © 2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.
For further information contact: richard.schroedter[at]tu-dresden.de, ORCID: 0000-0003-3259-4571

Post-print version (generated on 22.12.2022)
This publication is available at:
https://tu-dresden.de/ing/elektrotechnik/iee/ge/die-professur/beschaeftigte/richard-schroedter

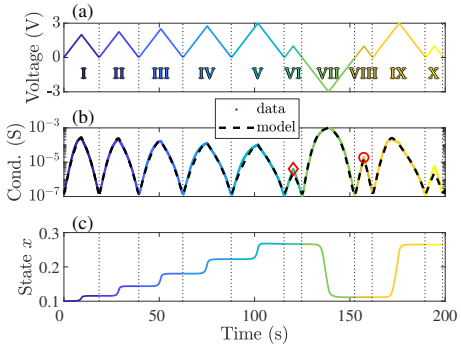

Fig. 1: Quasi-static characterization: (a) input voltage sequence, (b) conductance plot of measurement data as points applying $G = I/V$ with model as dashed line, (c) and state evolution.

10 nm and 2 nm respectively. The MIM stack was electrically characterized by current-voltage (I-V) measurements with the Keithley 4200 measurement system (Tektronix Inc., US) at ambient temperature. In extension to previous studies [6], [7], the MIM stack was optimized to perform analog switching showing gradual reset, and to be utilized as synaptic devices in crossbar arrays. In contrast to a filamentary forming step, the device is activated by a single $-4\,\mathrm{V}$ setting step, which switches resistance from above 500 MΩ down to 8 MΩ around 0 V, where it is operational afterwards. Fig. 1 shows the result from the quasi-static I-V measurement over time. The voltage was swept in a triangular waveform with gradually increasing amplitude resulting in an analog switching behavior of the memristor device, which was afterwards set (-3V) and reset (3V) completely. The resistance $R = V/I$ demonstrates memory behavior in Fig. 2, i.e. the non-volatile resistance level at 1 V was decreased from 247 kΩ (4 µS) after gradual reset (red diamond in Fig. 1 (b)) to 53 kΩ (19 µS) after set (red circle in Fig. 1 (b)). For the analysis of switching kinetics the device was tested applying a sequence of set ($-3\,\mathrm{V}$) or reset (3 V) voltage pulses, and intermediate readings at 1 V, while sweeping up the set or reset pulse length by four orders of magnitudes from 100 µs to 1 s. Different conduction mechanisms are known to be present in NbO_x devices [2], [3], [12], while previous works [4], [11] confirmed good agreement between the I-V characteristics and Poole-Frenkel emission[1]

$$I_{\mathrm{PF}}(V) = V \cdot A \exp\left(B\sqrt{V}\right), \tag{1}$$

which is also consistent with the extended memristor theory, where is $G(x, V_\mathrm{m} = 0) \neq \infty$ [13].

III. Modeling and SPICE implementation

The graphical approach from Acha et al. [14] provides an equivalent circuit, based on the inclusion of a parallel

[1]The coefficients in (1) are defined $A = q\mu N_C d^{-1} \exp(-q\Phi/(k_\mathrm{B}T))$ and $B = \sqrt{q^3}/(\sqrt{\pi\varepsilon d}\, k_\mathrm{B}T)$, where denotes q elementary charge, μ electron mobility, N_C density of states in conduction band, Φ trap barrier height, ε permittivity, k_B Boltzmann constant, T ambient temperature and d dielectric thickness [3], [11].

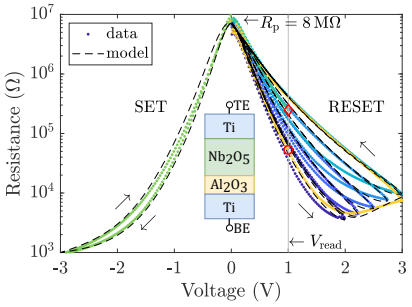

Fig. 2: Resistance $R = V/I$ of measurement (cf. Fig 1) and model as dashed line; inset illustrates bi-layer $Ti/Al_2O_3/Nb_2O_5/Ti$ stack.

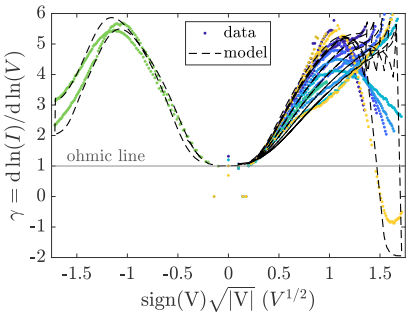

Fig. 3: Power exponent representation $\gamma = \mathrm{d}\ln(I)/\mathrm{d}\ln(V)$ of measurement (cf. Fig 1) as points and model as dashed line

resistor R_p, which is related to the non-switching part of the bi-layer stack, a series resistor R_s, which can be related to residual filament resistance or to contact resistances [11], and a core memristor, which was adopted on the derivation of a circuit-theoretic model for our device. The power exponent $\gamma = \mathrm{d}\ln(I)/\mathrm{d}\ln(V)$, given in Fig. 3, starts on the ohmic line $\gamma = 1$ for small voltages, largely increases up to ($\gamma = 6$), and also reaches negative $\gamma = -1$ values (cycle IX in Fig. 1). The overall memristor circuit model, as depicted in Fig. 4b, leads to the equations for the total current I and voltage V:

$$I = I_\mathrm{m} + \frac{V_\mathrm{m}}{R_\mathrm{p}}, \quad \text{and} \quad V_\mathrm{m} = V - IR_\mathrm{s}. \tag{2}$$

The non-volatile analog switching device is modeled as an extended memristor [13], where the I-V relation of the core memristor and its dynamic equation for the state x are

$$I_\mathrm{m} = G(x, V_\mathrm{m}) \cdot V_\mathrm{m}, \quad \text{and} \quad \frac{\mathrm{d}x}{\mathrm{d}t} = f(x, V_\mathrm{m}). \tag{3}$$

The state variable x is assumed to be mainly dependent on the permittivity change (as proposed in [11]), and only mildly on the electron mobility, leading to the memductance model for the core memristor as:

$$G(x, V_\mathrm{m}) = A_\mathrm{r}\, x \exp\left(B_\mathrm{r}\, \mathrm{sign}(V_\mathrm{m}) \sqrt{\frac{|V_\mathrm{m}|}{x}}\right) + A_\mathrm{s}\, x \exp\left(-B_\mathrm{s}\, \mathrm{sign}(V_\mathrm{m}) \sqrt{|V_\mathrm{m}|}\right). \tag{4}$$

Post-print version of the article: R. Schroedter, A. S. Demirkol, A. Ascoli, R. Tetzlaff, E. Mgeladze, M. Herzig, S. Slesazeck, T. Mikolajick, "SPICE Compact Model for an Analog Switching Niobium Oxide Memristor", *2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, Germany*, pp. 1-4, 2022.
DOI: 10.1109/MOCAST54814.2022.9837726
© © 2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.
For further information contact: richard.schroedter[at]tu-dresden.de, ORCID: 0000-0003-3259-4571

Post-print version (generated on 22.12.2022)
This publication is available at:
https://tu-dresden.de/ing/elektrotechnik/iee/ge/die-professur/beschaeftigte/richard-schroedter

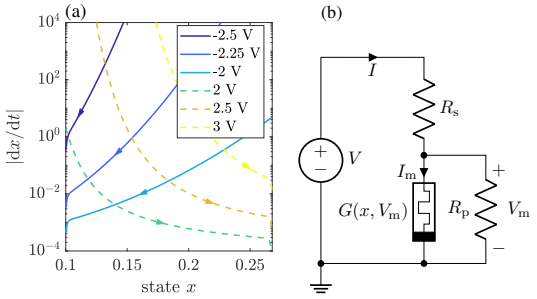

Fig. 4: (a) Dynamic Route Map (DRM) in absolute y-axis log scale and (b) overall memristor circuit-theoretic model

The memductance (4) is modeled by two exponential terms to capture its different behavior for negative and positive input voltage individually, following Poole-Frenkel equation (1). Note that, only the positive term (reset) in (4) shows state dependency of the exponential argument, since a small memory windows was observed in the set branch of the quasi-static I-V curve (cf. Fig. 2).

Considering the state dynamic equation, an exponential dependency of the evolution function of the current I_m through the core memristor is assumed; an approach also found in literature [8], [11], [15]. After a detailed analysis of the measurement data, the state variable was introduced in the argument of each of the exponents, leading to

$$\frac{dx}{dt} = c_1\left[\exp(c_2\, x\, I_m + w_{off}(x)) - \exp(-c_3\, x\, I_m + w_{on}(x))\right], \tag{5}$$

with the fitting constants c_1, c_2 and c_3, and considering the two window functions, inspired by [8], as upper state limit x_{off} and the lower state limit x_{on}:

$$w_{off}(x) = -\exp\left[(x - x_{off})\, w_c\right], \tag{6}$$
$$w_{on}(x) = -\exp\left[(x_{on} - x)\, w_c\right]. \tag{7}$$

Inserting (3) and (4) into (5), it can be seen, that the voltage terms $\exp(B_{s,r}\sqrt{|V_m|})$ dominate the state change, as visualized through the DRM in Fig. 4a. Iterative fitting of the model parameters introduced in (4) and (5) to the measurement data set was performed in Matlab solving the implicit equations in (2). All constants are further provided in the SPICE code given in Fig. 5. The fitting accuracy in reproducing the quasi-static I-V measurement in Fig. 2 is found to be better than $R^2 = 0.997$. During the parameter fit optimization the initial state $x_0 = 0.1$ was kept constant, and as a result the state was constraint to be at all times between $x_{on} = x_0$ and $x_{off} = 0.284$. The large parallel resistance R_p was identified to be $8\,\mathrm{M\Omega}$ (cf. Fig. 2), while the series resistance was fitted to $R_s = 278\,\Omega$. The SPICE implementation for the core memristor with memductance $G(x, V_m)$ is given in Fig. 5, while for the overall circuit-theoretic model of Fig. 4b resistances R_p and R_s need to be included in each simulation

```
* Namlab analog core memristor
* Author: Richard Schroedter, April 2022
* Connections:
*   TE: Top electrode
*   BE: Bottom electrode
*   SV: State variable for plot
.SUBCKT MEM_NAMLAB_CORE TE BE SV

.params Ar=4.7447e-8 As=1.1253e-8 Br=2.6831 Bs=9.3348
+ c1=2.9457e-4 c2=57414 c3=11103 wc=1000 xon=0.1 xoff=0.284

* Function G(x,Vm) - Core Memductance
.func G(x,Vm)=Ar*x*exp(Br*sgn(Vm)*sqrt(abs(Vm)/x))+
+ As*x*exp(-Bs*sgn(Vm)*sqrt(abs(Vm)))

* Function w(x) - Window function
.func win_off(x) = -exp((x-xoff)*wc)
.func win_on(x)  = -exp(-(x-xon)*wc)

* Function F(Vm,x) - State equation
.func F(Vm,x)=c1*(exp(c2*x*Vm*G(x,Vm)+win_off(x))-
+ exp(-c3*x*Vm*G(x,Vm)+win_on(x)))

* Circuit to determine state variable dx/dt = F(Vm,x)
Cx SV 0 {1}
.ic V(SV) = {x0}
Gx 0 SV value = {F(V(TE,BE),V(SV,0))}

* Current source for memristor IV response
Gmem TE BE value={V(TE,BE)*G(V(SV,0),V(TE,BE))}

.ENDS MEM_NAMLAB_CORE
```

Fig. 5: SPICE implementation of core memristor $G(x, V_m)$. For the simulation of the overall memristor, the linear resistors R_s and R_p are added as depicted in Fig. 4b. [Link to code on GitHub]

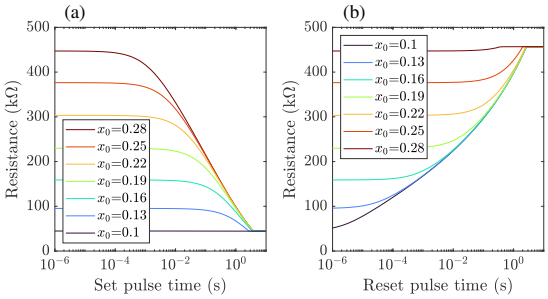

Fig. 6: Resistance versus pulse time for overall memristor model of Fig. 4b: (a) Set dynamics at $-3\,\mathrm{V}$ from initial state x_0 of 0.284 and (b) Reset dynamics at $3\,\mathrm{V}$ starting from initial state x_0 of 0.1; Reads are done at $1\,\mathrm{V}$.

set-up. The state derivative function is implemented in SPICE with a capacitor and a controlled current source [16].

IV. Synaptic Functionality and Crossbar Simulation

The proposed compact memristor model is investigated for storing synaptic weights of a neural network in a crossbar structure. Essentially, the memristor state dynamics are visualized for set and reset pulses under various initial conditions in Fig. 6, verifying the gradual state change depending on the pulse length. Similarly, Fig. 7 demonstrates the incremental and decremental memristor conductance change labeled as potentiation and depression through the application of 100 pulses with an amplitude of -3V for potentiation and 2.7 V

Post-print version of the article: R. Schroedter, A. S. Demirkol, A. Ascoli, R. Tetzlaff, E. Mgeladze, M. Herzig, S. Slesazeck, T. Mikolajick, "SPICE Compact Model for an Analog Switching Niobium Oxide Memristor", *2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, Germany*, pp. 1-4, 2022.
DOI: 10.1109/MOCAST54814.2022.9837726
© © 2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.
For further information contact: richard.schroedter[at]tu-dresden.de, ORCID: 0000-0003-3259-4571

Post-print version (generated on 22.12.2022)
This publication is available at:
https://tu-dresden.de/ing/elektrotechnik/iee/ge/die-professur/beschaeftigte/richard-schroedter

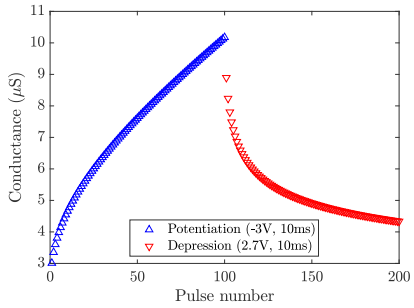

Fig. 7: Memristor conductance under potentiation at $-3\,\mathrm{V}$ and depression at $2.7\,\mathrm{V}$ input pulses of length $10\,\mathrm{ms}$ and reads at $1\,\mathrm{V}$ were used.

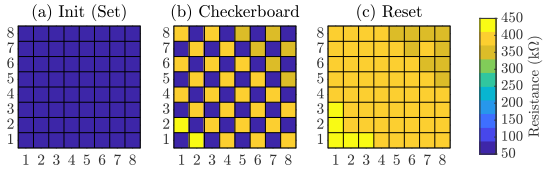

Fig. 8: Simulation result for an 8×8 1R crossbar performed in Matlab/Simulink: (a) initial values of all resistances with fully set core memristors, (b) checkerboard after two steps of a $V_{\mathrm{write}}/2$ biasing scheme applied to form non-adjacent memristor in each row using $3\,\mathrm{V}$-high $2\,\mathrm{s}$-long programming pulses, and (c) full reset crossbar array after applying the same two steps to the earlier-unselected memristors.

for depression, applying a fixed pulse width of $10\,\mathrm{ms}$. The proposed compact model was utilized to test the applicability of the memristor in a 1R passive crossbar configuration without the need for select transistors. For this purpose, we have simulated an 8×8 resistive crossbar in Matlab/Simulink with a wire resistance of $10\,\Omega$ between each device. A simulation conducted in Matlab/Simulink was performed using a $V_{\mathrm{write}}/2$ biasing scheme [16], as shown in Fig. 8, successfully realizing a checkerboard of cell resistances $R_{\mathrm{cell}} = R_{\mathrm{s}} + 1/[G(x, V_{\mathrm{read}}) + 1/R_{\mathrm{p}}]$. A small gradient of resistance can be observed in the right most plot of Fig. 8, while this wire resistance related artifact can be easily removed by increasing the writing time for the devices located in a certain region of the crossbar array.

In summary, the simulation results demonstrate that, the presented compact model of a niobium oxide memristive device, featuring analog switching, is applicable for the design of crossbar arrays implementing matrix-vector multiplication in neural network hardware accelerators, as well as other similar memristive circuits.

V. Conclusion

Based on quasi-static I-V and dynamic pulse measurements as well as further recent investigations [11], a compact model for an Al_2O_3/Nb_2O_5 device was derived that exhibits a high modeling accuracy and is particularly suitable for simulating crossbar applications. The analog switching device characteristics were studied in detail considering a setup consisting of parallel and series resistor parasitic beside the core memristor. A compact SPICE model implementation was first presented and then utilized to explore the gradual switching behavior of the memristor for synaptic potentiation and depression modeling. The circuit model of the overall device was employed finally to verify the proper programmability of an 8×8 1R crossbar arrays, which paves the way for further analysis of its application in hardware platforms for in-memory computing paradigms and may also guide an ad hoc optimization of the bi-layer stack.

References

[1] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges," *Adv. Mat.*, vol. 21, no. 25-26, pp. 2632–2663, 2009.

[2] M. Hansen, M. Ziegler, L. Kolberg, R. Soni, S. Dirkmann, T. Mussenbrock, and H. Kohlstedt, "A double barrier memristive device," *Scientific Reports*, vol. 5, no. 1, p. 13753, 2015.

[3] N. Alimardani, J. M. McGlone, J. F. Wager, and J. F. Conley, "Conduction processes in metal–insulator–metal diodes with Ta $_2$ O $_5$ and Nb $_2$ O $_5$ insulators deposited by atomic layer deposition," *J. of Vac. Sci. & Tech. A: Vacuum, Surfaces, and Films*, vol. 32, no. 1, p. 01A122, 2014.

[4] S. Slesazeck, H. Mähne, H. Wylezich, A. Wachowiak, J. Radhakrishnan, A. Ascoli, R. Tetzlaff, and T. Mikolajick, "Physical model of threshold switching in NbO 2 based memristors," *RSC Advances*, vol. 5, no. 124, pp. 102 318–102 322, 2015.

[5] A. Ascoli, A. S. Demirkol, R. Tetzlaff, S. Slesazeck, T. Mikolajick, and L. O. Chua, "On Local Activity and Edge of Chaos in a NaMLab Memristor," *Frontiers in Neuroscience*, vol. 15, 2021.

[6] S. Slesazeck, H. Wylezich, and T. Mikolajick, "Analog memristive and memcapacitive properties of Ti / Al2O3 / Nb2O5 / Ti resistive switches," in *IEEE Latin American Symposium on Circuits Systems*, 2017, pp. 1–4.

[7] H. Mähne, H. Wylezich, F. Hanzig, S. Slesazeck, D. Rafaja, and T. Mikolajick, "Analog resistive switching behavior of Al/Nb2O5/Al device," *Semicond. Sci. and Tech.*, vol. 29, no. 10, p. 104002, 2014.

[8] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 211–221, 2013.

[9] C. Lammie, W. Xiang, B. Linares-Barranco, and M. Rahimi Azghadi, "MemTorch: An Open-source Simulation Framework for Memristive Deep Learning Systems," *Neurocomputing*, vol. 485, pp. 124–133, 2022.

[10] J. Radhakrishnan, S. Slesazeck, H. Wylezich, T. Mikolajick, A. Ascoli, and R. Tetzlaff, "A physics-based Spice model for the Nb2O5 threshold switching memristor," in *CNNA 2016; 15th International Workshop on Cellular Nanoscale Networks and Their Applications*, 2016, pp. 1–2.

[11] R. Schroedter, E. Mgeladze, M. Herzig, A. Ascoli, S. Slesazeck, T. Mikolajick, and R. Tetzlaff, "Physics-based modeling of a bi-layer Al2O3/Nb2O5 analog memristive device," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Texas, 2022.

[12] Z. Wang, S. Kumar, Y. Nishi, and H.-S. P. Wong, "Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback mechanism," *Applied Physics Letters*, vol. 112, no. 19, p. 193503, 2018.

[13] L. Chua, "If it's pinched it's a memristor," *Semiconductor Science and Technology*, vol. 29, no. 10, p. 104001, 2014.

[14] C. Acha, "Graphical analysis of current-voltage characteristics in memristive interfaces," *Journal of Applied Physics*, vol. 121, no. 13, p. 134502, 2017.

[15] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching dynamics in titanium dioxide memristive devices," *Journal of Applied Physics*, vol. 106, no. 7, p. 074508, 2009.

[16] C. Yakopcic, T. M. Taha, G. Subramanyam, and R. E. Pino, "Memristor SPICE model and crossbar simulation based on devices with nanosecond switching time," in *International Joint Conference on Neural Networks (IJCNN)*, 2013, pp. 1–7.

Post-print version of the article: R. Schroedter, A. S. Demirkol, A. Ascoli, R. Tetzlaff, E. Mgeladze, M. Herzig, S. Slesazeck, T. Mikolajick, "SPICE Compact Model for an Analog Switching Niobium Oxide Memristor", *2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAST), Bremen, Germany*, pp. 1-4, 2022.
DOI: 10.1109/MOCAST54814.2022.9837726
© © 2022 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.
For further information contact: richard.schroedter[at]tu-dresden.de, ORCID: 0000-0003-3259-4571