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A pseudo-memcapacitive neurotransistor for spiking neural networks

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***Abstract*—In this paper, we present a pseudo-memcapacitive neurotransistor by embedding a nonvolatile, abrupt-switching memristor at the gate of an NMOS transistor to emulate neuronal integrate and fire behavior. Neural networks, implementing spike-based computing paradigms on hardware platforms, integrating memristor crossbar arrays on underlying CMOS circuitry, operate similarly as neuronal networks in the human brain, which can significantly improve the time and energy efficiency of standard data processors. We demonstrate that also nonvolatile memristors can be considered to realize neuronal leaky integration and firing functionality including the neuron reset being performed intrinsically by a sufficiently discharged 'membrane' potential at the gate of a transistor. A versatile, compact and abrupt-switching model of a nonvolatile memristor with built-in cycle-to-cycle variability is proposed, forming a pseudo-memcapacitance along with the gate capacitance and evoking conditional neuronal spike generation depending upon the properties of the input pulse train. The SPICE code of the pseudo-memcapacitive neurotransistor is applied to verify the design parameters that trigger firing. Finally, the envisaged circuit realization of the proposed design is discussed.**

***Index Terms*—Pseudo-memcapacitive neurotransistor, nonvolatile memristor, SPICE model, spiking neural networks**

I. Introduction

The tremendous energy consumption observed during training and inference of large neural networks demands for low-power hardware accelerators. In this regard, nanoscale memristive devices enable to improve the time and energy efficiency of these networks, endowing them with bio-mimetic functionalities [1]. Memristors are widely used as synaptic elements in neuromorphic circuits [2], while in different studies the neuronal integrate and firing dynamics are investigated as reviewed in [3]. Abrupt-switching nonvolatile memristive behavior is attractive for the analog implementation of conditional neuronal firings in spiking neural networks. A memristive integrate and fire neuron with minimal complexity was derived in [4], as inspired from the Hodgkin-Huxley neuron model [5]. Volatile memristors hosting the peculiar current-controlled negative differential resistance region [6], [7], have been utilized in the design of neuristor circuits [8]. A compact hardware solution, employing diffusive memristors for emulating the leaky integrate-and-fire neurons and realizing a pattern classification task, is proposed in [9]. Similarly, the diffusive volatile memristor has been embedded at the gate of a transistor enabling integration and firing behavior for neural spiking networks [10]. However, the neurotransistor concept has not been shown with nonvolatile memristors, which are in fact being studied extensively to improve the performance of memories and neuromorphic accelerators [1], [11].

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In this paper, we propose a pseudo-memcapacitive neurotransistor implementation, consisting of an NMOS transistor and a pseudo-memcapacitor, where the latter exploits the combined action of a nonvolatile memristor coupled to the gate of a transistor exploiting its inherent parasitic capacitances. The presented implementation does not necessarily require additional circuit elements, but takes advantage of the intrinsic memristor capacitance, which is present in many metal-oxide-metal stacks, and the gate capacitance of a MOSFET serving as neuronal 'membrane' capacitance. The integration and firing dynamic of the proposed memcapacitive neurotransistor is simulated using uniform spike inputs as in neural spiking networks. The abrupt-switching or runaway dynamics, which governs many valence change (VCM), electrochemical metallization (ECM) or thermochemical (TCM) memory devices, cf. [11], [12], is activated with spike-based stimuli, which further charges the memcapacitive 'membrane' to the voltage level that a MOSFET may switch on. This switching leads to a current flow through the drain terminal, finally emulating a neuronal action potential. The neurotransistor is suitable for operating in a cascaded structure realizing multiple layers of a spiking neural network with capacitively coupled weight synapses connected to the neurotransistor [10]. The paper is organized as follows: First, we explain the pseudo-memcapacitive neurotransistor concept in Sec. II and then demonstrate the integrate and fire functionality in Sec. III, followed by discussion Sec. IV and conclusion Sec. V.

II. Pseudo-memcapacitive neurotransistor

The pseudo-memcapacitive neurotransistor, as depicted in Fig. 1a, is a three-terminal device emulating the leaky integrate-and-fire dynamics of a biological neuron [10]. Here, a pseudo-memcapacitor is placed at the gate of an NMOS transistor which forms a charge reservoir through its considerably large gate-source capacitance. The equivalent circuit representation including the memristor-based pseudo-memcapacitor is shown in Fig. 1b, where the memristor R_{m} with intrinsic

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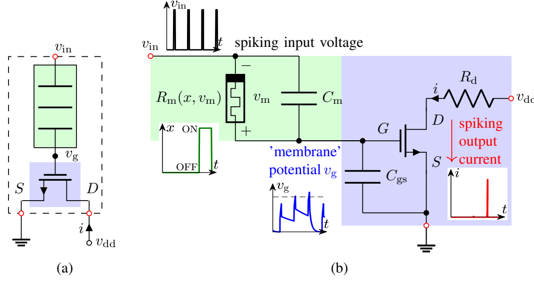

Fig. 1: Neurotransistor structure: (a) Pseudo-memcapacitor at the gate of an NMOS transistor (dashed box), and (b) proposed circuit with a memristor-based pseudo-memcapacitive device (green) and the NMOS with gate capacitance C_{gs} (blue). Insets show representative signals from Fig. 5.

(or external) capacitance C_{m} forms the neuronal 'membrane' capacitance, together with the intrinsic (or external) gate-source capacitance C_{gs} of the NMOS transistor. Regarding the realization of such a device, the memristive stack might be deposited on the gate of a transistor, while the off-to-on memristance and capacitance ratios, i.e. $R_{\mathrm{off}}/R_{\mathrm{on}}$ and $C_{\mathrm{gs}}/C_{\mathrm{m}}$, critical design parameters in this study, can be tuned, if necessary, through a careful selection of the memristor and transistor devices.

The neurotransistor operates as follows (cf. insets in Fig. 1b or Fig. 5): In a spiking neural network a spike train reaches the memcapacitance input node v_{in} and leads to an incremental charging of the 'membrane' potential v_{g} at the gate. When the voltage level at the gate node reaches the transistor threshold voltage V_{to} (dashed line in the inset depicting v_{g} over time), the transistor emulates neuron firing by passing a spike current i through the drain. In parallel, the raised 'membrane' potential, in conjunction with the input spike train, switches the memristor ON in low resistance state (LRS), which causes first a faster charging of the 'membrane' potential and then a discharging of the same node through the memristor after the firing pulse. In parallel to the firing event, as the input signal v_{in} returns to zero, the voltage $v_{\mathrm{m}} = v_{\mathrm{g}} - v_{\mathrm{in}}$, falling across R_{m}, exceeds the SET threshold, and the memristor switches on. Its low resistance state (LRS) offers a discharging path for the membrane capacitance. With the gate potential sufficiently low, as soon as a new spike arrives at the input, the memristor undergoes a RESET transition, attaining once again the HRS, and the neuristor returns back to its initial condition.

The memristor-based *pseudo-memcapacitor* [10] consists of a memristor connected in parallel and in series with two capacitors, which can be programmed to low and high capacitance values by switching the memristor to HRS and LRS, respectively, cf. Fig. 2. The time constant $\tau = R_{\mathrm{m}}(C_{\mathrm{m}} + C_{\mathrm{gs}})$ of the pseudo-memcapacitor changes according to the memristance $R_{\mathrm{m}} = [R_{\mathrm{on}}, R_{\mathrm{off}}]$ establishing a slow or fast charging of the 'membrane' voltage v_{g}, cf. Fig. 2. Taking into account a sufficiently large off-to-on memristance ratio $R_{\mathrm{off}}/R_{\mathrm{on}} > 10$ and a considerable high capacitance ratio $C_{\mathrm{gs}}/C_{\mathrm{m}} > 5$, the low capacitance state (LCS) becomes approximately C_{m}, while the high capacitance state (HCS) is C_{gs}. This pseudo-memcapacitive switching between LCS and HCS is visualized by the I-V sine wave response in Figs. 2d and 2e.

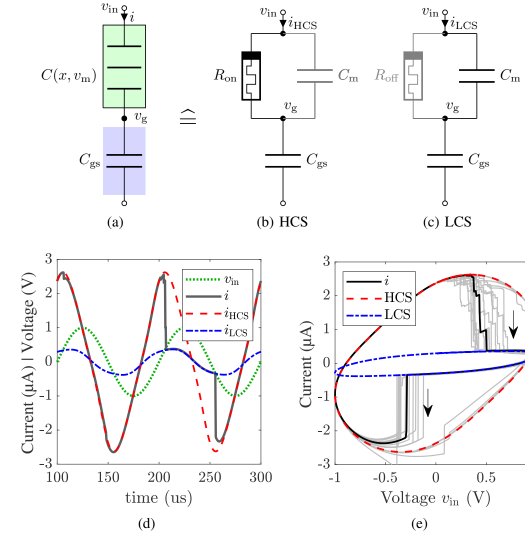

Fig. 2: Memristor-based pseudo-memcapacitor: (a) schematic with state dependent memcapacitance $C(x, v_{\mathrm{m}})$, (b) schematic for HCS with $\tau_{\mathrm{on}} = R_{\mathrm{on}}(C_{\mathrm{m}} + C_{\mathrm{gs}})$, (c) schematic for LCS with $\tau_{\mathrm{off}} = R_{\mathrm{off}}(C_{\mathrm{m}} + C_{\mathrm{gs}})$, (d) and (e) time and I-V response for a 10 kHz ± 1 V sine wave input (green) for memristor-based pseudo-memcapacitor (gray; median in black) with values $C_{\mathrm{m}} = 5$ pF and $C_{\mathrm{gs}} = 45$ pF, as well as for the ideal cases HCS (red) and LCS (blue).

III. Verification of Integrate and Fire Behavior

For the verification of the proposed neurotransistor we analyze the equivalent circuit of Fig. 1 based on a SPICE simulation. The diode-like memristor description [13] provides a versatile model for abrupt switching memristive devices in agreement with the experimental data for many memristive devices and is suitable for the proposed neurotransistor concept. The voltage-controlled memristor current is:

$$i_{\mathrm{m}} = K(x, i_{\mathrm{on}}, i_{\mathrm{off}}) \cdot \sinh\left(K(x, a_{\mathrm{on}}, a_{\mathrm{off}}) \cdot v_{\mathrm{m}}\right), \quad (1)$$

where the state variable x reads values in the interval $[0, 1]$, and the function $K(x, \lambda_{\mathrm{on}}, \lambda_{\mathrm{off}}) = \lambda_{\mathrm{off}} + x \cdot (\lambda_{\mathrm{on}} - \lambda_{\mathrm{off}})$ is a linear function of x bounded in the interval $[\lambda_{\mathrm{on}}, \lambda_{\mathrm{off}}]$. The memristor state dynamics are defined individually for set and reset according to the memristor voltage polarity with

$$\dot{x} = \begin{cases} (x_{\max} - x)\exp\left[\eta_{\mathrm{s}}(v_{\mathrm{m}} - V_{\mathrm{s}}^{*})\right] & \text{for } v_{\mathrm{m}} \geq 0 \\ (x_{\min} - x)\exp\left[-\eta_{\mathrm{r}}(v_{\mathrm{m}} - V_{\mathrm{r}}^{*})\right] & \text{for } v_{\mathrm{m}} < 0 \end{cases}. \quad (2)$$

The switching speed is determined by the factors η_{s} and η_{r}. A built-in intrinsic white noise source $n(t)$, with variance of $0.05\,\mathrm{V}^2$ for 10 ns sample time, is embedded into the memristor SET and RESET voltage thresholds, according to

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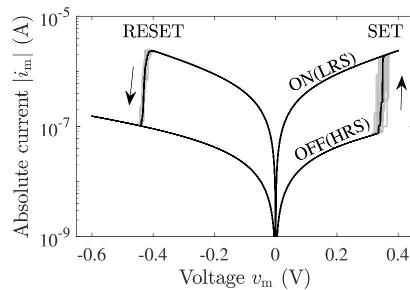

Fig. 3: I-V curves of 20 periods (gray) and its median (black) of the memristor for 1 Hz sine wave input demonstrating abrupt-switching with variability for set around 0.35 V and for reset around −0.42 V

$V_\mathrm{s}^* = V_\mathrm{s}(1 + n(t))$ and $V_\mathrm{r}^* = V_\mathrm{r}(1 + n(t))$, respectively, to account for the effects of cycle-to-cycle variability in the abrupt switching dynamics. The cycle-to-cycle variability of the switching is visualized for 20 cycles together with its median in Figs. 2e and 3. The variability also lowers the nominal switching thresholds $V_{\mathrm{s,r}}$. These 'snapback' and 'snapforward' effects, i.e. known for filamentary VCM devices, lead to abrupt-switching at certain thresholds that vary in time [14]. The implemented memristor model is designed within parameter space reported in [13] and fits to this class of abrupt-switching memristors. The SPICE implementation of the pseudo-memcapacitive neurotransistor is given by Fig. 4. To obtain results without numerical defects, we use the function $\mathtt{limit}(x, x_{\min}, x_{\max})$, which bounds the state within $[0, 1]$, as well as the memristor current I_{cc} in a physically reasonable range.

The neurotransistor functionality is visualized in Fig. 5 for uniform spike inputs of 1.8 V amplitude, 10 µs width and variation of the spike intervals $\Delta t = \{200, 100, 40, 15\}$µs. The output spike events are marked by arrows above each plot. For the initially arriving spikes with an interval of 200 µs, the gate node can neither exceed markedly the transistor threshold nor it switches the memristor ON. As a result, no firing event may be reached in the first phase, cf. Fig. 5g. Hereafter, the 'membrane' potential leaks through the memristor, cf. Fig. 5f from 1 ms to 1.5 ms. Following a decreased spike interval of 100 µs starting at 1.5 ms, three successive pulses are sufficient for v_g to exceed noticeably the transistor threshold V_{to} (see Fig. 5f) and thus resulting in a firing event of the transistor current (cf. Fig. 5g). Meanwhile, the memristor switches ON, i.e. its resistance undergoes an abrupt transition from HRS to LRS (cf. Figs. 5d, 5e), and leads to a fast discharge of the 'membrane' gate voltage as a negative current flows through the memristor (cf. Fig. 5c). The subsequent incoming pulse switches the memristor back to the OFF state (i.e. HRS) and thus resets the neurotransistor, since the voltage drop across the memristor is below V_r. In addition, one can observe the influence of switching variability at 2.6 ms, where the memristor is not fully switched ON, but the fire event can still happen. As expected, shorter spike intervals of 40 µs and

```
** Memristor-based memcapacitive neurotransistor
.SUBCKT MemNeuroTransistor IN D G S SV
** Parameter
.params Icc=1m xmax=1 xmin=0 x0=0
+ion=1u ioff=100n aon=4 aoff=2
+etas=250 etar=100 Vs=0.5 Vr=-0.5
+Cp=5p Cgs=45p Rp=200Meg Rs=10
** Circuit
* Noise source for snap forward/snap back current
Gn 0 N value={white(1e8*time)}
Rn N 0 {1}
* Series resistance
Ri G M {Rs}
* Current source for memristance IV response
Gm M IN value={limit(Im(V(SV,0),V(M,IN)),-Icc,Icc)}
* Parallel capacitance and resistance
Cm G IN {Cp}
Rm G IN {Rp}
* State dynamics dx/dt = F(V,x)
Cx SV 0 {1} ic={x0}
Gx 0 SV value={F(V(SV,0),V(G,IN),I(Gn))}
* NMOS and gate-source capacitance
Mn D G S NT
Cg G S {Cgs}
** Functions
*linear state dependency
.func K(x,on,off)=off+(on-off)*limit(x,xmin,xmax)
*diode-like current function
.func Im(x,vm)= K(x,ion,ioff)*sinh(K(x,aon,aoff)*vm)
*set and reset time constants with noise n
.func TS(v,n)=exp(-etas*(v-Vs*(1+n)))
.func TR(v,n)=exp( etar*(v-Vr*(1+n)))
*State equation for state in range of [0,1]
.func F(x,v,n)= if(v>=0,(xmax-x)/TS(v,n),(xmin-x)/TR(v,n))
** NMOS transistor
.model NT NMOS(LEVEL=3 L=1u W=4u Vto=0.45 Tox=12n
+Uo=798 PHI=66)
.ENDS MemNeuroTransistor
```

Fig. 4: SPICE code of three-terminal neurotransistor with input (IN), drain (D) and source (S) and additionally the internal 'membrane' gate voltage v_g (G) and state variable x (SV) for verification purposes.

15 µs result in more frequent neuron firing at each two and single successive pulses, respectively. After the last incoming pulse burst, it is visible that the previously switched ON memristor maintains its resistance state until a subsequent incoming spike, i.e. at 4 ms, resets the neuron.

In order to achieve the described neurotransistor functionality the parameter are designed as follows:

- The gate-source capacitance C_{gs} must be much larger, e.g. by a factor of 5, than the parallel capacitor C_m, i.e. $C_{\mathrm{gs}} = 45$ pF and $C_\mathrm{m} = 5$ pF, to allow integration of multiple incoming voltage spikes and charge the gate 'membrane' successively.
- The current ratio $i_{\mathrm{on}}/i_{\mathrm{off}}$, determined by the memristance ratio $R_{\mathrm{off}}/R_{\mathrm{on}} > 10$ (cf. [11]), enables the implementation of different charging times with τ_{off} and τ_{on}.
- Considerable high memristor switching speeds, i.e. $\eta_\mathrm{s} = 250$ and $\eta_\mathrm{r} = 100$, with respect to the 'membrane' integration time allow an abrupt-switching behavior before the 'membrane' gate potential is charged or discharged, respectively. The internal white noise source features the typical randomness in the abrupt switching behavior and increases switching probability before the nominal thresholds at ±0.5 V such that it switches for set around 0.35 V and for reset around −0.42 V as shown in Fig. 3.
- The transistor threshold, i.e. $V_{\mathrm{to}} = 0.45$ V, is above

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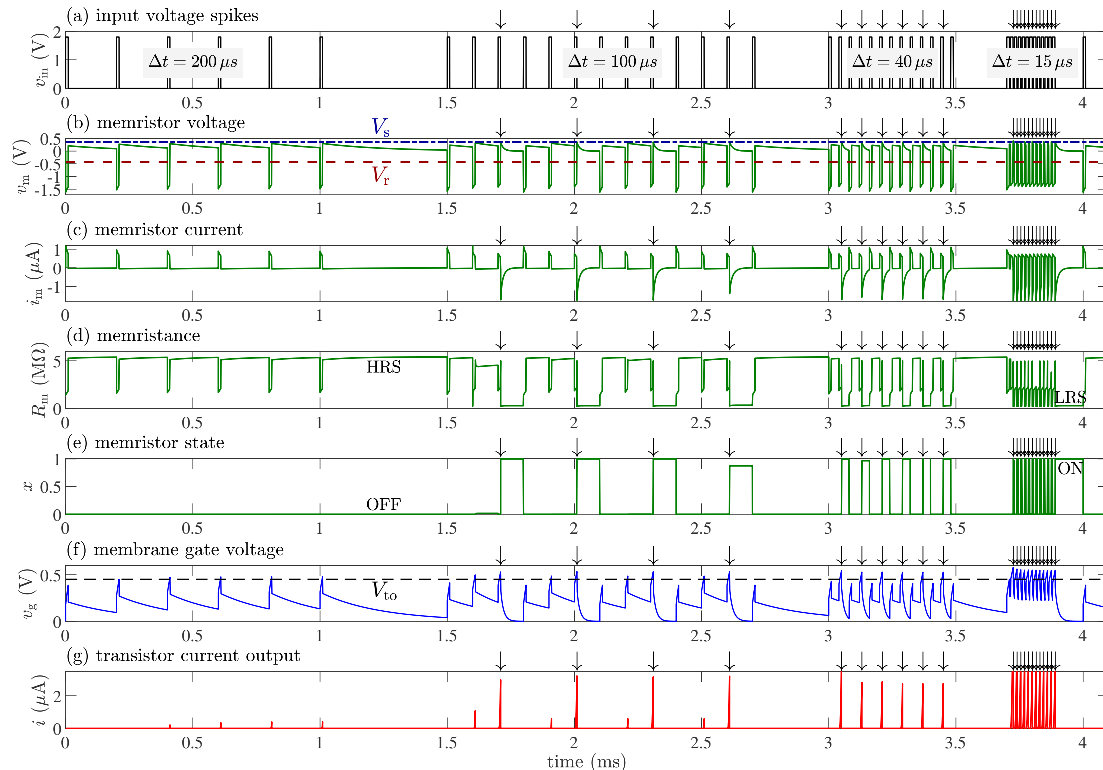

Fig. 5: Simulation result of the proposed neurotransistor for uniform input spikes (10 µs-long pulses with 1.8 V amplitude) while varying their intervals $\Delta t = \{200, 100, 40, 15\}$µs at $\{0, 1.7, 3.0, 3.7\}$ms of the time: (a) input voltage v_{in}, (b) memristor voltage $v_{\mathrm{m}} = v_{\mathrm{g}} - v_{\mathrm{in}}$, (c) current i_{m} through memristor, (d) memristance $R_{\mathrm{m}} = v_{\mathrm{m}}/i_{\mathrm{m}}$, (d) memristor state variable x, (e) gate 'membrane' voltage v_{g}, (f) NMOS transistor current through R_{d} for $v_{\mathrm{dd}} = 3\,\mathrm{V}$. The output spike events are marked with arrows above each plot.

enough the effective set voltage, which is around 0.35 V, such that the variations in the 'membrane' potential occurring during the integration phase can be filtered out.

- The neuron can be reset if only the memristor is previously switched ON, and therefore, discharging the gate node to a low enough level resulting in a negative voltage drop with the arrival of the subsequent spike input, see Fig. 5b.

IV. Discussion

The neurotransistor results in Fig. 5 verify a functional neuronal behavior of the proposed pseudo-memcapacitive neurotransistor. The input spike times depend on the dynamics of the memcapacitor, which determines the scales of the spike network time of the neurons. In the demonstrated case, if the ratio between the input spike interval and spike duration falls below 10, the neuron leakage represented by the memristance causes the neuron not to fire anymore. The memristor abrupt-switching behavior defined by η_{r} and η_{s} and the noise $n(t)$ are essential to enable fast discharging of the 'membrane' capacitance and thereby resetting the nonvolatile memristor to the HRS. Fortunately, many filamentary switching devices exhibit such an abrupt-switching dynamic. Finally, the presented neurotransistor shows leaky-integrate-and-fire dynamics and could be fabricated in a compact design while making use of intrinsic capacitance of memristive stacks and parasitic gate-source capacitances of the transistor.

V. Conclusion

In conclusion, this paper proposes a pseudo-memcapacitive neurotransistor setup constructed by considering a nonvolatile memristor embedded at the gate of a NMOS transistor and employing its gate-source capacitance. A SPICE circuit simulation of a leaky integrate-and-fire neuron is provided receiving uniform spike inputs with various intervals. In contrast to previously used volatile memristors, our approach expands the neurotransistor concept to the applicability of nonvolatile memristors to operate as neurons. A hardware implementation with real components is underway to experimentally prove the predicted functionality, taking into account the parasitic properties of the real circuit elements and enabling a fully analog implementation of energy-efficient spiking neural networks.

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