Poster link

An $ErMnO_3$ memristive spiking neuristor

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$ErMnO_3$ memristive device and neuristor model

- Pt/$ErMnO_3$/Pt current-controlled memristive device exhibiting volatile threshold switching:
  - positive differential resistance (PDR) $i_m < 10$ mA
  - negative differential resistance (NDR) $i_m > 10$ mA
  - → Device is „locally active“ in NDR region, i.e. negative equivalent resistance R_1
- Neuristor circuit emulates leaky-integrate-and-fire neuron with biasing in NDR and external capacitor C
  - → Dynamic model as coupled ODE of internal temperature T and memristor voltage v_m:

$$C_{\mathrm{th}}\,\dot{T} = v_{\mathrm{m}} \cdot i_{\mathrm{m}}(T, v_{\mathrm{m}}) - \Gamma_{\mathrm{th}}(T - T_{\mathrm{amb}})$$

$$C\,\dot{v}_{\mathrm{m}} = \frac{v_{\mathrm{b}} - v_{\mathrm{m}}}{R_{\mathrm{b}}} - i_{\mathrm{m}}(T, v_{\mathrm{m}})$$

  - → Memristor current modeled combining Poole-Frenkel emission for G_{PF} with T − independent bipolar diode i_d:

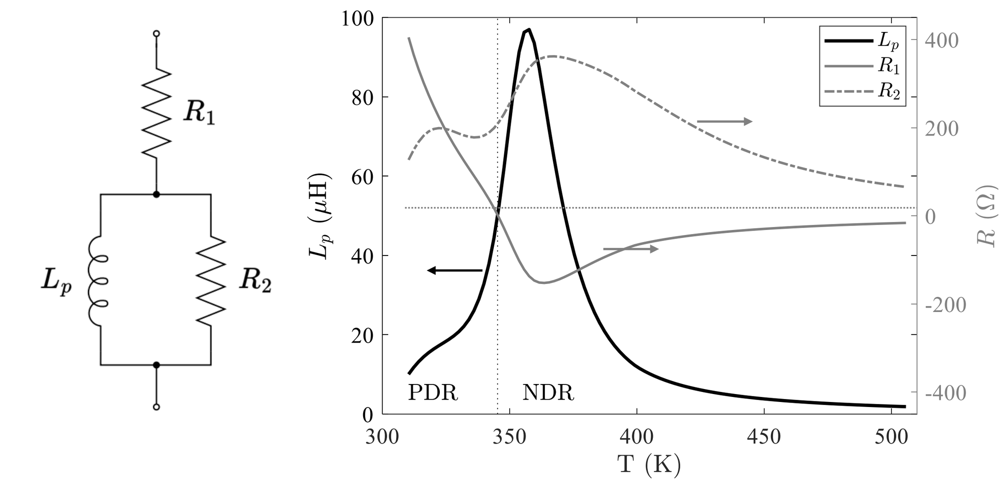
$$i_{\mathrm{m}}(T, v_{\mathrm{m}}) = G_{\mathrm{PF}}(T, v_{\mathrm{m}}) \cdot v_{\mathrm{m}} + i_{\mathrm{d}}(v_{\mathrm{m}})$$

$$G_{\mathrm{PF}}(T, v_{\mathrm{m}}) = g_0 \exp\left(\frac{-g_1 + g_2\sqrt{|v_{\mathrm{m}}|} - g_3|v_{\mathrm{m}}|}{T}\right)$$

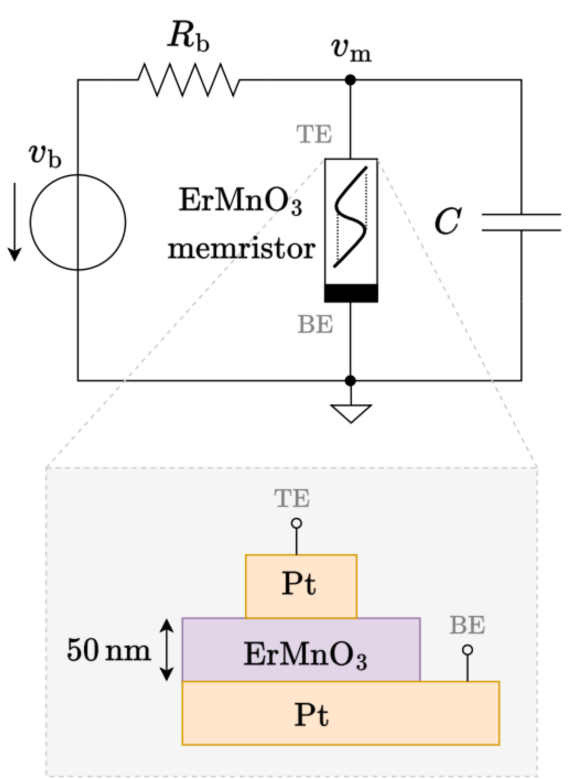
$$i_{\mathrm{d}}(v_{\mathrm{m}}) = I_{\mathrm{d}} \exp(k_{\mathrm{d}}|v_{\mathrm{m}}|)$$

Model constants: g_0, g_1, g_2, g_3, I_{d}, k_{d}, Γ_{th}, C_{th}

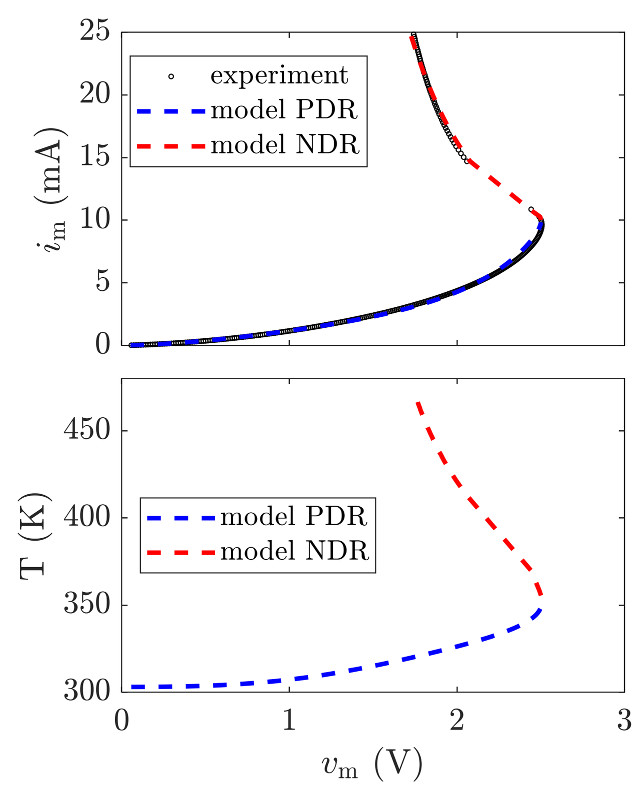
AC equivalent circuit parameter of $ErMnO_3$ memristor



Neuristor circuit



DC exp. and model

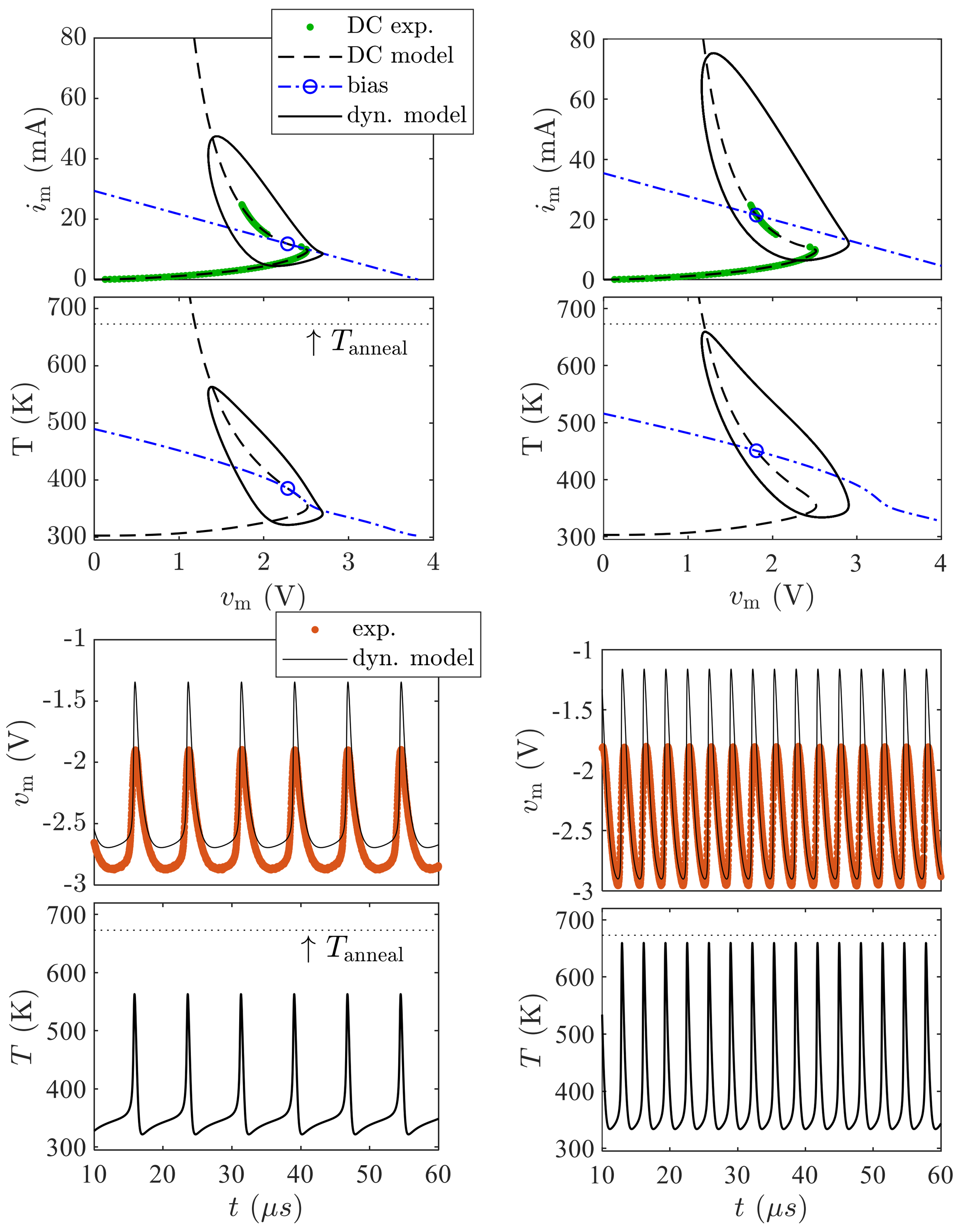


Neuristor results

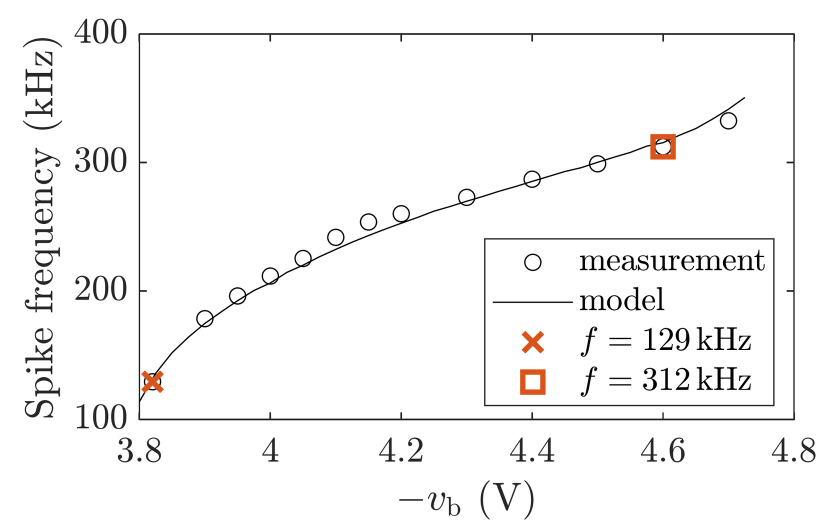
Stable neuristor oscillations

Low frequency response (×) $f = 129$ kHz at $v_b = -3.82\,V$

High frequency response (□) $f = 312$ kHz at $v_b = -4.6\,V$

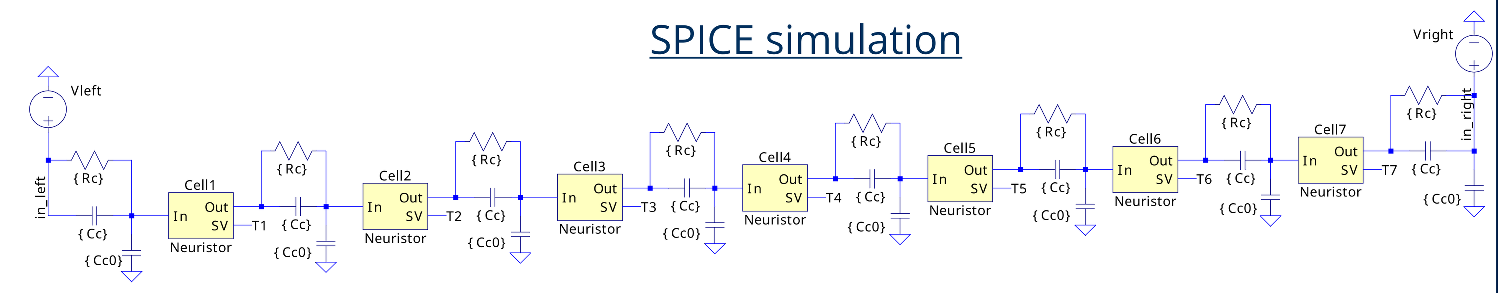


- Neuristor circuit with $C = 10.7$ nF, $R_b = 100\,\Omega$ demonstrates stable oscillations with high agreement between experimental and dynamic model.
- More than 2×10^9 cycles of stable oscillations have been measured over 8 hours.
- During the experiments, it was observed that non-volatile shifts start to occur in the DC I-V characteristic when the internal temperature reaches larger values than the annealing temperature of $T_{\mathrm{anneal}} = 400°C$.
  This phenomenon can be investigated through simulations of the dynamical model.
- Tuning of biasing voltage allows spike interval frequencies from 100 kHz to 300 kHz.
- The device thermal capacitance $C_{\mathrm{th}} = 20\,\frac{\mathrm{nWs}}{\mathrm{K}}$ is determined by matching dynamic model with measurements resulting in high agreement of spike interval frequency.

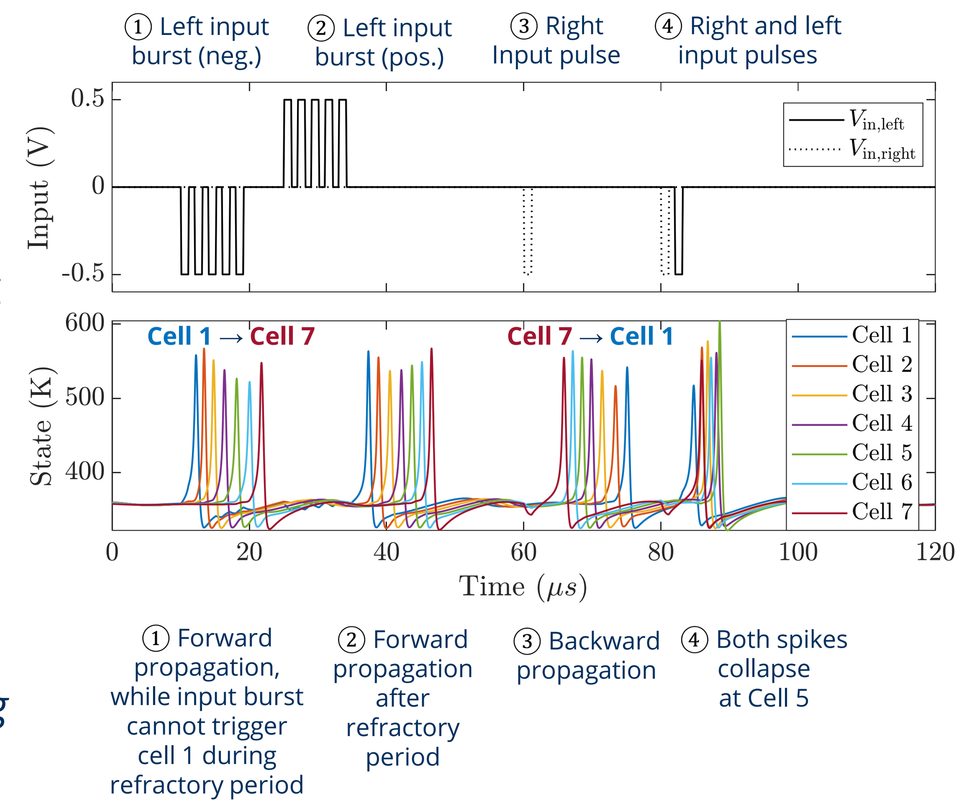


RC coupled neuristor chain

SPICE simulation

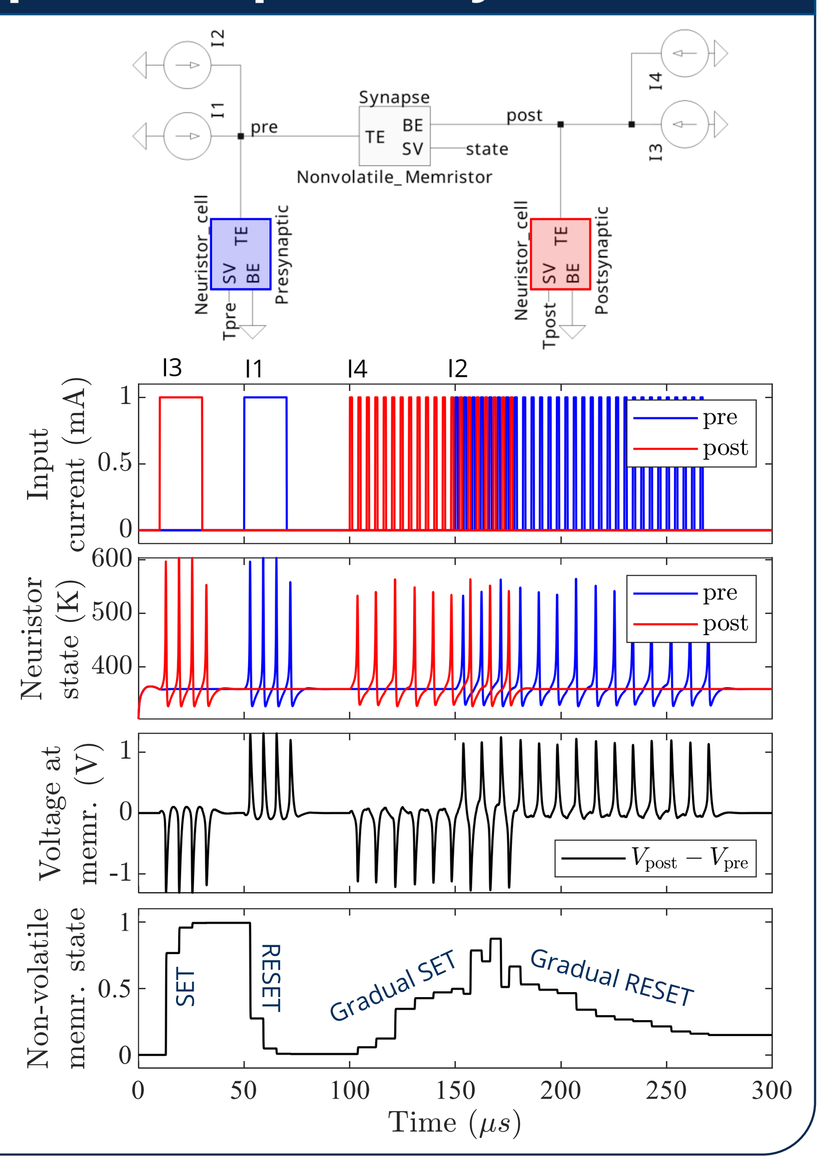


- RC-coupled neuristor chain of 7 cells:
  - → Refractory period of ~10 µs
  - → ①, ② forward and ③ backward travelling
  - → ④ destructive interference for spikes travelling in opposite direction
- RC element values define the coupling strength
- *Converging* and *diverging* branches of neuristor chains can be designed



Spike-time-dependent-plasticity

- Spike-time-dependent-plasticity (STDP) rule is implemented by coupling two neuristor cells via a non-volatile *synaptic* memristor in a SPICE simulation
- Model of non-volatile *synaptic* memristor from Aguirre et al., Micromachines, 13, 330, 2022
- Post- and pre-synaptic neuristors are stimulated with current pulses I1-I4
- Long current pulses (I3, I1) result in full SET/RESET of *synaptic* memristor within 3 spikes :
  SET for $V_{\mathrm{post}} - V_{\mathrm{pre}} < 0$ (I3)
  RESET for $V_{\mathrm{post}} - V_{\mathrm{pre}} > 0$ (I1)
- Short current pulses (I4, I2) result in gradual update of *synaptic* memristor depending on the neuristor's pulse timing



Summary

- Emerging memristive devices hosting an NDR region, such as the presented $ErMnO_3$ device, can be employed in neuristor circuits to emulate spiking neural networks and pave the way towards energy-efficient in-memory computing systems.
- We present a static and dynamic model for the $ErMnO_3$ device and derive the equivalent circuit parameters, e.g. a negative resistance R_1 in the NDR.
- The neuristor model employs the internal temperature as state variable which is a critical parameter for long term operations.
- We show the application of the neuristor model employed in a chain structure as well as for STDP learning through a non-volatile memristor.
- By emulating leaky-integrate-and-fire neurons, the presented neuristor is a promising device realizing spiking neural networks in in-memory hardware.

Literature:
[1] Demirkol, A.S., Ascoli, A., Messaris, I., Tetzlaff, R., 2021. Analytical Investigation of Pattern Formation in an M-CNN with Locally Active NbOx Memristors, in: 2021 IEEE International Symposium on Circuits and Systems (ISCAS). pp. 1–5. https://doi.org/10.1109/ISCAS51556.2021.9401280
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[3] Wu, R., "Resistive switching in mixed orthorhombic/hexagonal RMnO3 (R = Y, Er) polycrystalline thin films", Disseration, FU Berlin, 2024. http://dx.doi.org/10.17169/refubium-44694

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