Modul Number	Modul Name	Lecturer in Charge
NES-12 08 07	VLSI Processor Design	Prof. Mayr
Contents and Objectives	Content of the module: • Basics, concepts and methods for designing complex digital VLSI-systems • Architectures for highly integrated digital processing systems, with emphasis on user-specific signal processing systems • Methods for the efficient transfer of architectural concepts in the highly integrated implementation of a digital system. • Specification and abstract modelling of the system, conversion into a Register-Transfer-Level (RTL) description, automated circuit synthesis and physical implementation (place & route, layout synthesis), which results in the data needed for manufacture of the chip. • Verification of the design on all levels of abstraction (behaviour, implementation) via simulation (functional verification) • Proof of the equivalence of transformation steps via formal verification, i.e. by checking compliance with design rules (signoff-verification) • Training in working together as a design team (division of tasks, definition of interfaces, schedule planning and time management) Objectives: After completion of this module, the students will be able to carry out a complete implementation and verification of a VLSI-System (e. g. a processor with a complexity comparable to an 8051) using industrial design software (Synopsys, Cadence).	
Modes of Teaching and Learning	The module consists of 2 hours per week lectures, 2 hours tutorial, 2 hours lab work and self study.	
Prerequisites		
Usability	The module is an elective module in the master's program ‚Nanoelectronic Systems'.	
Requirements for Acquiring Credit Points	The credit points are awarded when the module assessment is passed. The module assessment consists of a project report with a scope of 30 hours.	
Credit Points and Grades	7 credit points can be obtained by the module. The module grade is the grade of the project.	
Frequency	The module is offered every summer semester.	
Work Load	The total effort is 210 hours.	

Duration	1 Semester