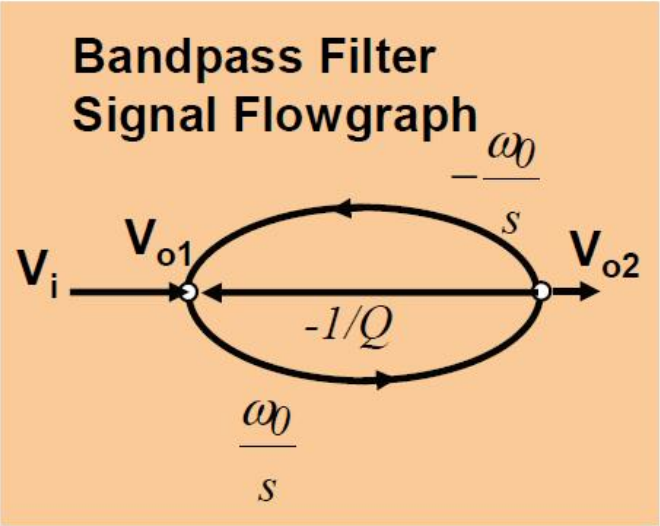
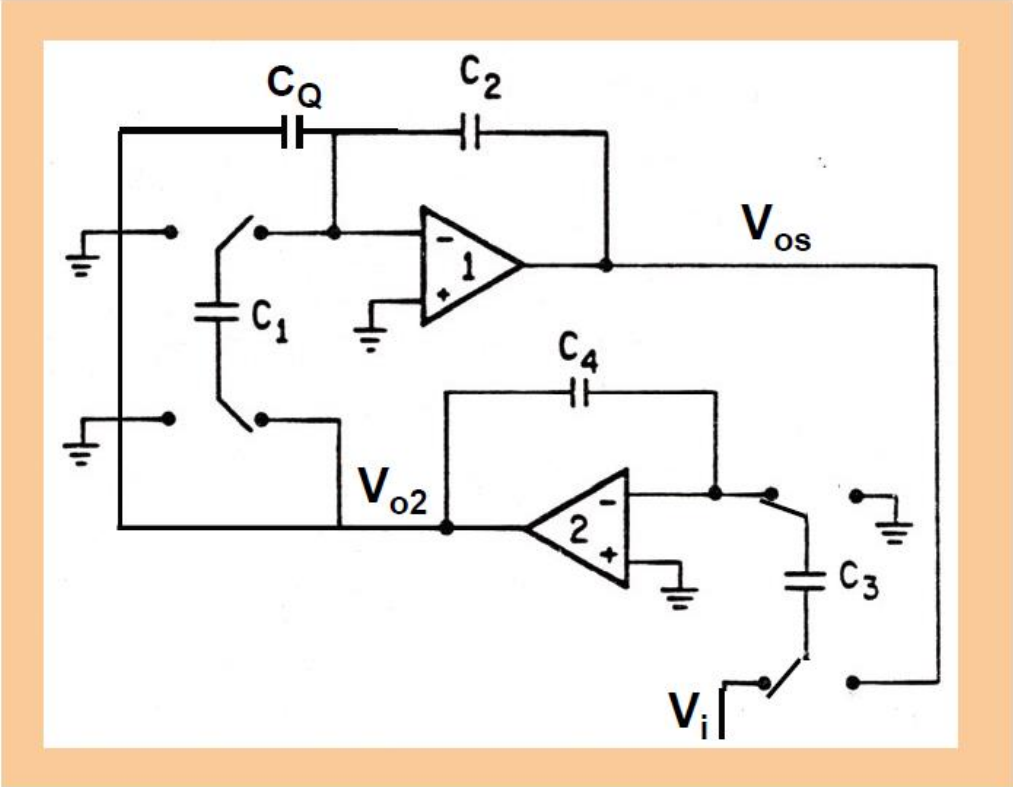
Discrete Time Example

- **Switched Capacitor (SC) resonator used as band-pass**



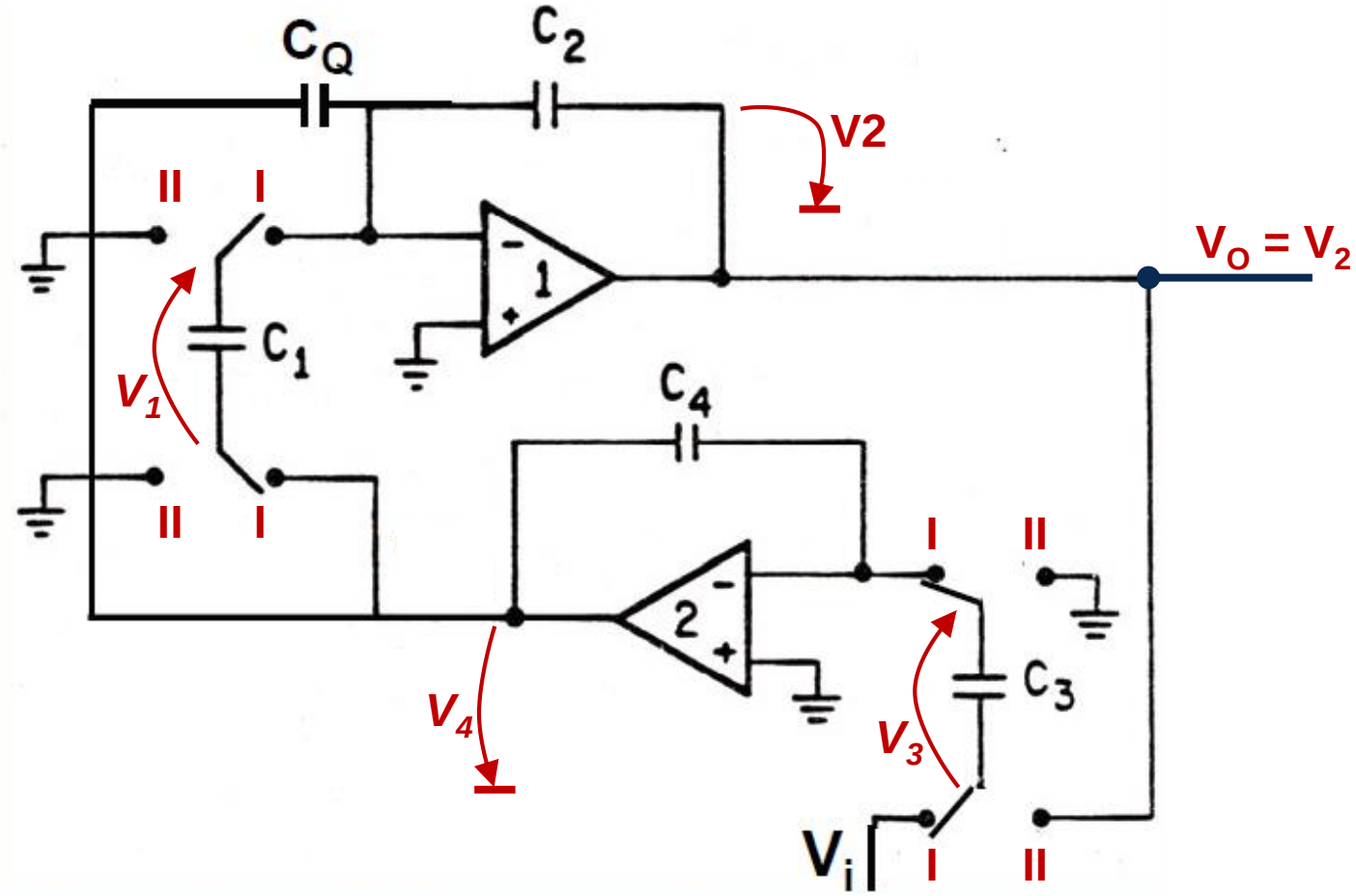
$$\omega_0 = f_s \times \frac{C_3}{C_4} = f_s \times \frac{C_1}{C_2}$$

$$Q = \frac{C_2}{C_Q}$$



http://www-inst.eecs.berkeley.edu/~ee247/fa08/files07/lectures/L10s_f08.pdf

Switches are operated synchronously in two phases I and II.
Define voltages for the following calculations.



Assume ideal operational amplifiers.
Calculate charge balances, when all switches change from position II to I:

C3 gets connected to V_i and to virtual ground:

$$V_{3,I} = V_i$$
$$\Delta V_3 = V_{3,I} - V_{3.II} = V_i - V_{3,II}$$

Through the virtual ground, charge is transferred from C3 to C4:

$$\Delta V_4 = -\frac{C3}{C4} \cdot \Delta V_3$$
$$V_{4,I} = V_{4,II} + \Delta V_4$$

C1 gets connected to V_4 and to virtual ground:

$$V_{1,I} = V_{4,I}$$
$$\Delta V_1 = V_{1,I} - V_{1.II} = V_{4,I} - V_{1,II}$$

Charge from C1 and from CQ is transferred to C2:

$$\Delta V_2 = -\frac{C1}{C2} \cdot \Delta V_1 - \frac{CQ}{C2} \cdot \Delta V_4$$
$$V_{2,I} = V_{2,II} + \Delta V_2$$

SC works in two phases:
Calculate charge balances, when all switches change to position II:

The input at C4 is left open, no change at V_4:
$V_{4,II} = V_{4,I}$

C1 is discharged, and all charge on C1 dissipates:
$V_{1,II} = 0$

C1 is disconnected from C2. No charge transfer through CQ because V_4 does not change: Also V_2 does not change.
$V_{2,II} = V_{2,I}$

C3 gets connected to V_2 and to ground, changes in charge dissipate:
$V_{3,II} = V_{2,II}$

Source code: **sc_bandpass/source/behavioral/sc_bandpass.vhd**

In the model, associate **clk='1'** with phase I and **clk='0'** with phase II

In a real implementation, switches are operated in a non-overlapping scheme. Usually, the non-overlapping clock phases are derived from a single clock as above, so the simplifying assumption is reasonable.

Nyquist requires sampling frequency $f_s > 2 \cdot f_{max}$.
For practical applications $f_s > 10 \cdot f_{signal}$ is very reasonable.

Test bench: **sc_bandpass/source/tb/sc_bandpass_tb.vhd**

Generate the clock and a sinus input signal with a frequency sweep. Run for 1ms to see the full sweep.