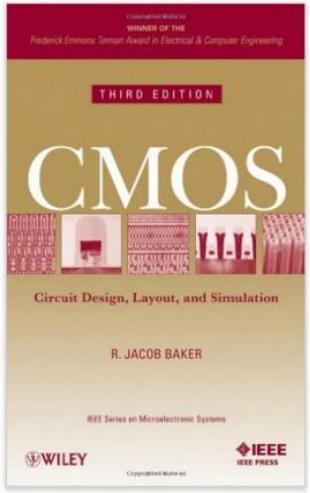
Schaltkreis- und Systementwurf

Teil 4: Digitale CMOS Schaltungen

Inhalt

- CMOS Technologie
- CMOS Logik
- Timing von CMOS Schaltungen
- Verlustleistung von CMOS Schaltungen
- Standardzellenbibliotheken
- SRAM
- I/O Zellen

- Ergänzende Vorlesungen:
  - Elektronische Bauelemente
  - Halbleitertechnologie
  - Schaltungstechnik
- Weiterführende Vorlesungen:
  - VLSI Prozessorentwurf
  - Neuromorphe VLSI-Systeme

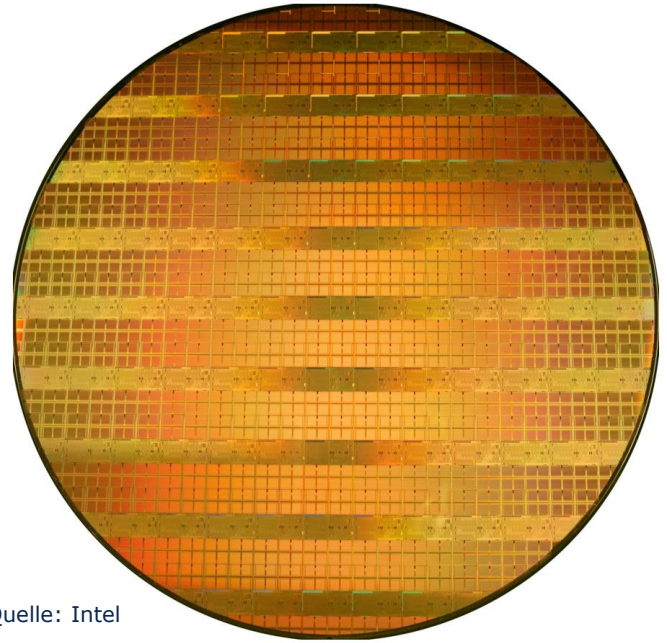


- Literaturempfehlungen:
  - CMOS, Circuit Design, Layout and Simulation; R. Jacob Baker; IEEE Press Series on Microelectronic Systems, 3rd Edition, 2011
  - Halbleiter-Schaltungstechnik; Ulrich Tietze, Christoph Schenk; Springer; 2002

CMOS Technologie

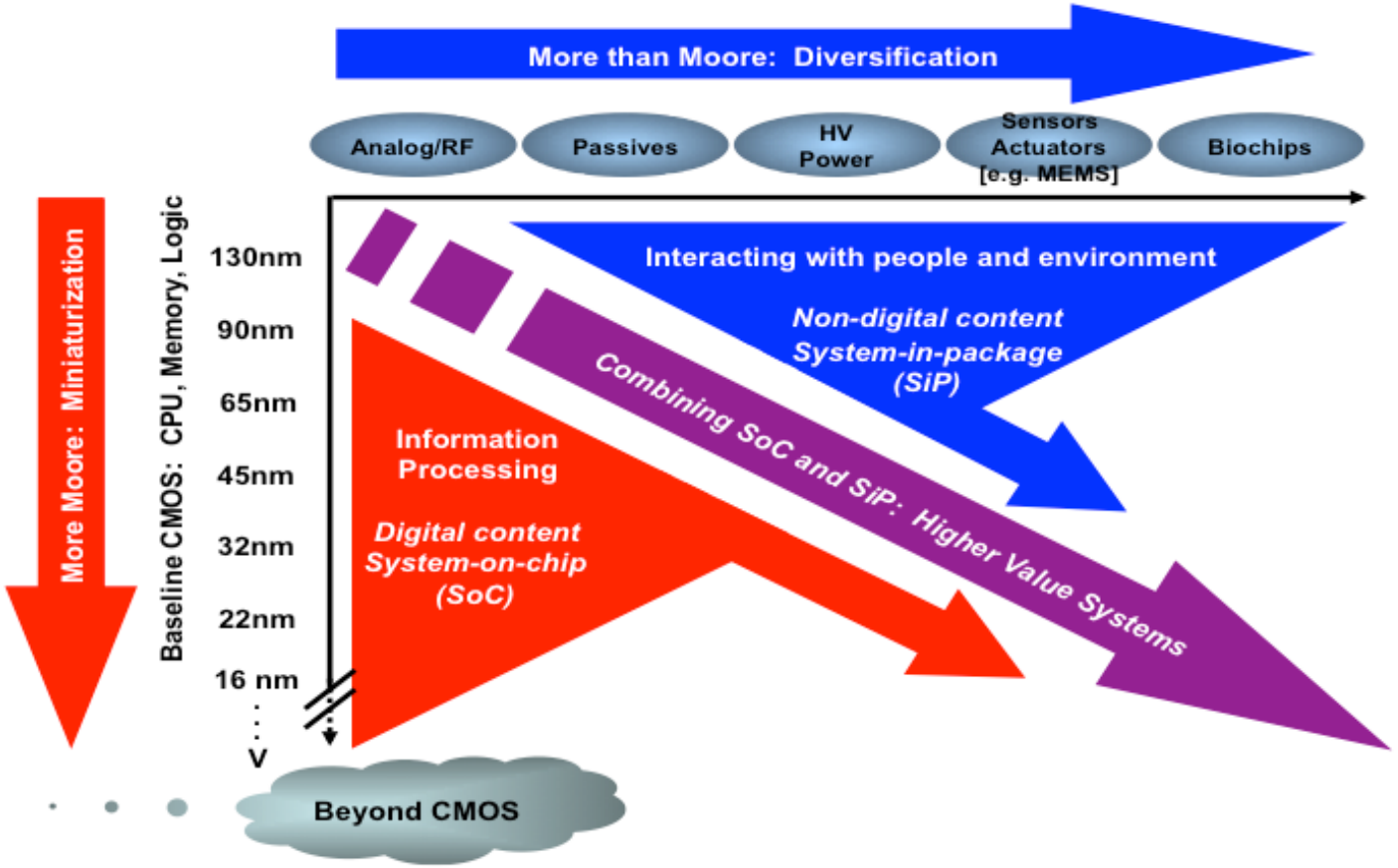
CMOS Technologie

- Complementary Metal Oxide Semiconductor (CMOS) Technologie
- Integration von n-Kanal (NMOS) und p-Kanal (PMOS) Feldeffekttransistoren auf einem Siliziumchip
- Halbleiterprozess zur kostengünstigen Herstellung von integrierten digitalen, analogen und Mixed-Signal Schaltungen
- Herstellung im Waferprozess



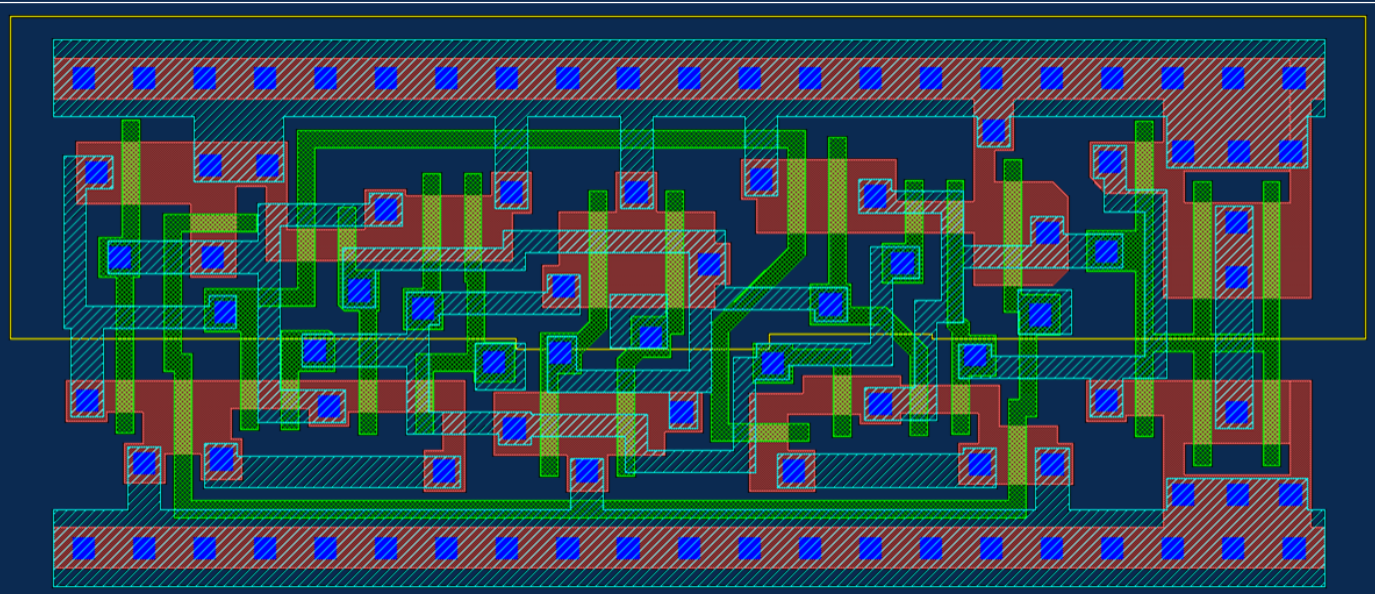
Quelle: Intel

CMOS Technologieskalierung

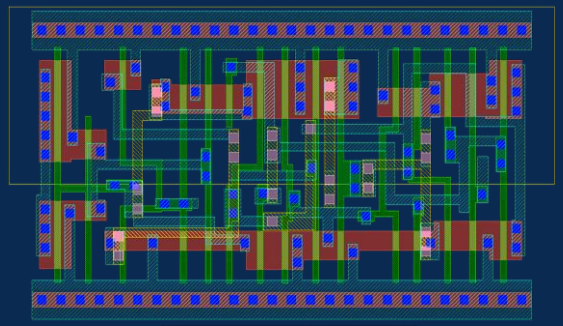


Quelle: International Technology Roadmap for Semiconductors

Standard Cell Scaling



180nm

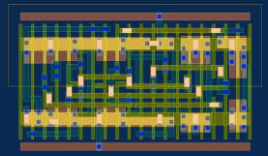


65nm

D-Flip-Flop

Drawn to Scale

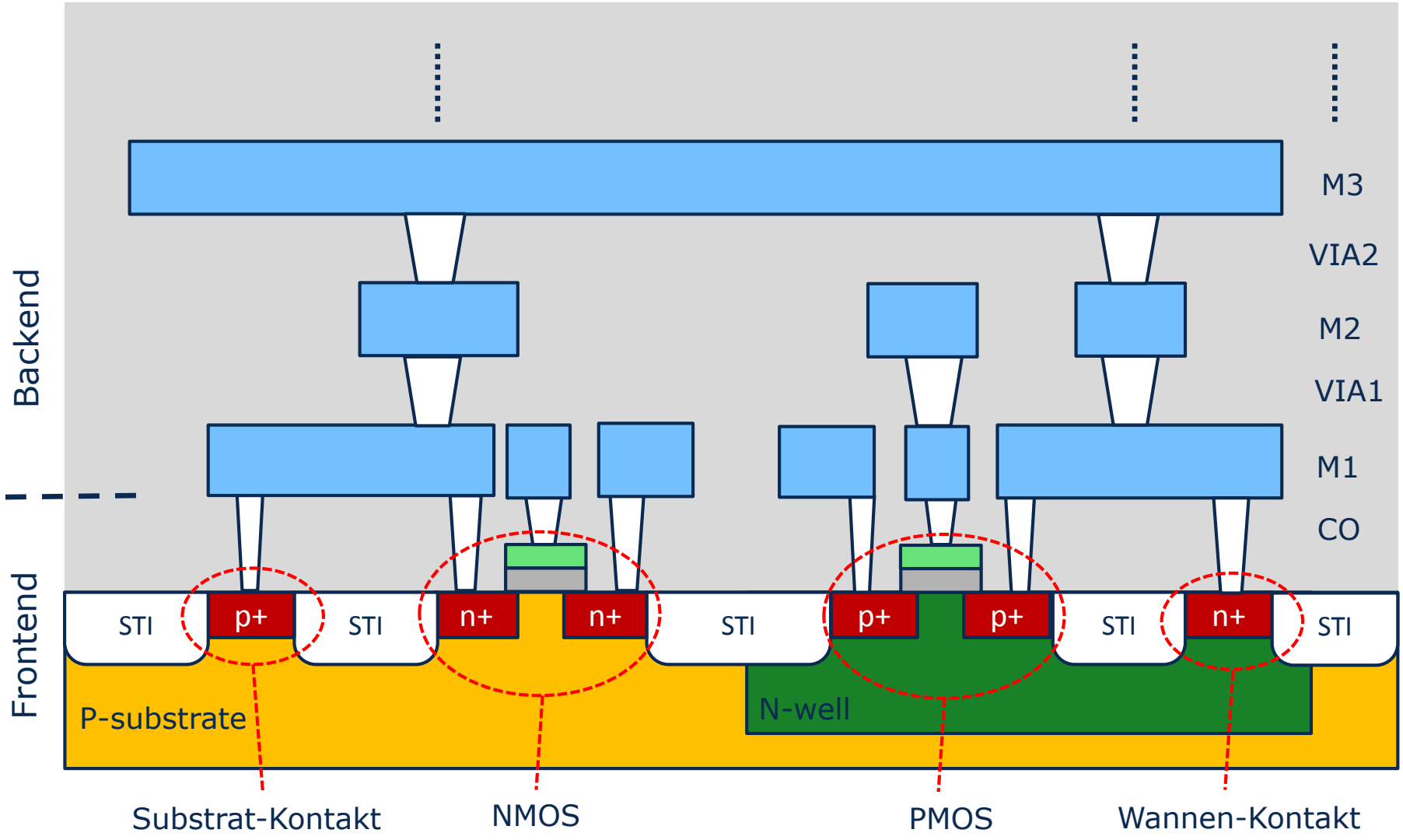
1000 nm

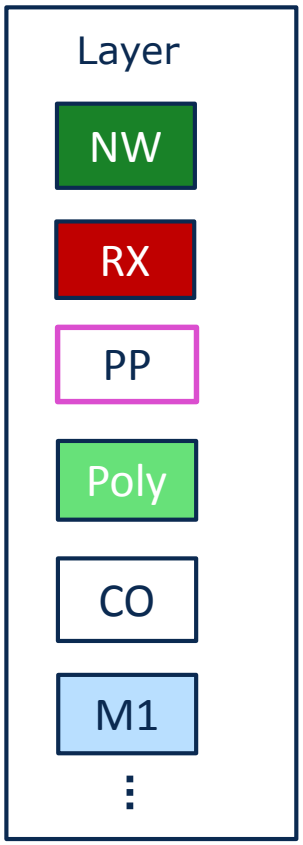


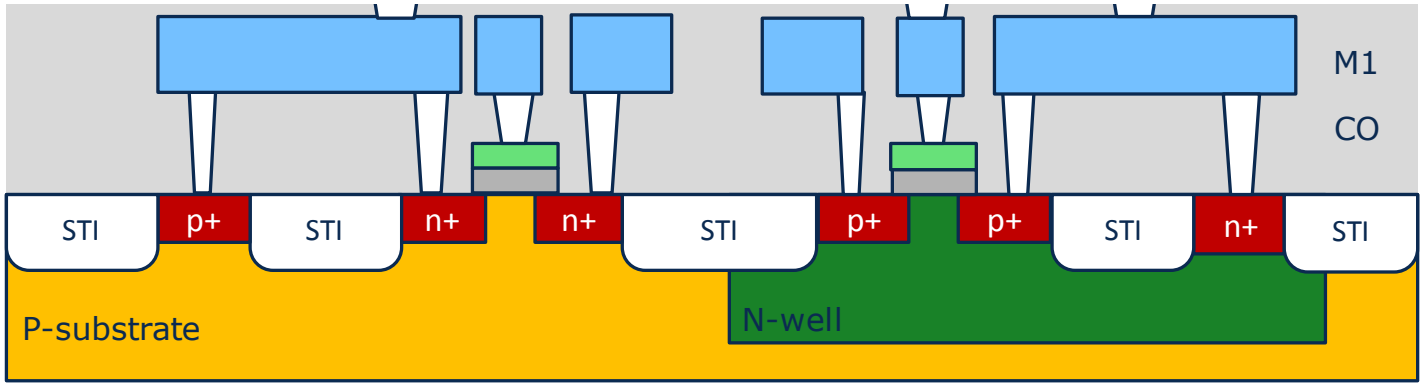
28nm

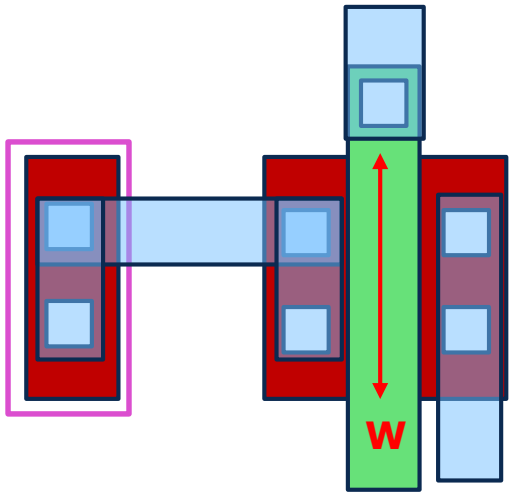
No End of the Road yet

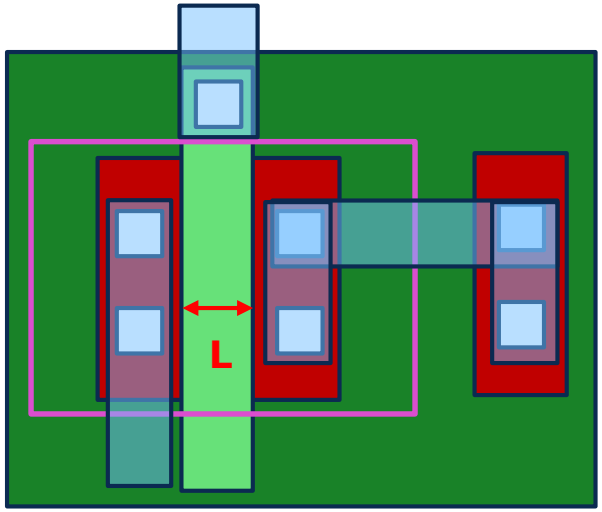
CMOS Querschnitt (Bulk Prozess)







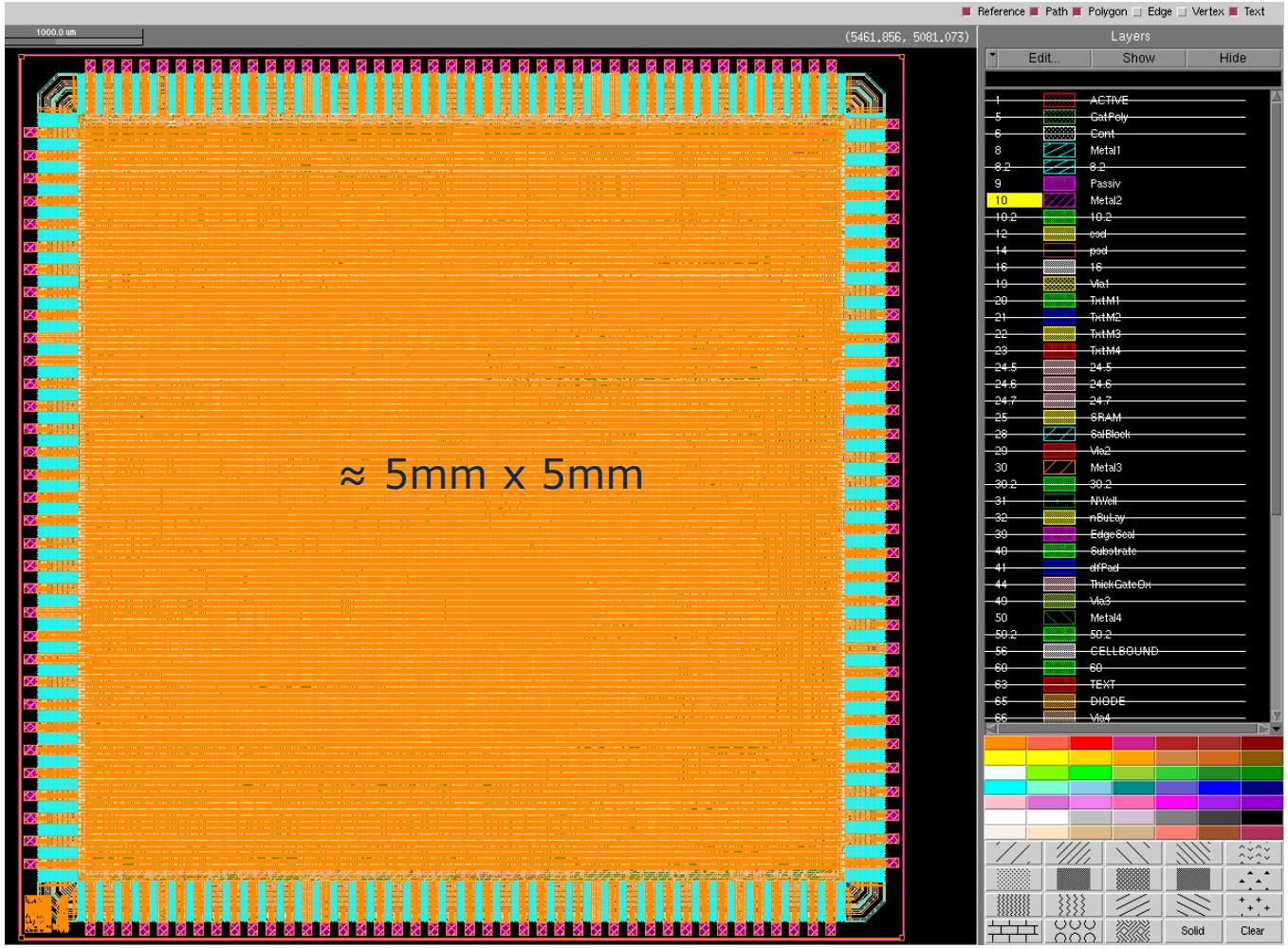




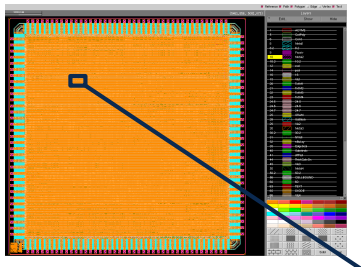
- Freiheitsgrade des Designers beim Schaltungsentwurf/Layoutentwurf:
  - Positionierung und Verdrahtung von NMOS und PMOS Transistoren
  - Transistor Parameter: **W**, **L**

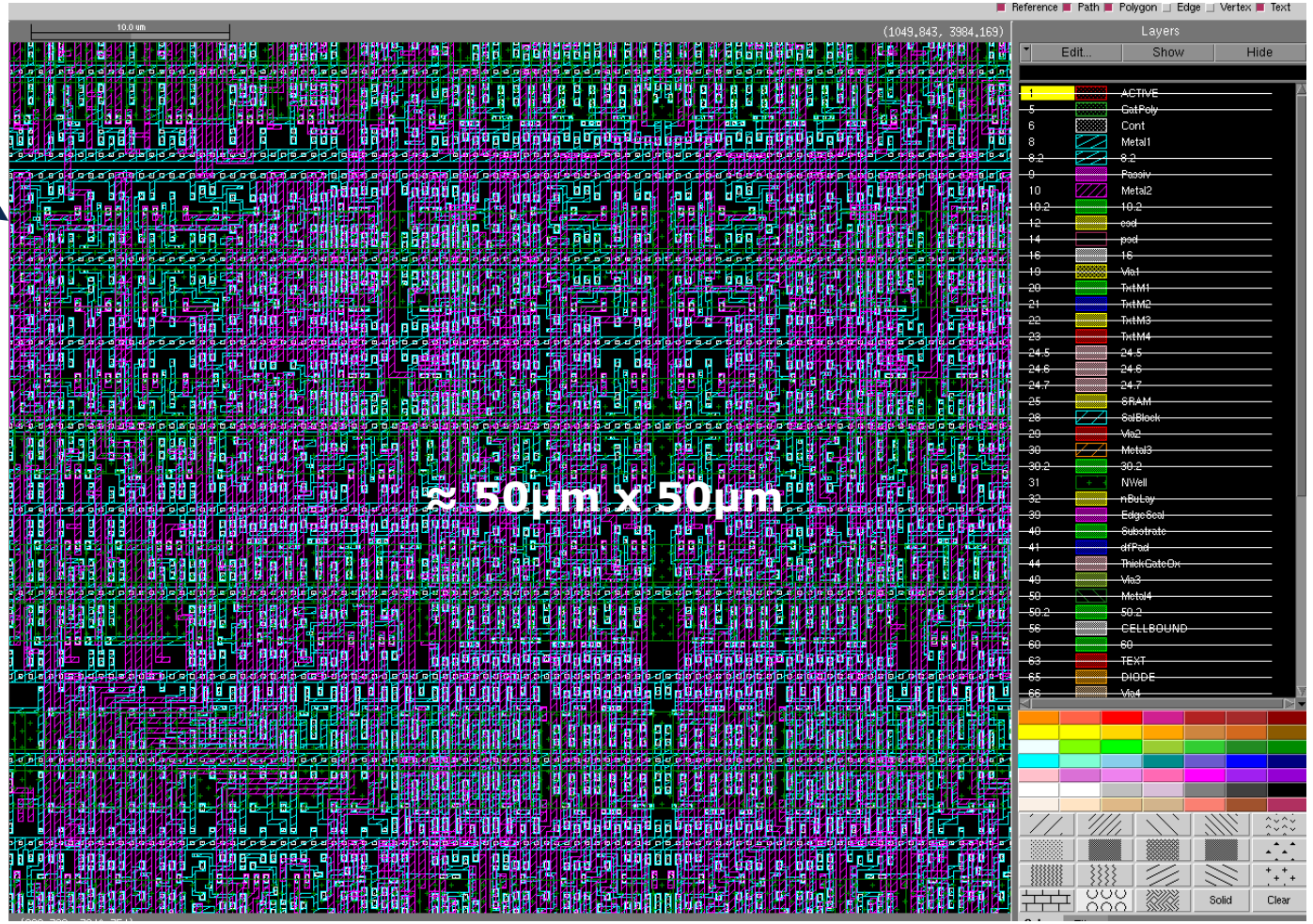
CMOS Layout Beispiel

- Layout zur Herstellung der Masken zur Chip Fertigung

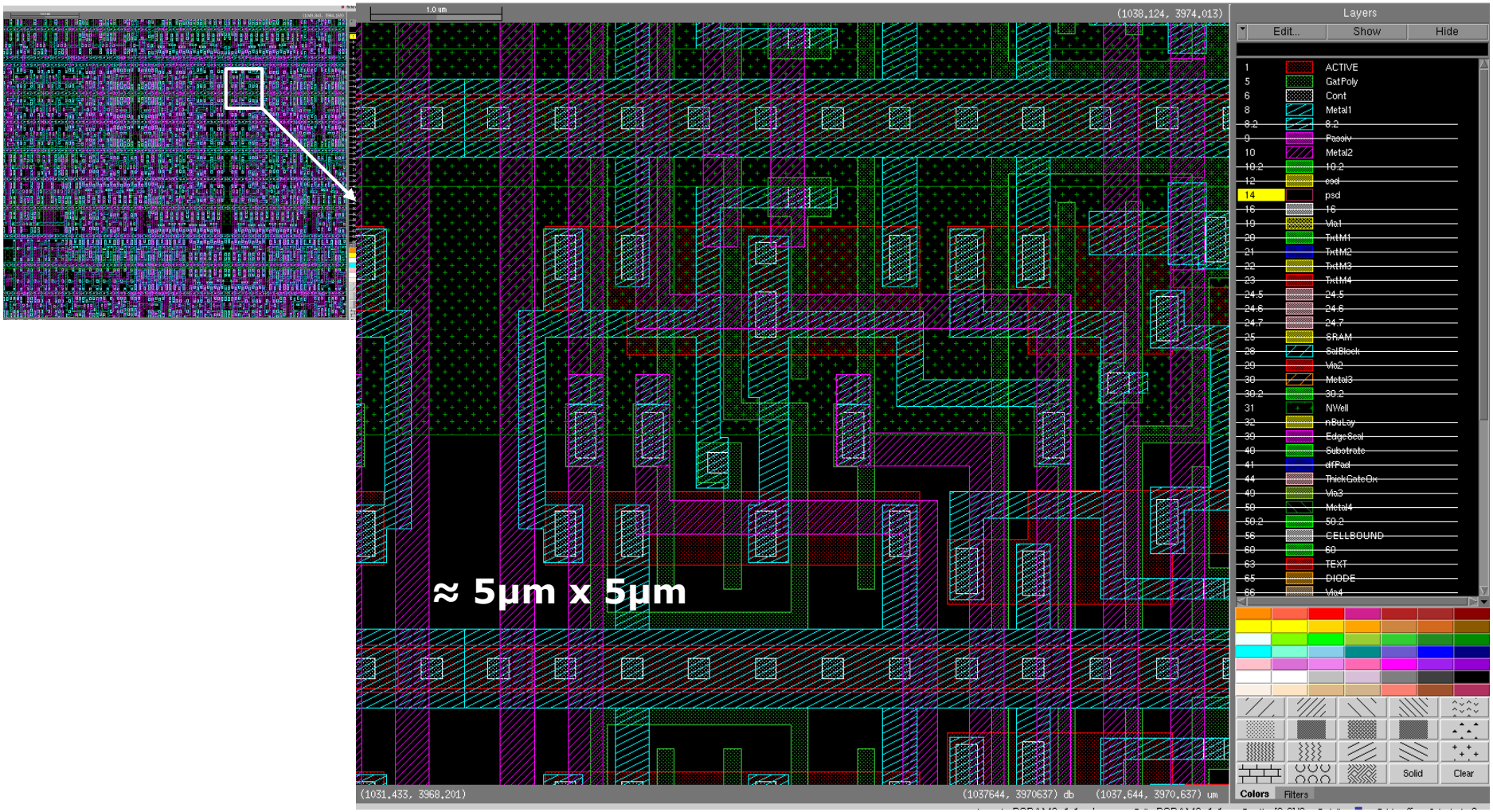


CMOS Layout Beispiel



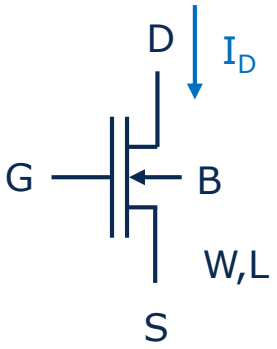


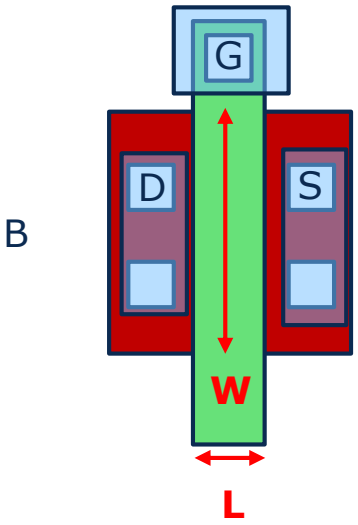
CMOS Layout Beispiel



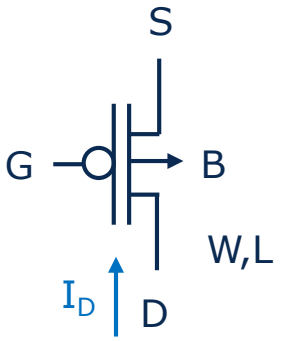
NMOS und PMOS Transistoren

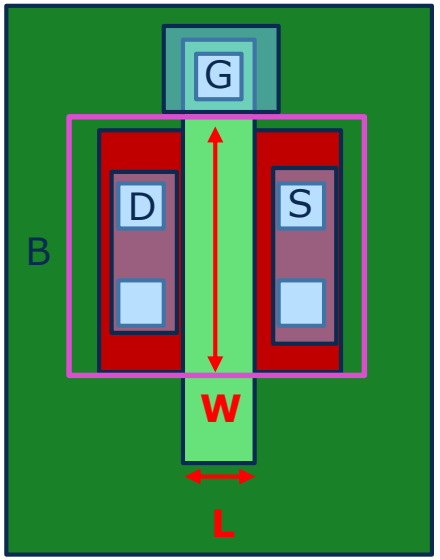
- NMOS Transistor:





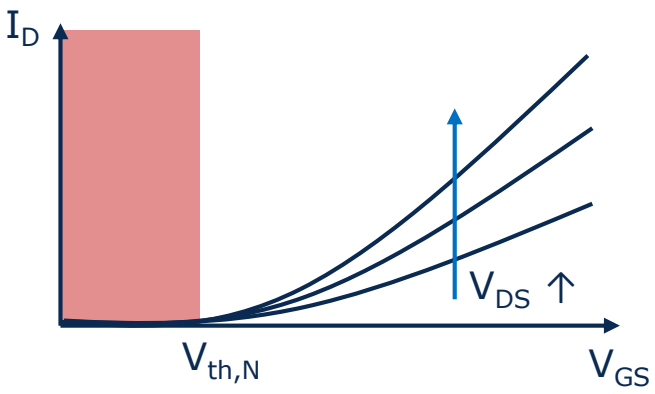
- PMOS Transistor:



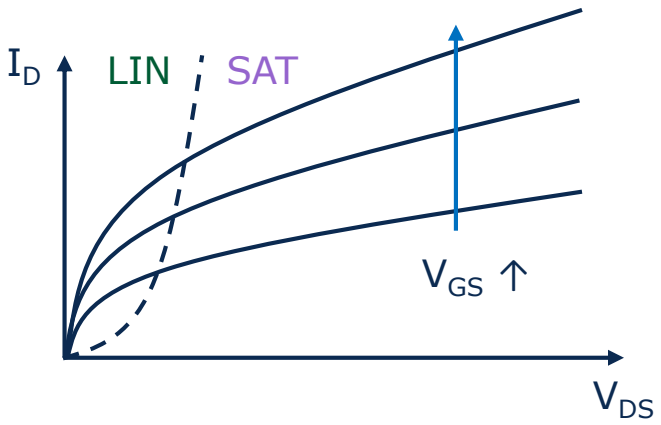


Transistor Kennlinien (NMOS)

Transferkennlinien



Ausgangskennlinien

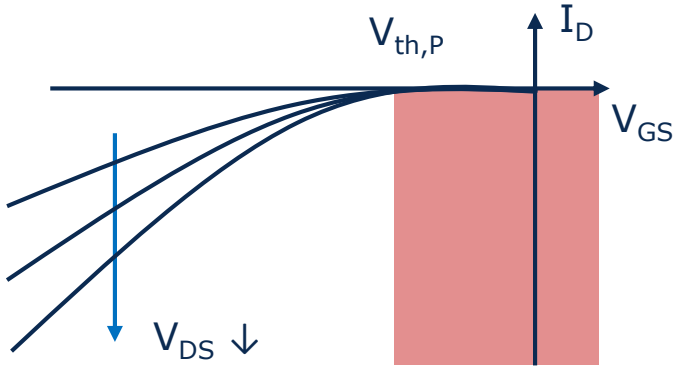


- Sperrbereich: $V_{GS} < V_{th,N}$
  - $I_D = 0$
- Linearer Bereich: $V_{DS} < V_{GS} - V_{th,N}$
  - $I_D = \beta_N\left(\left(V_{GS} - V_{th,N}\right)V_{DS} - \frac{V_{DS}^2}{2}\right)$
- Sättigungsbereich: $V_{DS} \geq V_{GS} - V_{th,N}$
  - $I_D = \frac{\beta_N}{2}\left(V_{GS} - V_{th,N}\right)^2 \cdot (1 + \lambda_N(V_{DS} - V_{GS} + V_{th,N}))$

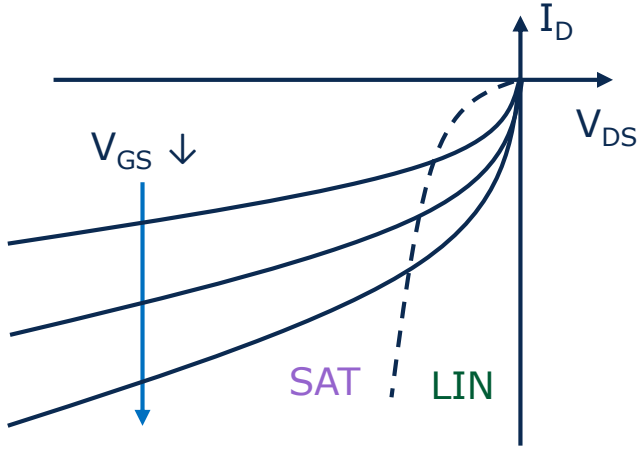
- Schwellspannung:
  - $V_{th,N}(V_{SB}) > 0$
- Steilkeitskonstante:
  - $\beta_N = KP_N \cdot \frac{W}{L} = \mu_N C_{ox} \cdot \frac{W}{L}$
  - $\mu_N > 0$
- Kanallängenmodulation
  - $\lambda_N(L) > 0$

Transistor Kennlinien (PMOS)

Transferkennlinien



Ausgangskennlinien

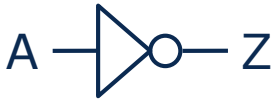


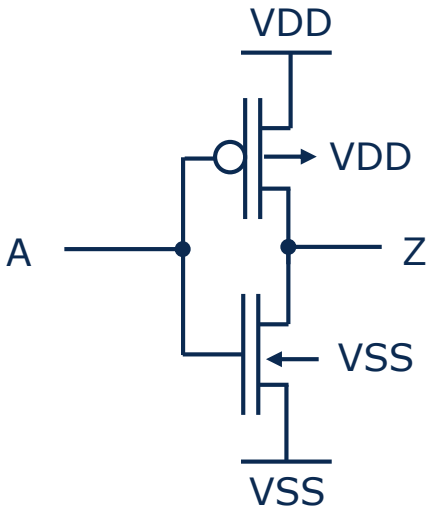
- Sperrbereich: $V_{GS} > V_{th,P}$
  - $I_D = 0$
- Linearer Bereich: $V_{DS} > V_{GS} - V_{th,P}$
  - $I_D = \beta_P((V_{GS} - V_{th,P})V_{DS} - \frac{V_{DS}^2}{2})$
- Sättigungsbereich: $V_{DS} \leq V_{GS} - V_{th,P}$
  - $I_D = \frac{\beta_P}{2}(V_{GS} - V_{th,P})^2 \cdot (1 + \lambda_P(V_{DS} - V_{GS} + V_{th,P}))$

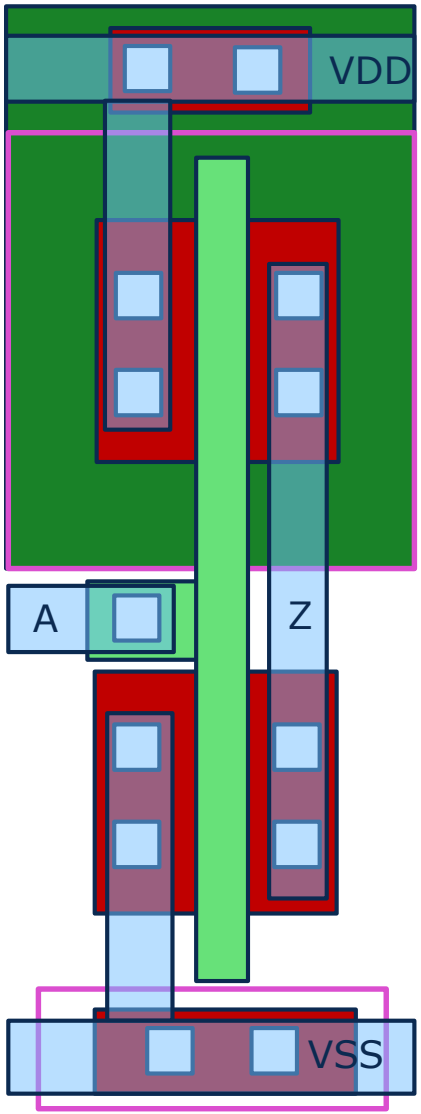
- Schwellspannung:
  - $V_{th,P}(V_{SB}) < 0$
- Steilkeitskonstante:
  - $\beta_P = KP_P \cdot \frac{W}{L} = \mu_P C_{ox} \cdot \frac{W}{L}$
  - $\mu_P < 0$
- Kanallängenmodulation
  - $\lambda_P(L) < 0$

CMOS Inverter

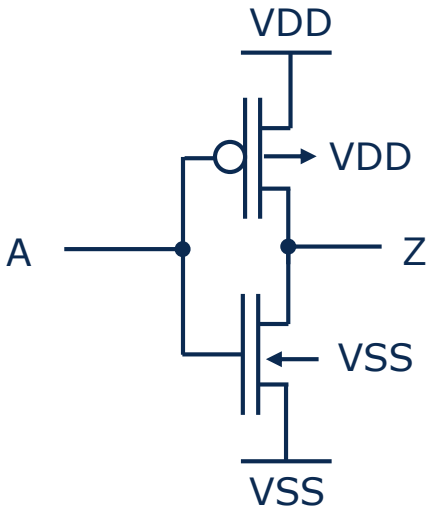
- Grundelement der CMOS Logik

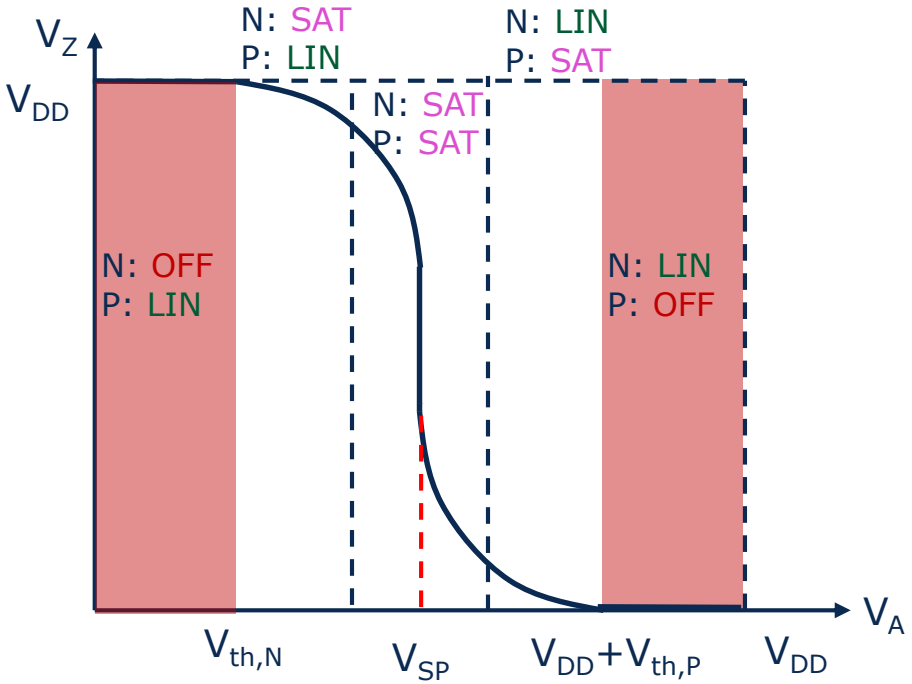






Statische CMOS Inverter Kennlinie





- Berechnung der Schaltschwelle (SP):
- N: SAT, PMOS: SAT (Annahme: λ=0)
  - $I_{D,N} = -I_{D,P}$
  - $\frac{\beta_N}{2}\left(V_{SP} - V_{th,N}\right)^2 = -\frac{\beta_P}{2}\left(V_{SP} - V_{DD} - V_{th,P}\right)^2$
  - $\rightarrow V_{SP} = \frac{(V_{DD}+V_{th,P}) - \sqrt{\frac{\beta_N}{-\beta_P}} \cdot V_{th,N}}{1 - \sqrt{\frac{\beta_N}{-\beta_P}}}$
  - $\rightarrow \frac{-\beta_P}{\beta_N} = \left(\frac{V_{SP} - V_{th,N}}{V_{SP} - V_{DD} - V_{th,P}}\right)^2$

Dimensionierung des CMOS Inverters

- Aufgabe: Dimensionierung der Transistoren für $V_{SP} \approx V_{DD}/2$
- Beispiel:
  - $V_{DD}=1.80V$
  - $V_{th,N}=0{,}40V$
  - $V_{th,P}=-0{,}45V$
  - $KP_N \approx -2{,}5 \cdot KP_P$
  - $L_P=L_N=L_{min}$ (minimale Kanallänge der Technologie)

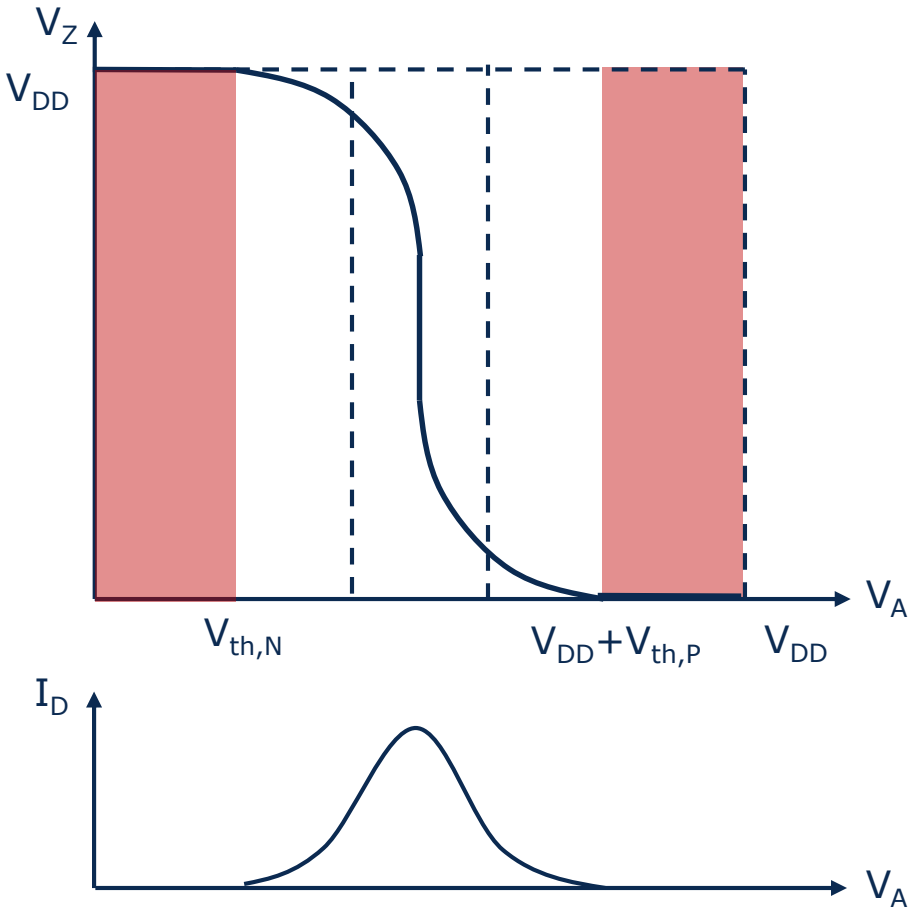
$$\frac{-\beta_P}{\beta_N} = \frac{-KP_P}{KP_N} \cdot \frac{L \cdot W_P}{L \cdot W_N} = \left(\frac{V_{SP}-V_{th,N}}{V_{SP}-V_{DD}-V_{th,P}}\right)^2$$

$$\frac{W_P}{W_N} = \frac{KP_N}{-KP_P} \cdot \left(\frac{V_{SP}-V_{th,N}}{V_{SP}-V_{DD}-V_{th,P}}\right)^2 \rightarrow \frac{W_P}{W_N} \approx 3{,}0$$

- → Statischer Ansatz zur Dimensionierung
- Dynamischer Ansatz → siehe Abschnitt CMOS Delays

CMOS Inverter Kennlinie: Statische Stromaufnahme

- Keine statische Stromaufnahme im geschalteten Zustand (Ausnahme Leckströme)
- Statische intrinsische Stromaufnahme (short circuit power) während des Umschaltvorgangs
- Details: → Abschnitt CMOS Verlustleistung

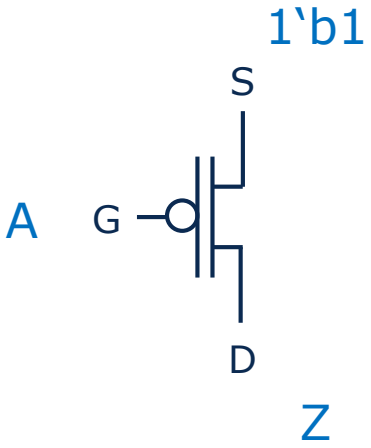


CMOS Logik

Formalisierung von CMOS Schaltungen; PMOS

- Idealisierung des Schaltverhaltens zur Beschreibung von Logik
- Annahmen:
  - CMOS Logikpegel VSS (1‘b0); VDD (1‘b1)
  - keine statischen Ströme

- Pull-Up Schalter (PMOS):
  - wenn V_G-V_S<$V_{th,P}$ (V_S-V_G>-$V_{th,P}$) , dann V_{DS}=0
  - sonst: DS Kanal hochohmig (1‘bz)

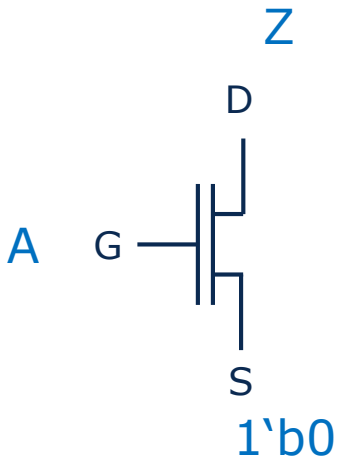


- Pull-up Funktion:
  - $Z = \bar{A}$, wenn A=1‘b0 und S=1‘b1

PMOS D		G	
		0	1
S	0	0	z
	1	1	z

Formalisierung von CMOS Schaltungen; NMOS

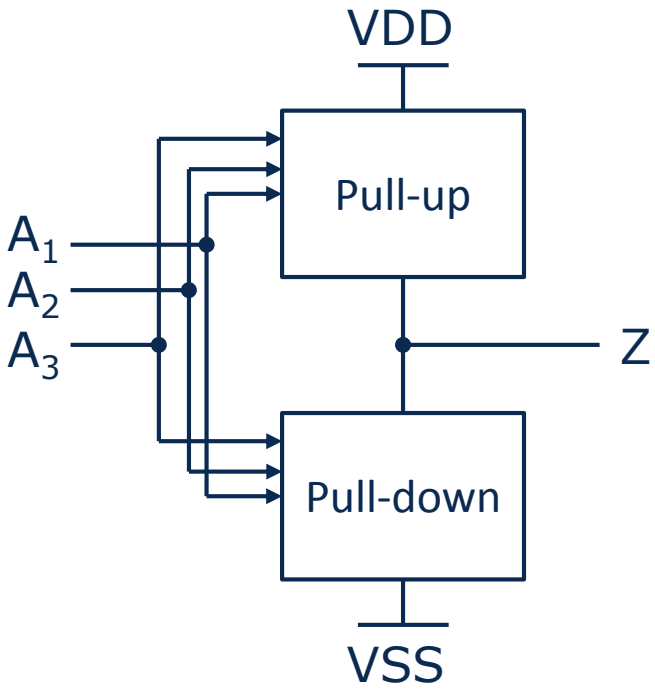
- Pull-Down Schalter (NMOS):
  - wenn V_G-V_S>$V_{th,N}$, dann V_{DS}=0
  - sonst: DS Kanal hochohmig (1‘bz)



- Pull-down Funktion:
  - $\bar{Z} = A$, wenn A=1‘b1 und S=1‘b0

NMOS D		G	
		0	1
S	0	z	0
	1	z	1

- Pull-Up Netzwerke (PMOS):
  - $Z = \boldsymbol{F}(\overline{A_1}, \overline{A_2}, \overline{A_3}, \dots)$
- Pull-Down Netzwerke (NMOS):
  - $\bar{Z} = \boldsymbol{G}(A_1, A_2, A_3, \dots)$
- **UND** Verknüpfung durch Reihenschaltung von Transistoren
- **ODER** Verknüpfung durch Parallelschaltung von Transistoren

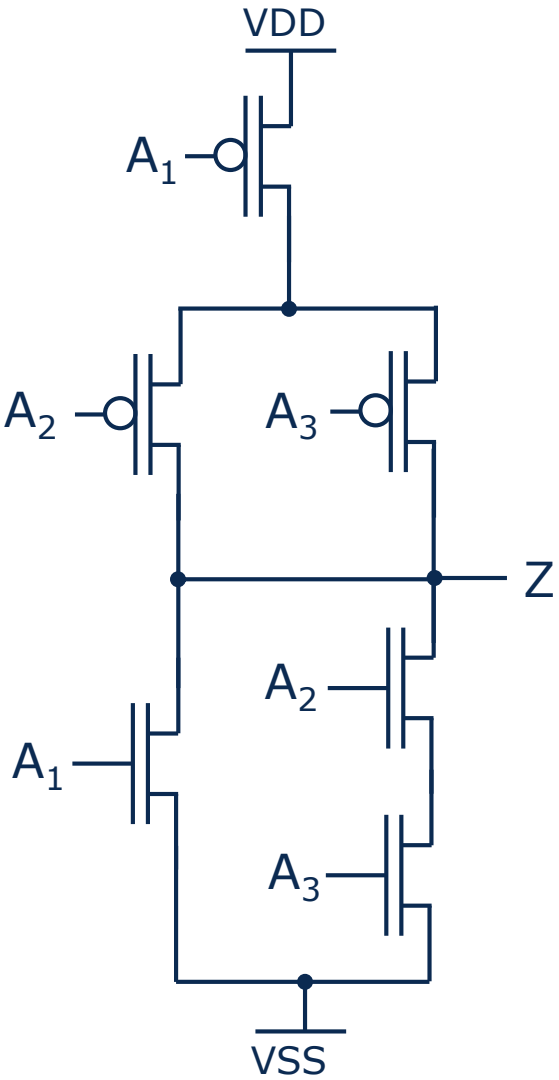


CMOS Logik Beispiel 1

- Logikfunktion: $\bar{Z} = A_1 + A_2 A_3$

- Pull-Up Netzwerk:
  - $Z = \overline{A_1 + A_2 A_3} = \overline{A_1} \cdot (\overline{A_2} + \overline{A_3})$

- Pull-Down Netzwerk:
  - $\bar{Z} = A_1 + A_2 A_3$



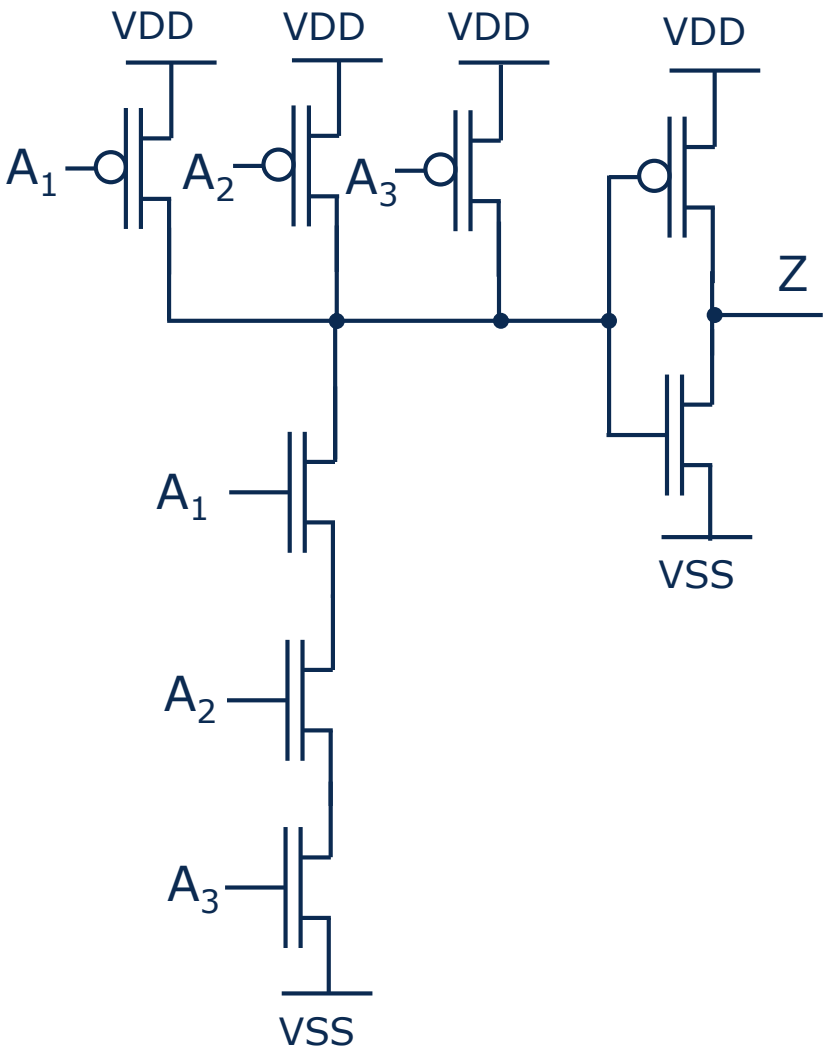
→ AOI12 Gatter

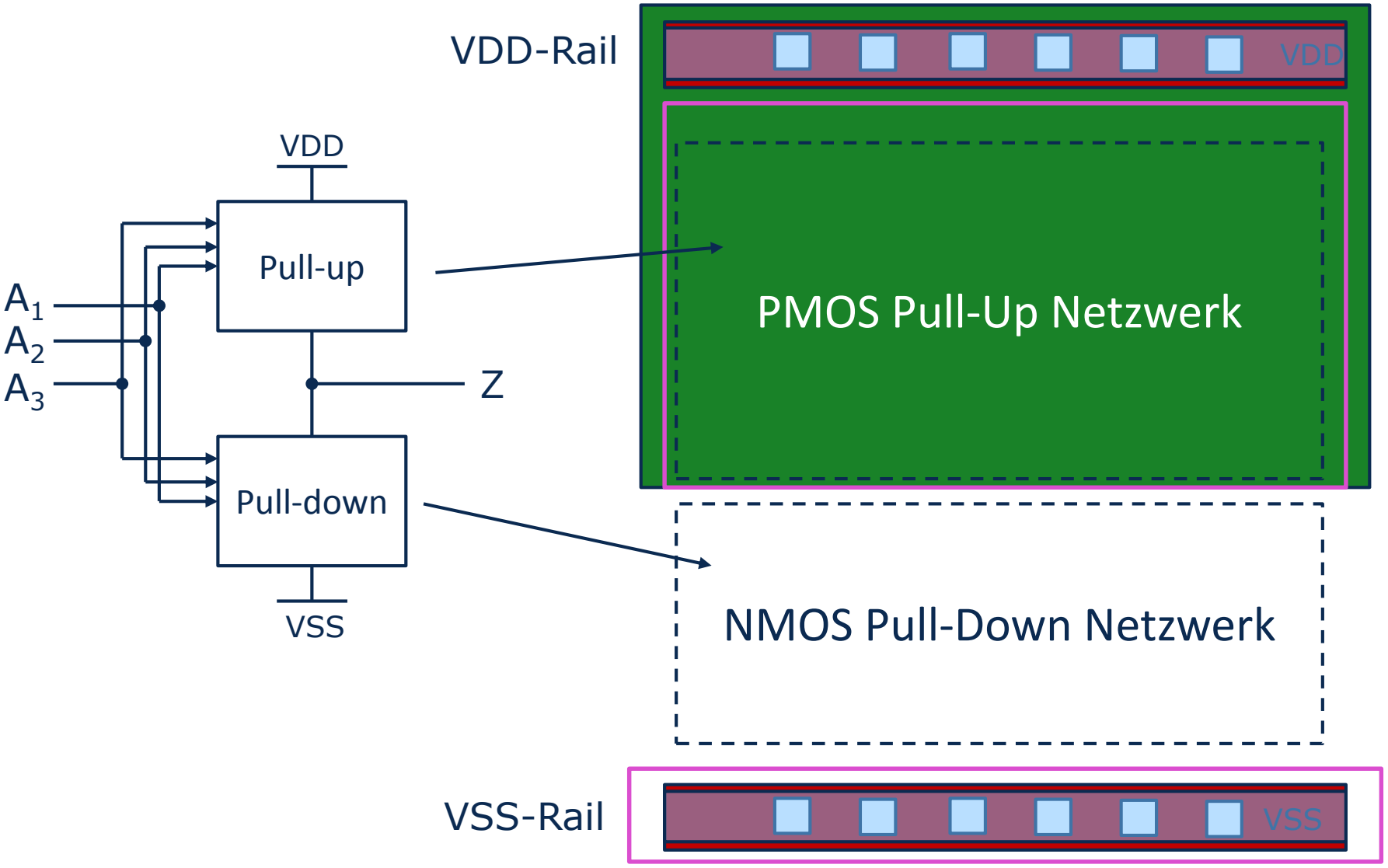
- Logikfunktion: $Z = A_1 A_2 A_3$

- Pull-Up Netzwerk:
  - $Z = \overline{\overline{A_1 A_2 A_3}} = \overline{(\overline{A_1} + \overline{A_2} + \overline{A_3})}$

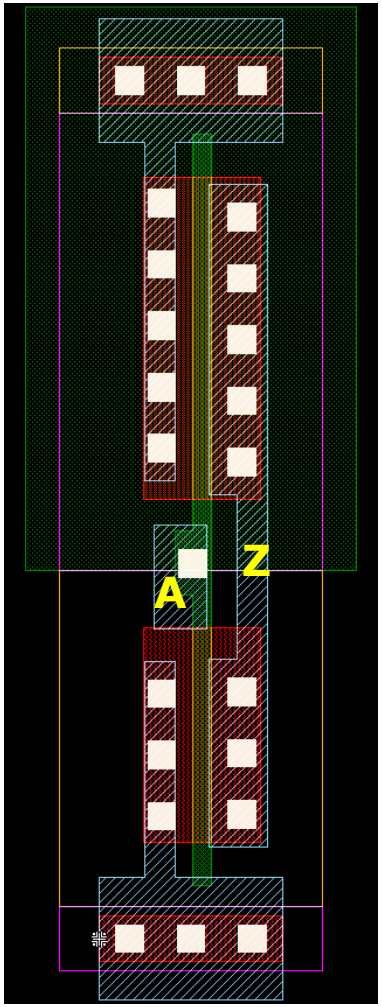
- Pull-Down Netzwerk:
  - $\bar{Z} = \overline{A_1 A_2 A_3}$

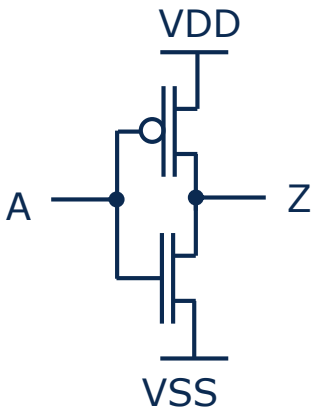
→ AND3 Gatter

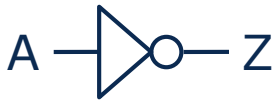



VDD-Rail
VDD
VDD
Pull-up
A_1
A_2
A_3
Z
PMOS Pull-Up Netzwerk
Pull-down
NMOS Pull-Down Netzwerk
VSS
VSS-Rail
VSS

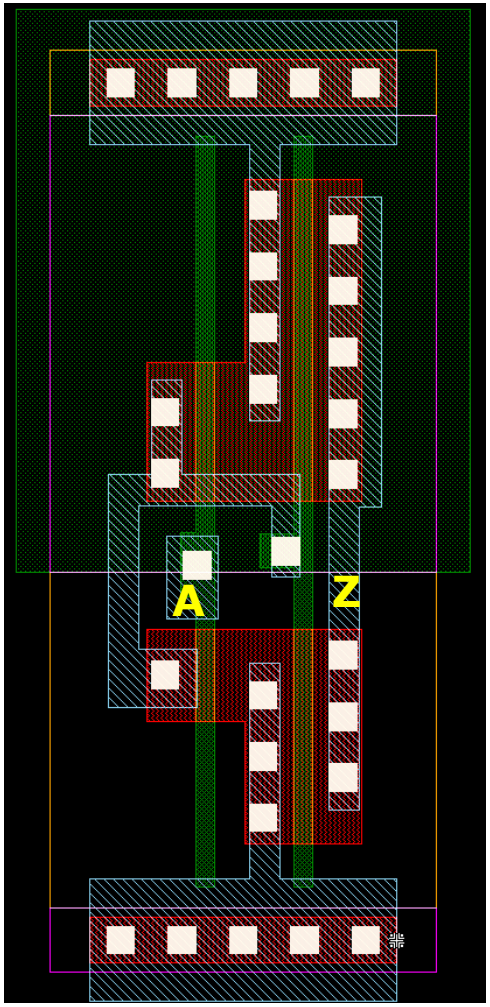
CMOS Gatter Beispiele 1

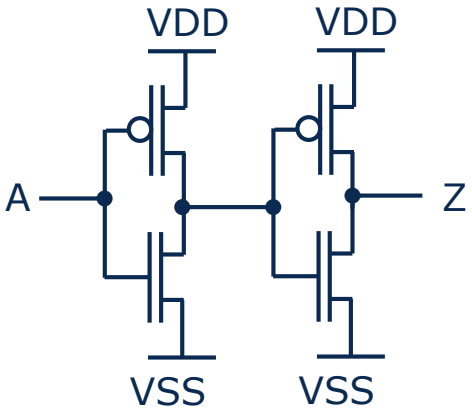


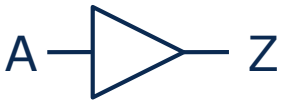




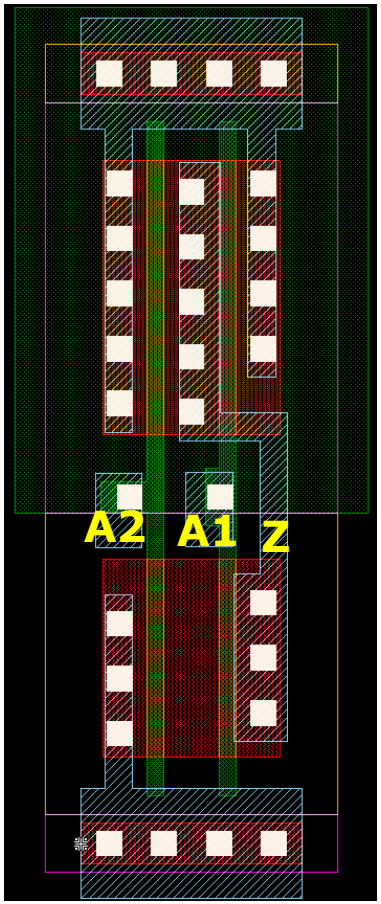
Inverter

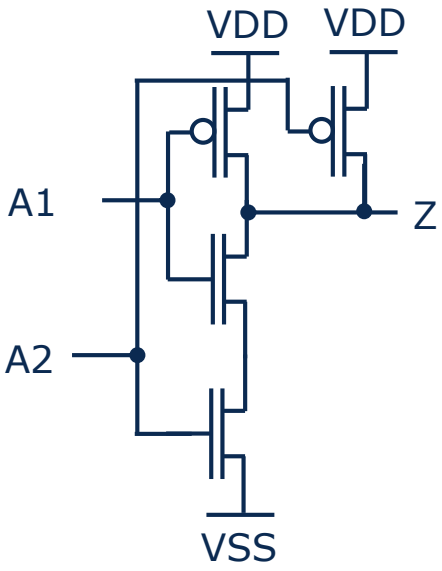






Buffer





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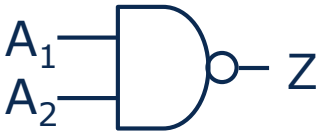
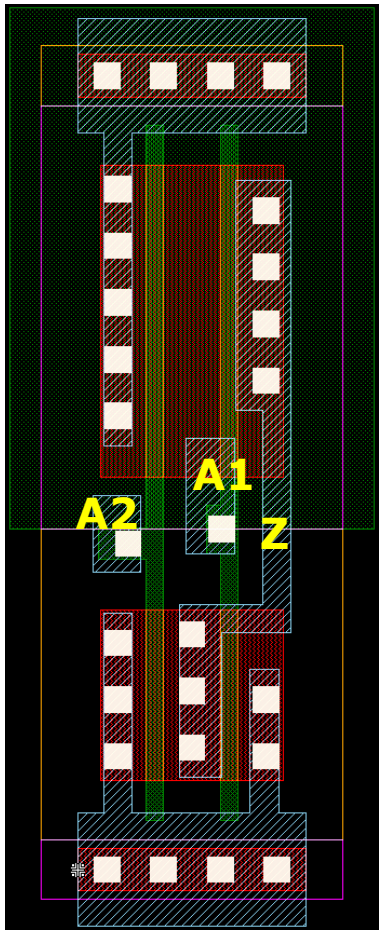
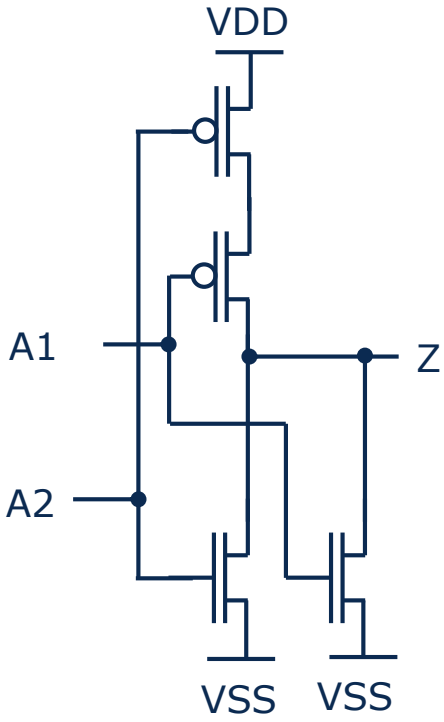
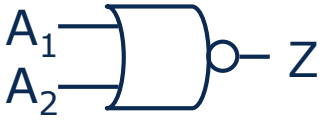


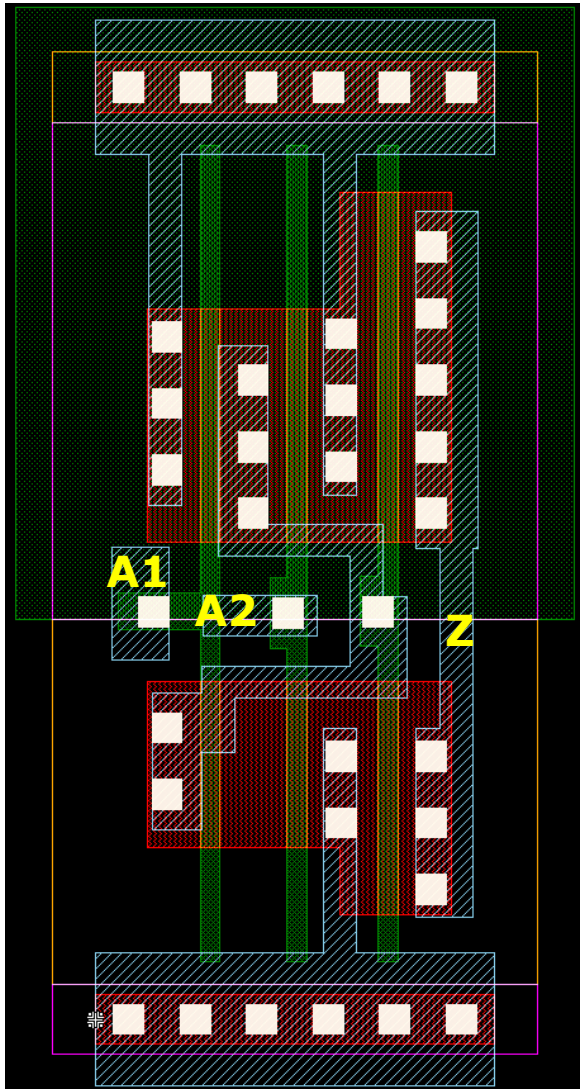


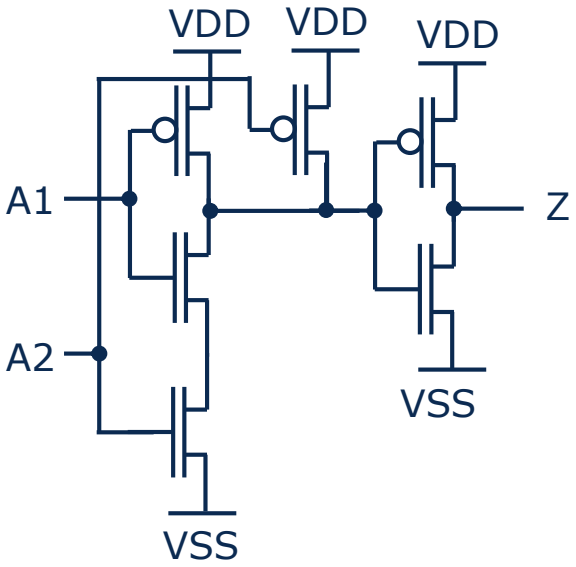


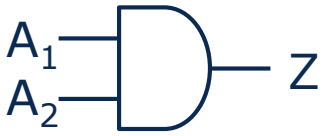
NOR2



CMOS Gatter Beispiele 3

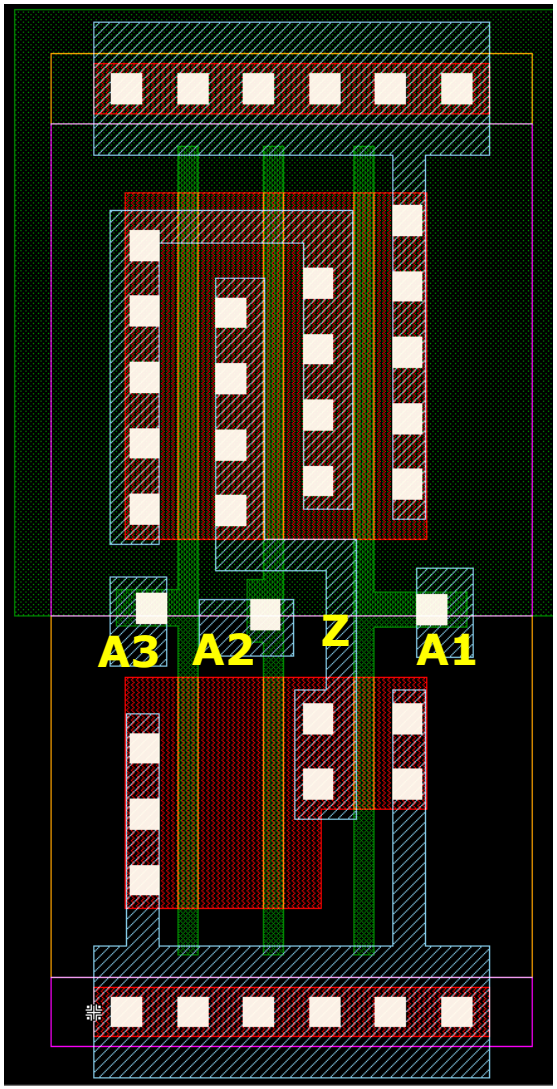


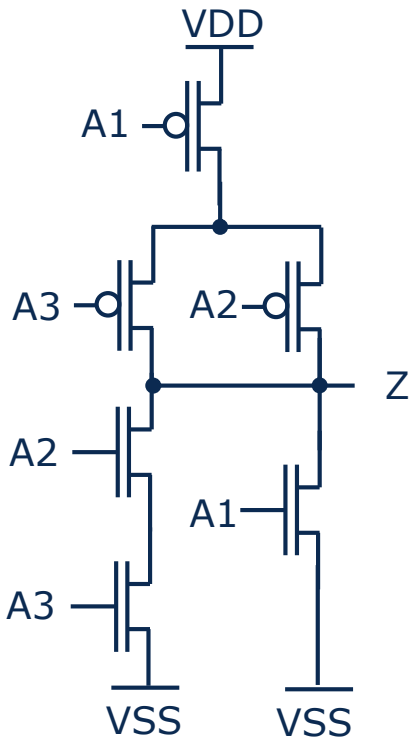


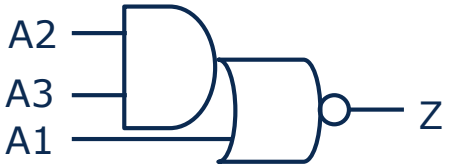


AND2

CMOS Gatter Beispiele 4

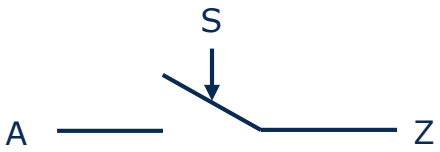




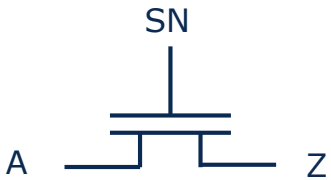


AOI2

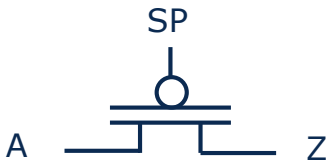
- Aufgabe: Realisierung eines gesteuerten Schalters zum Verbinden zweier Signalnetze

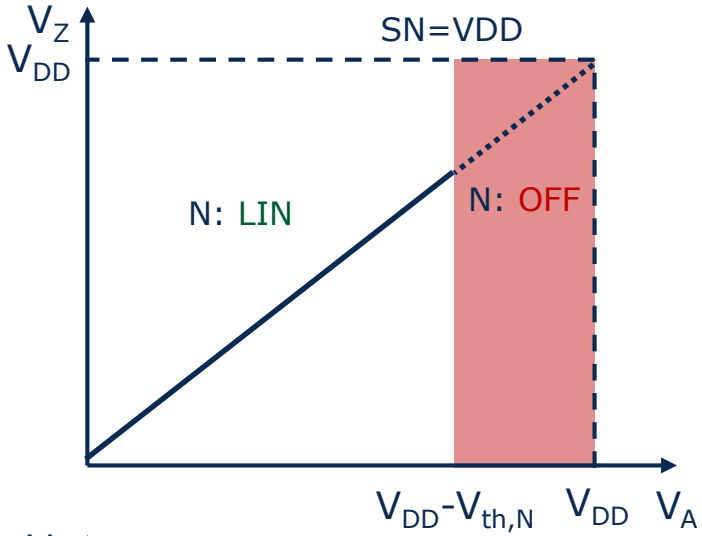


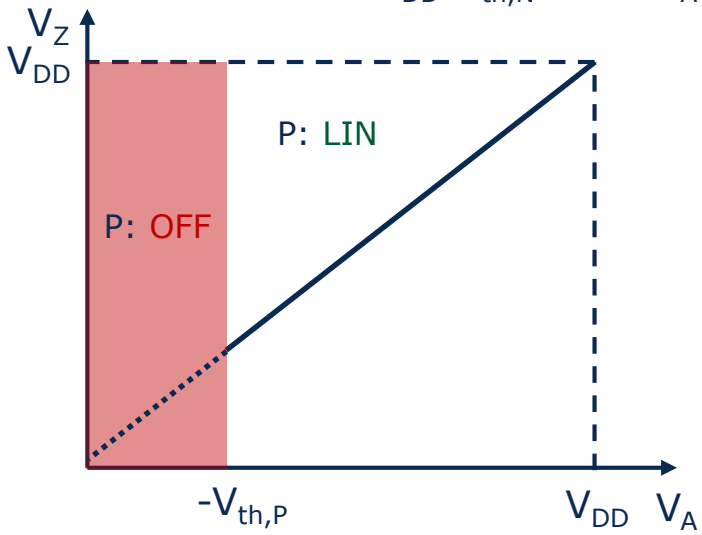
- **NMOS Schalter**
  - Niederohmiges Schalten von Signalen von V_{SS} bis V_{DD}-$V_{th,N}$



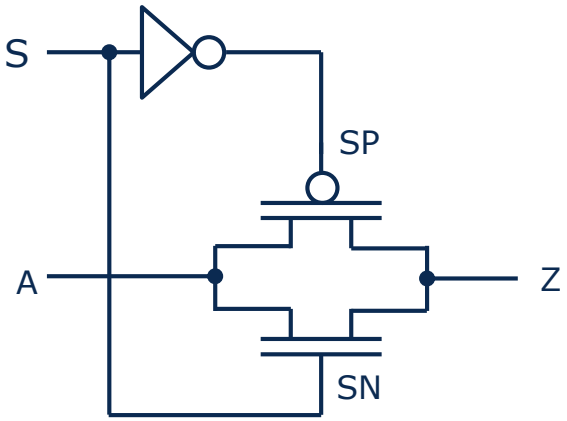
- **PMOS Schalter**
  - Niederohmiges Schalten von Signalen von $-V_{th,P}$ bis V_{DD}

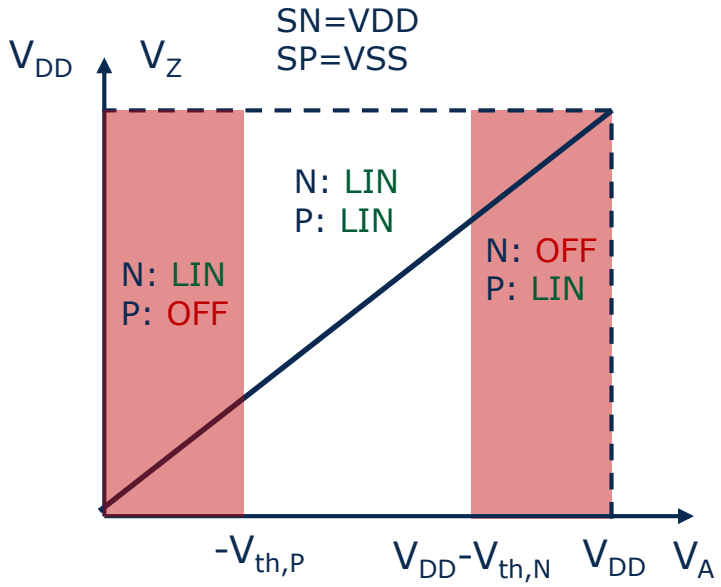




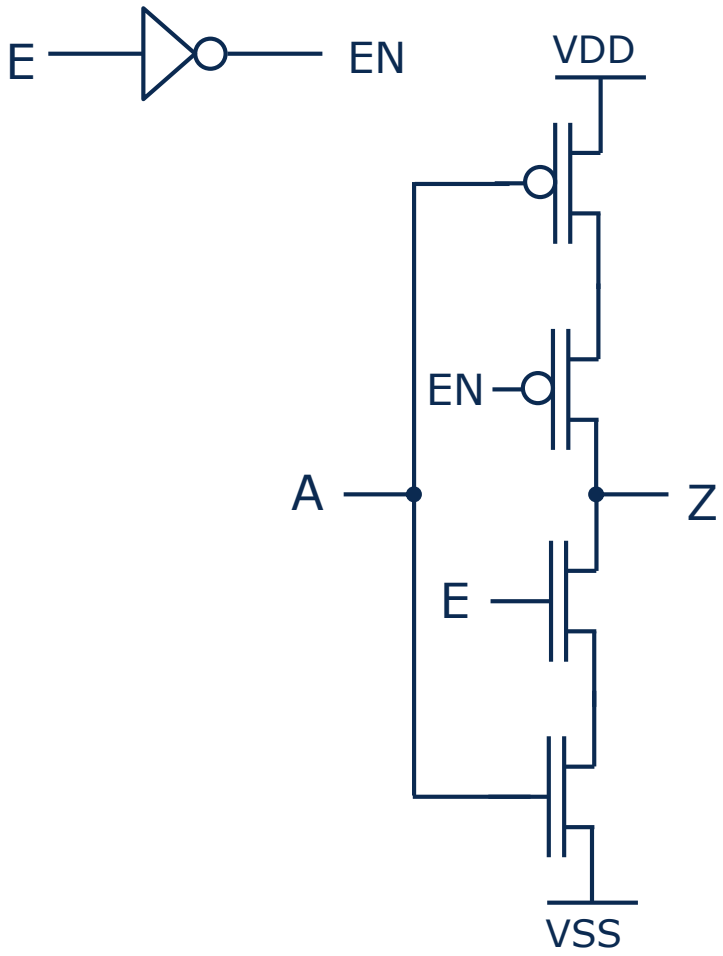


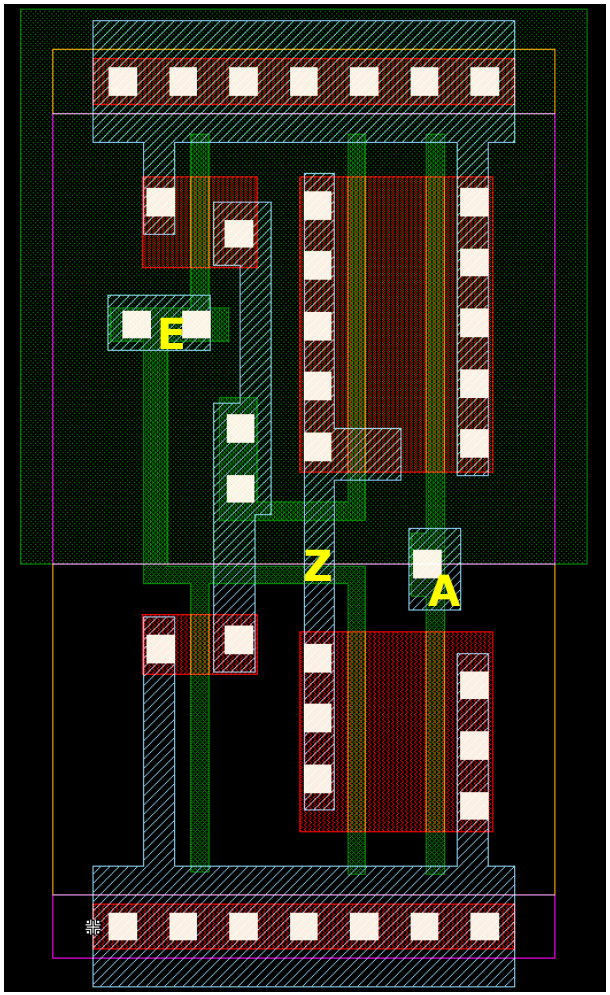
- Parallelschaltung von NMOS und PMOS Schaltern
- Ermöglicht niederohmiges Schalten über den kompletten Spannungsbereich





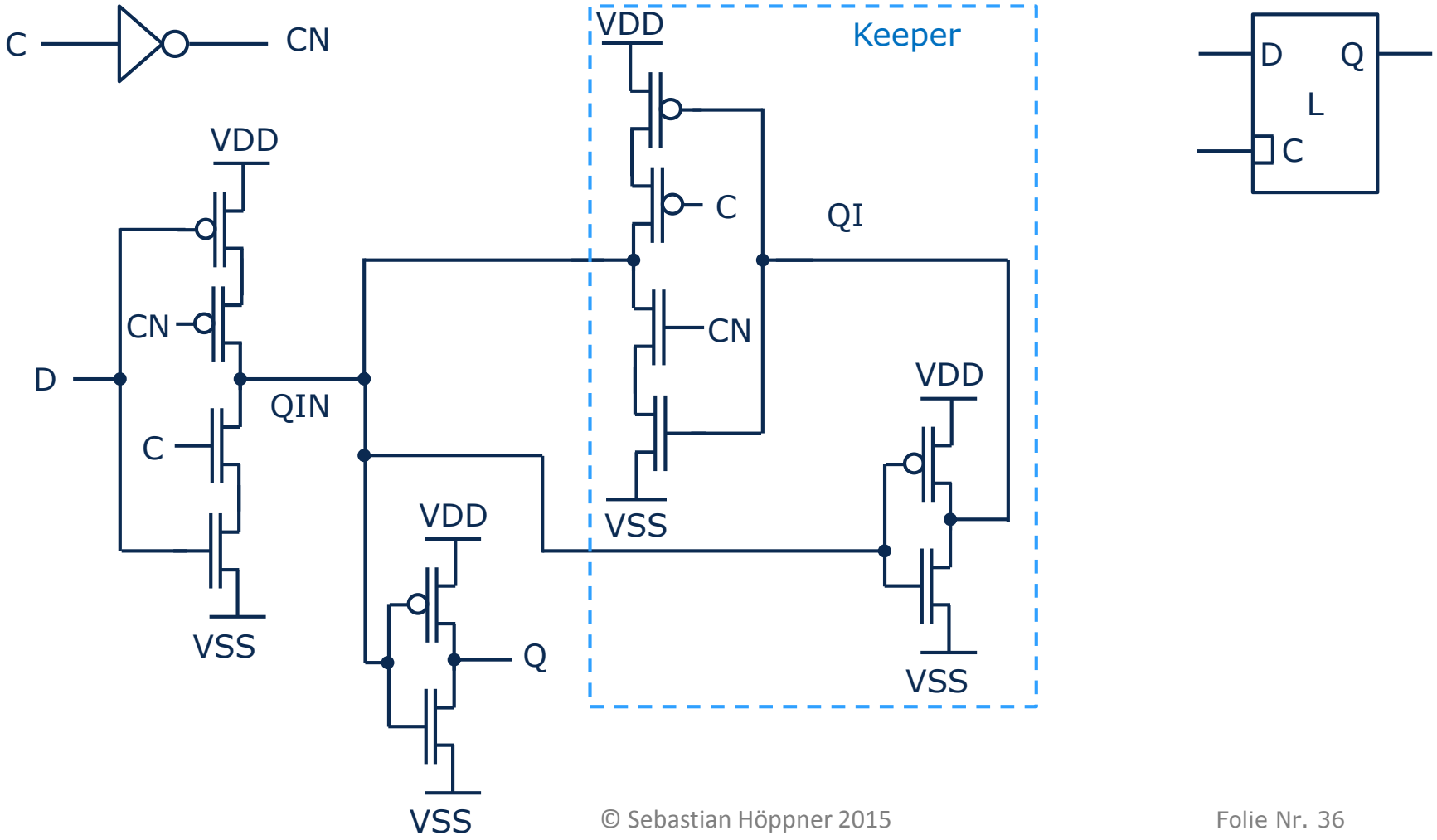
- Zusätzliches Enable/Disable (Tri-State) für Pull-Up und Pull-Down Pfade



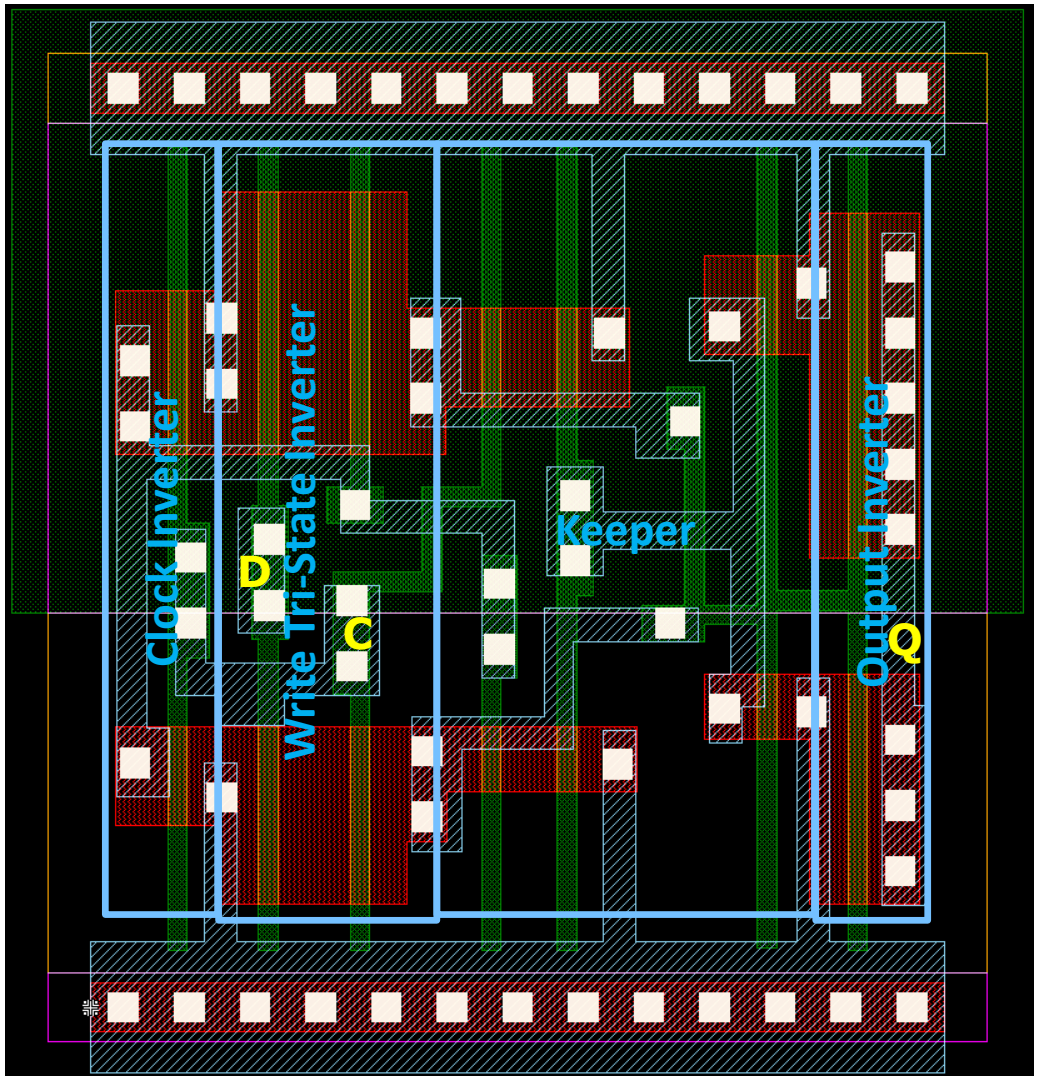


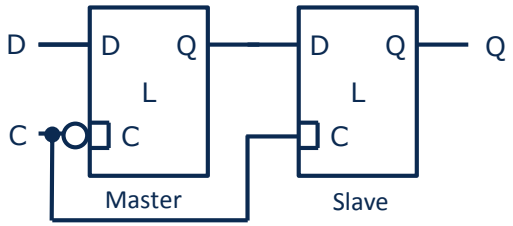
D-Latch

- Realisierung von des Schreibvorgangs auf einen Speicherknoten durch Tri-State Treiber
- Rückkopplung durch statische CMOS Logik → Keeper
  - Statischer Speicher → Kompensation von Leckströmen

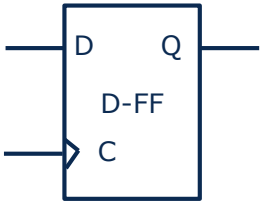


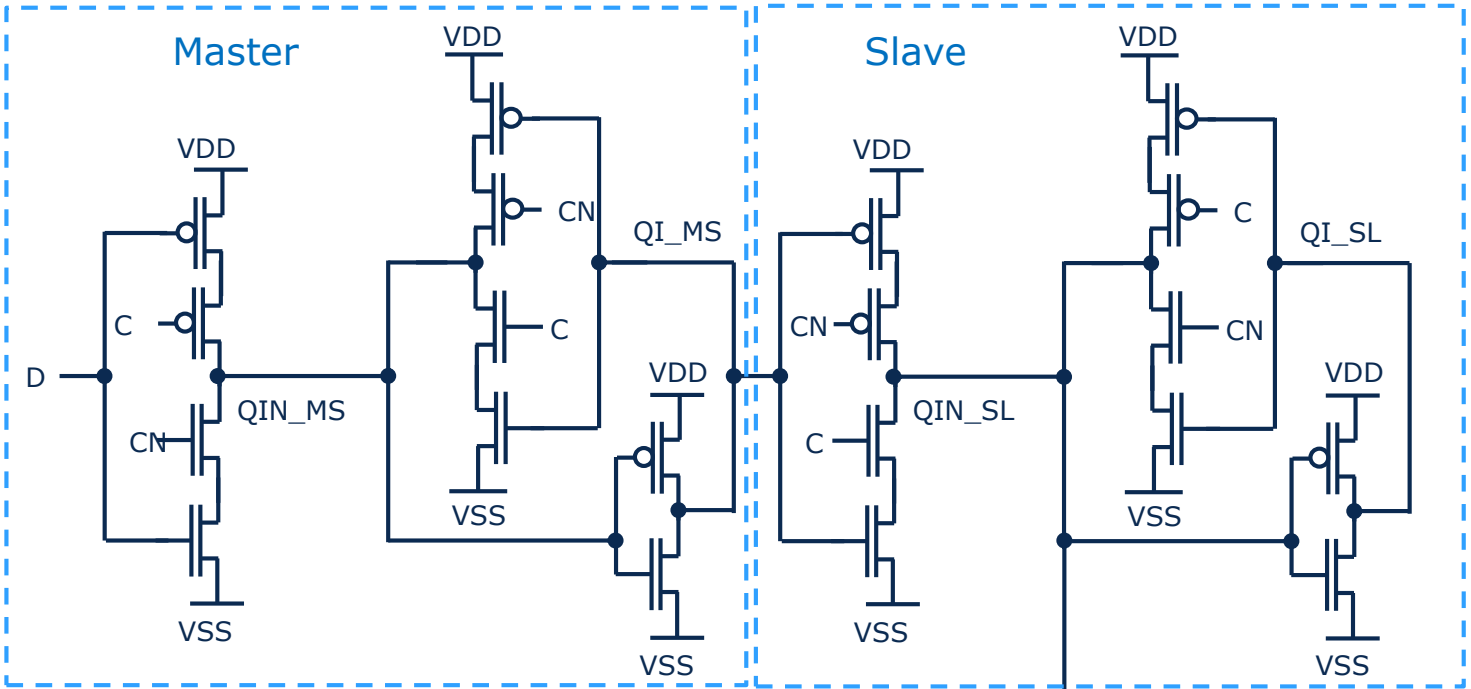
D-Latch Layout

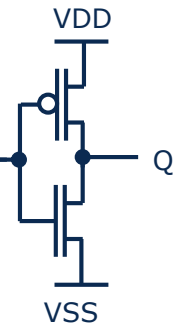




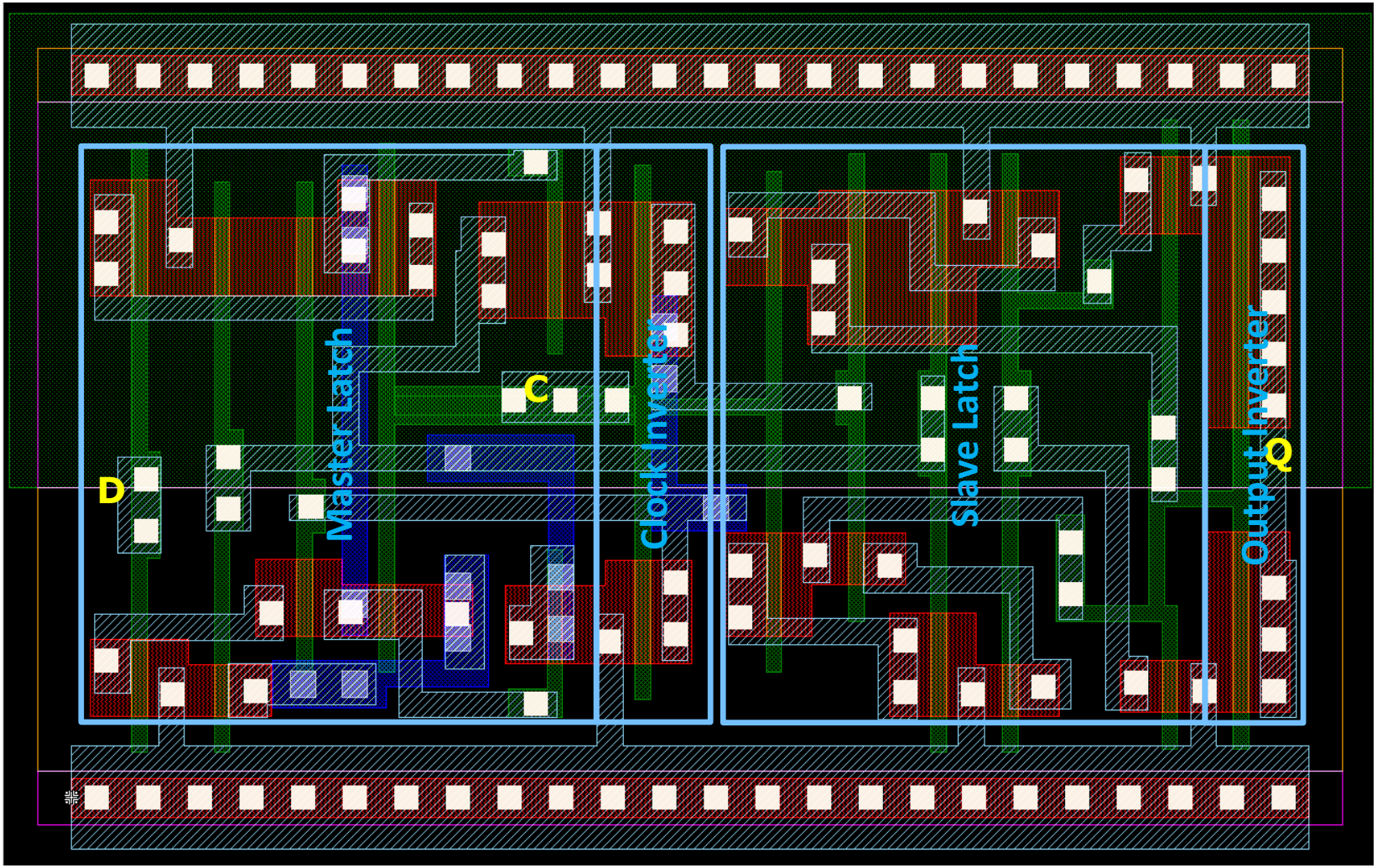
D-FlipFlop







D-FlipFlop Layout



Zusammenfassung

- Vorstellung der CMOS Technologie aus Sicht des Designers
- Vermittlung von Grundlagen zu
  - NMOS und PMOS Transistoren
  - CMOS Logik
- zur Realisierung statischer CMOS Logik (kombinatorisch, sequentiell) in Schaltplan und Layout