Schaltkreis- und Systementwurf

Teil 4: Digitale CMOS Schaltungen

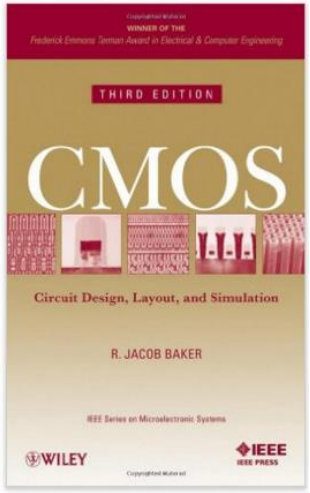
Inhalt

- CMOS Technologie und CMOS Logik

→ Details siehe Vorlesung digitale Schaltungstechnik

- **Vertiefung:** Timing von CMOS Schaltungen
- **Vertiefung:** Verlustleistung von CMOS Schaltungen
- Standardzellenbibliotheken und SRAM Compiler
- I/O Schaltungen

- Ergänzende Vorlesungen:
  - Elektronische Bauelemente
  - Halbleitertechnologie
  - Schaltungstechnik
- Weiterführende Vorlesungen:
  - VLSI Prozessorentwurf
  - Neuromorphe VLSI-Systeme

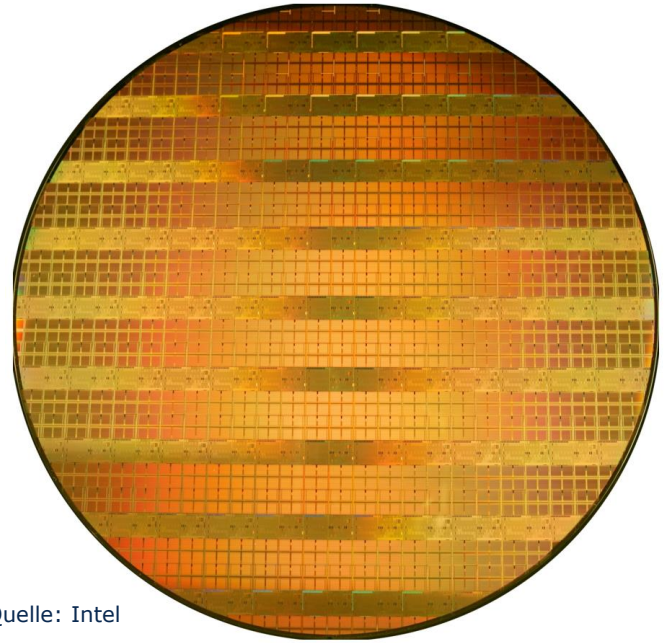


- Literaturempfehlungen:
  - CMOS, Circuit Design, Layout and Simulation; R. Jacob Baker; IEEE Press Series on Microelectronic Systems, 3rd Edition, 2011
  - Halbleiter-Schaltungstechnik; Ulrich Tietze, Christoph Schenk; Springer; 2002

CMOS Technologie

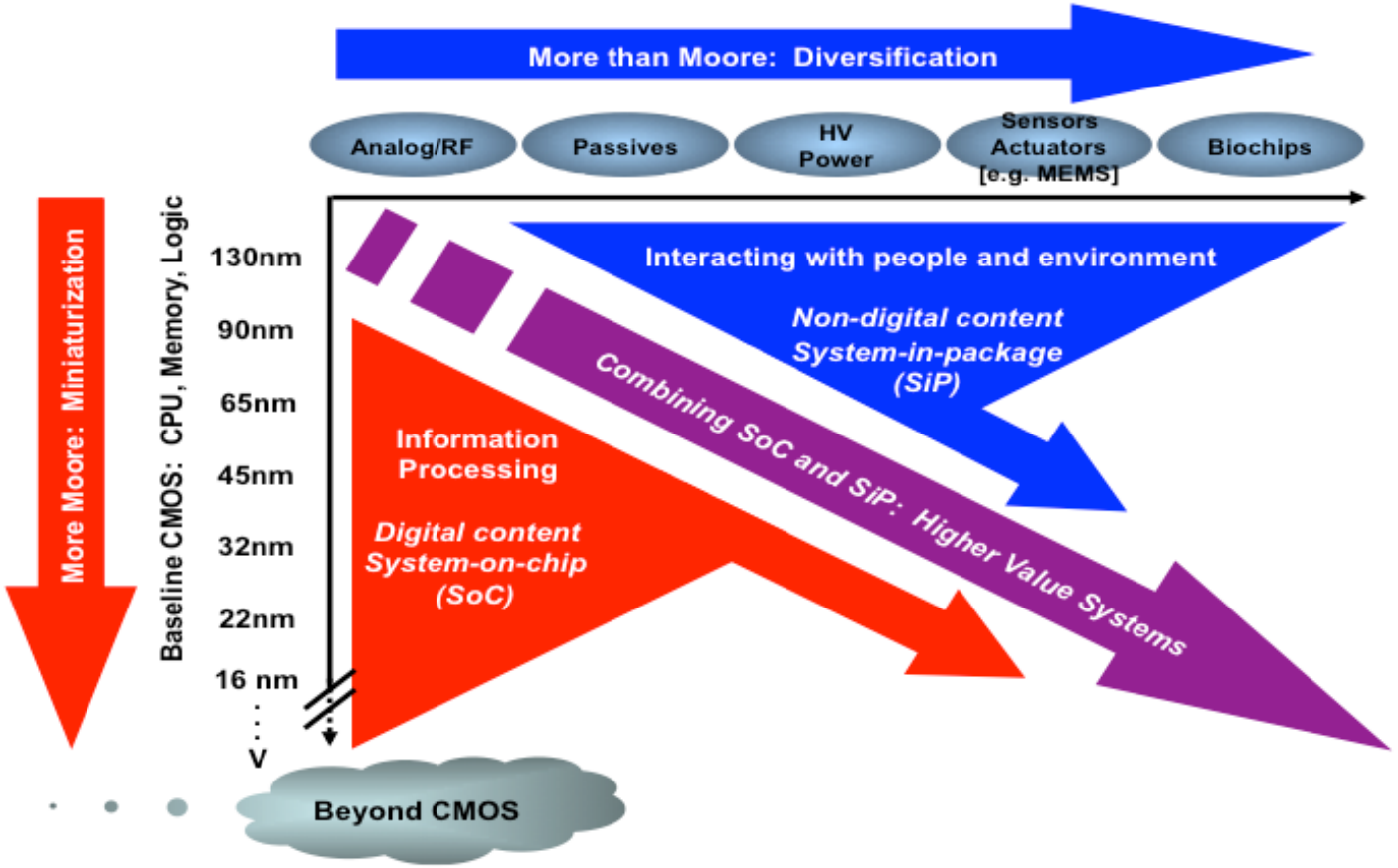
CMOS Technologie

- Complementary Metal Oxide Semiconductor (CMOS) Technologie
- Integration von n-Kanal (NMOS) und p-Kanal (PMOS) Feldeffekttransistoren auf einem Siliziumchip
- Halbleiterprozess zur kostengünstigen Herstellung von integrierten digitalen, analogen und Mixed-Signal Schaltungen
- Herstellung im Waferprozess



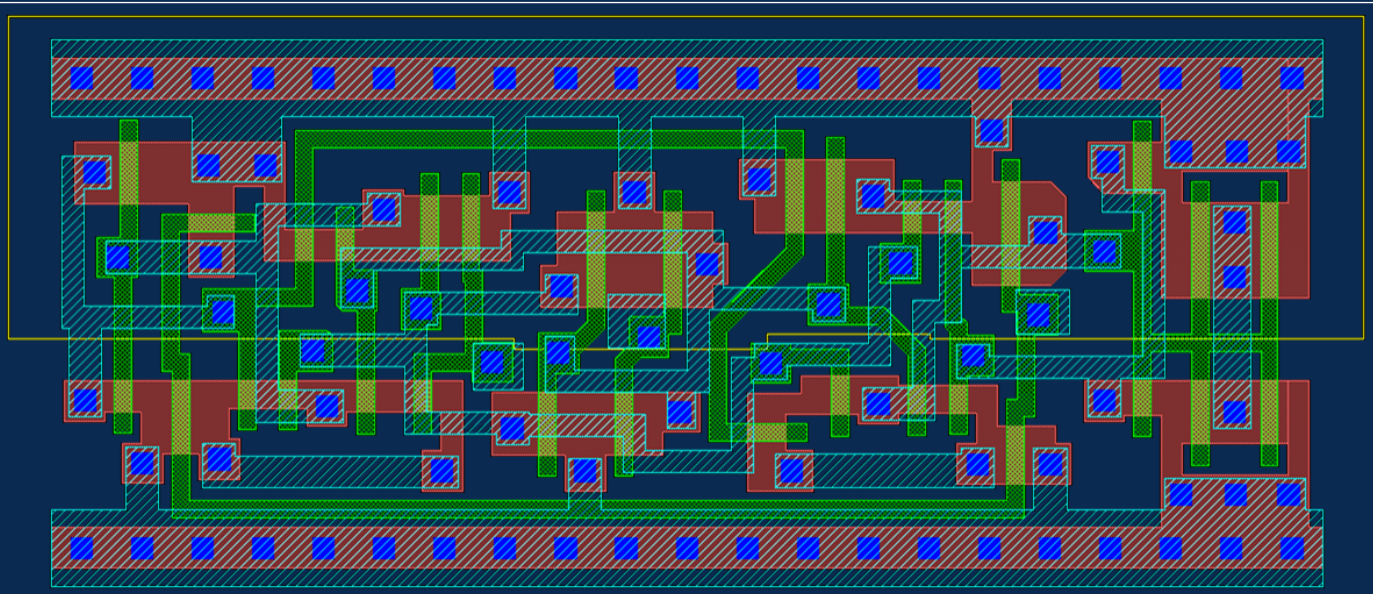
Quelle: Intel

CMOS Technologieskalierung

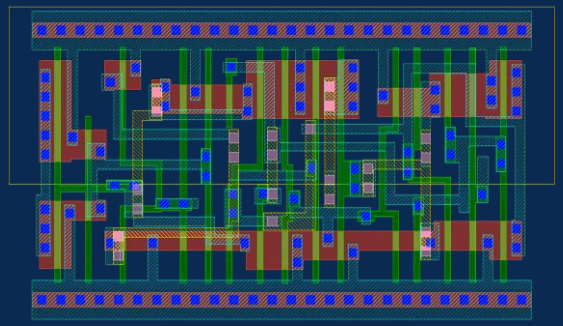


Quelle: International Technology Roadmap for Semiconductors

Standard Cell Scaling



180nm

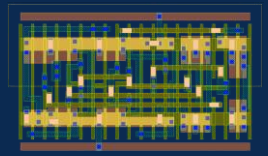


65nm

D-Flip-Flop

Drawn to Scale

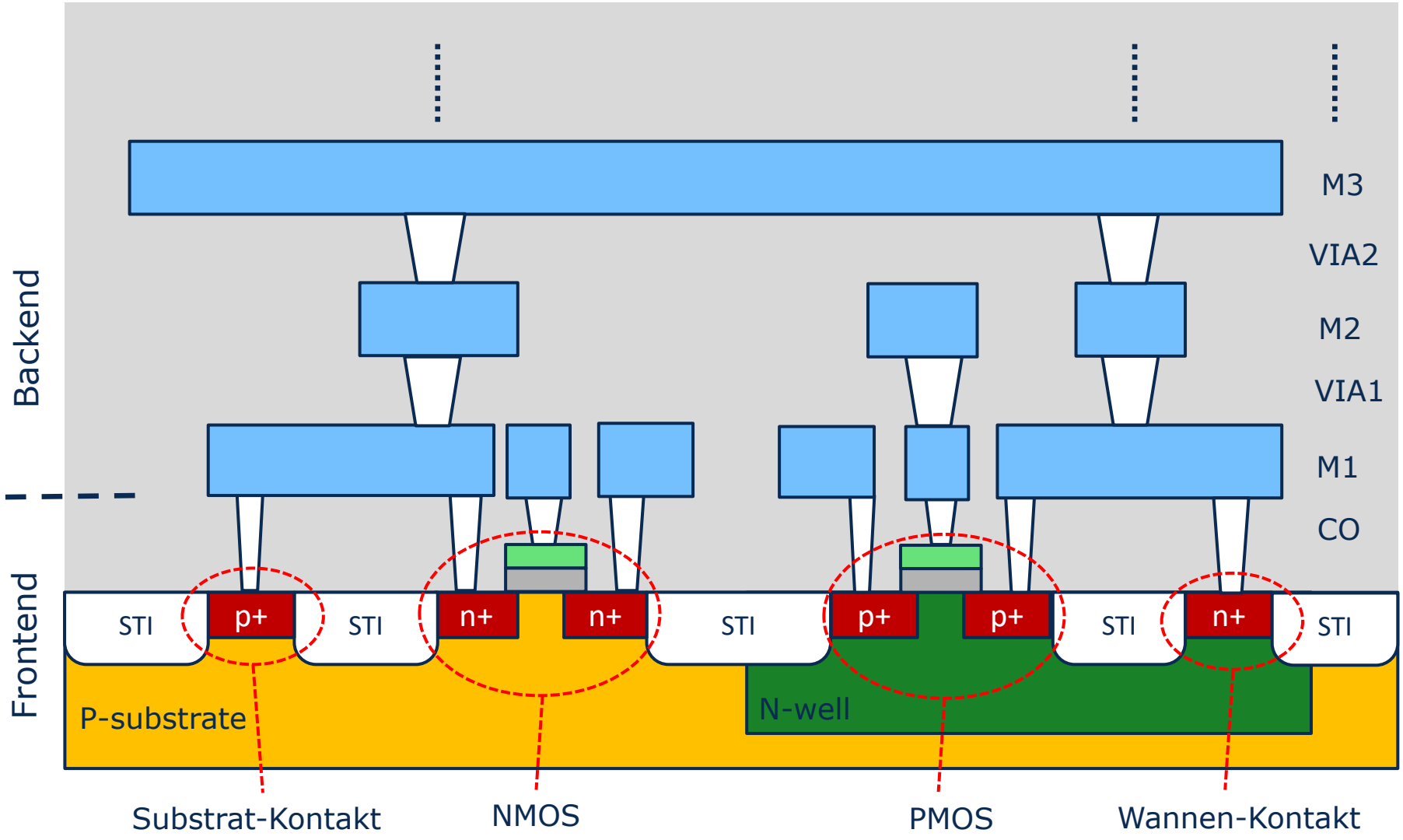
1000 nm

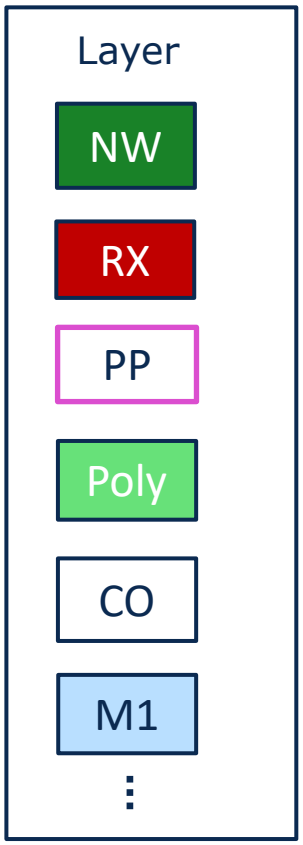


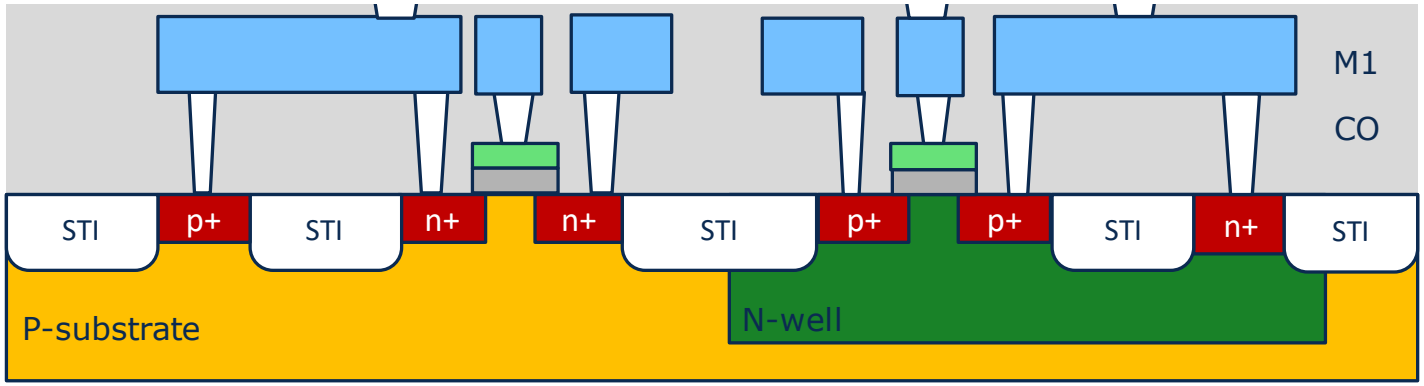
28nm

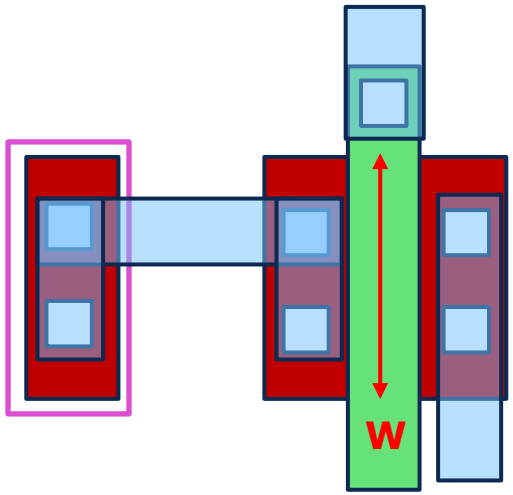
No End of the Road yet

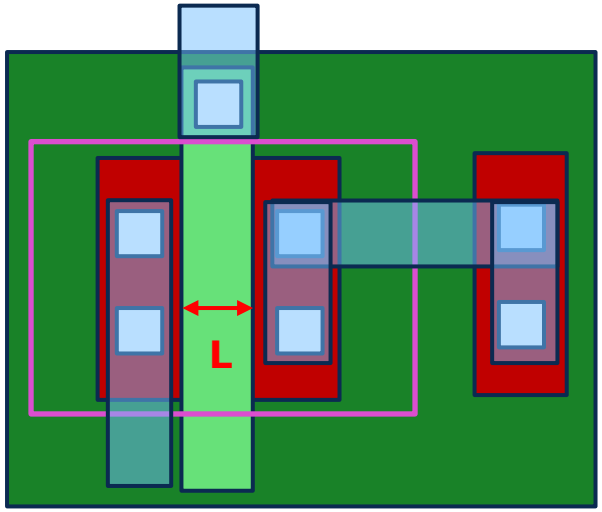
CMOS Querschnitt (Bulk Prozess)







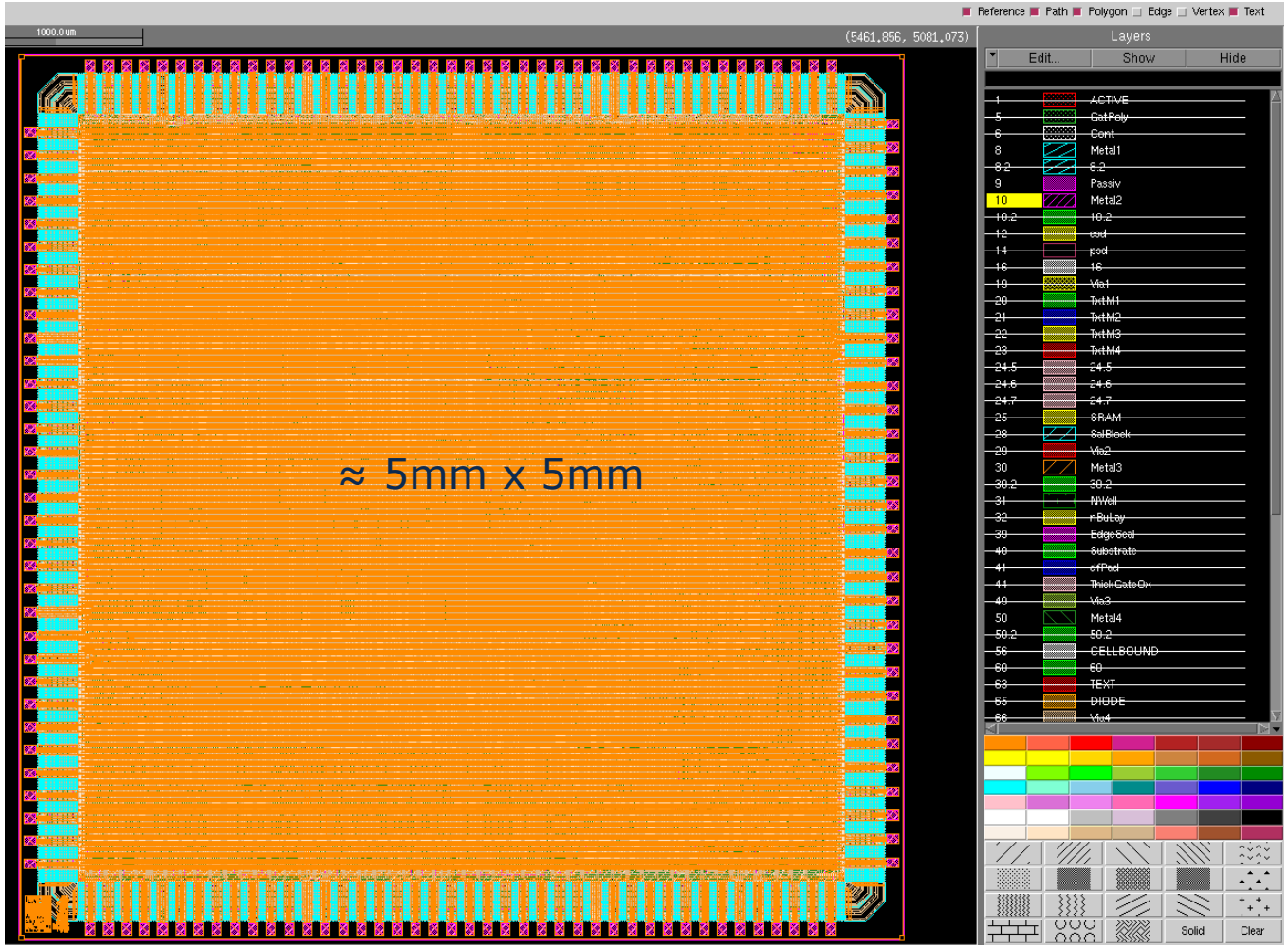




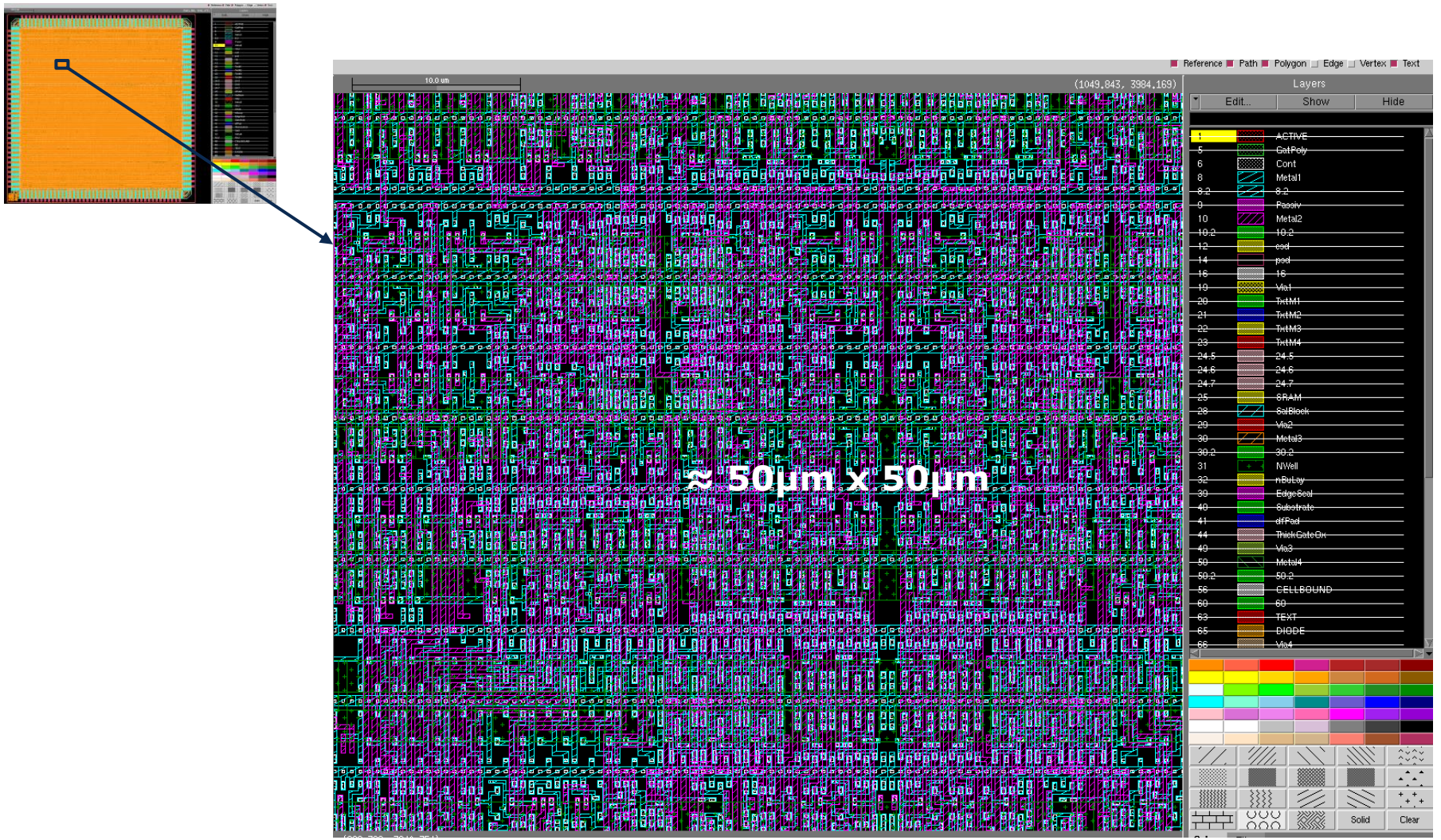
- Freiheitsgrade des Designers beim Schaltungsentwurf/Layoutentwurf:
  - Positionierung und Verdrahtung von NMOS und PMOS Transistoren
  - Transistor Parameter: **W**, **L**

CMOS Layout Beispiel

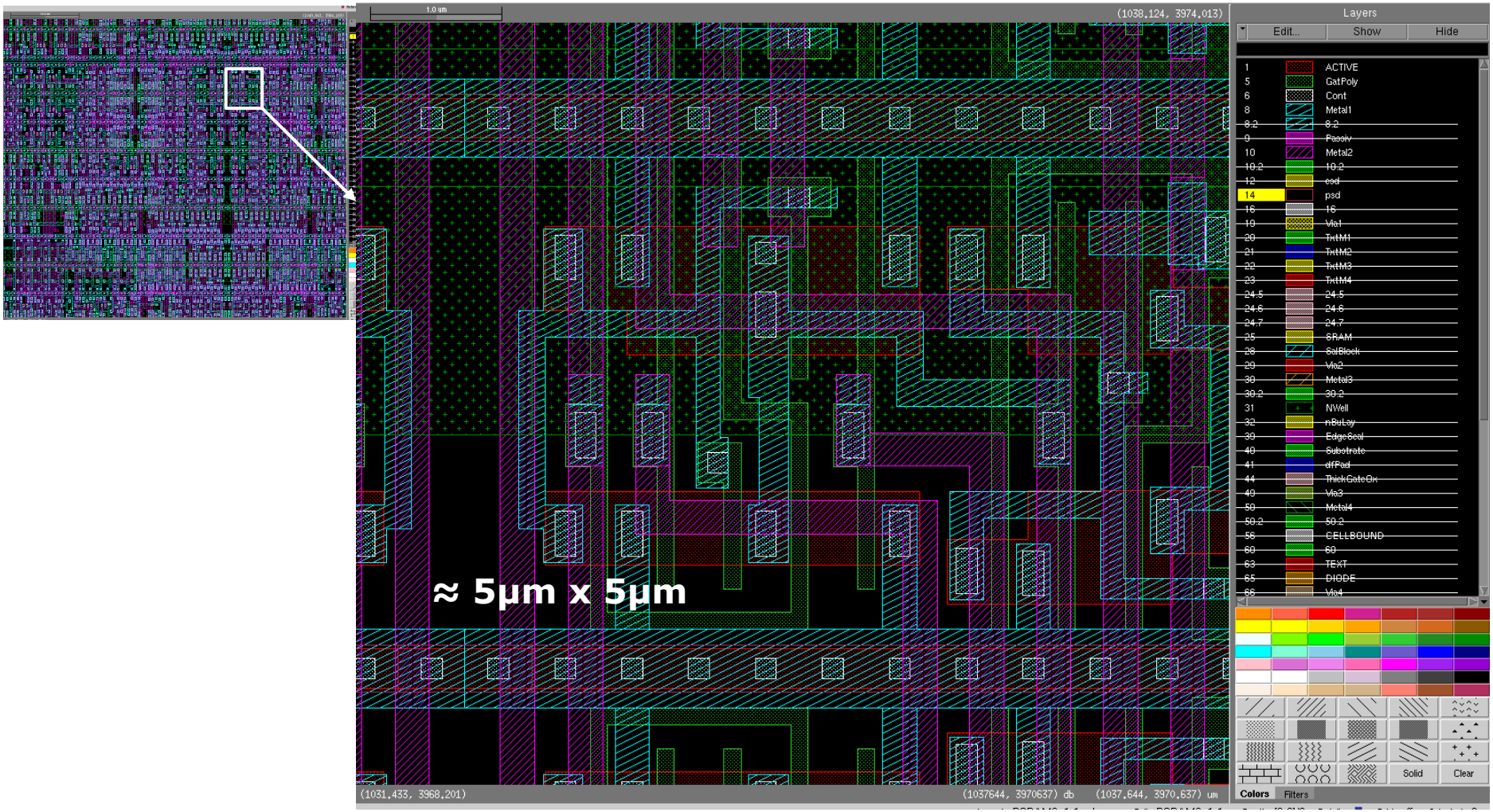
- Layout zur Herstellung der Masken zur Chip Fertigung



CMOS Layout Beispiel

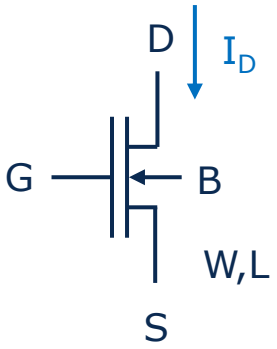


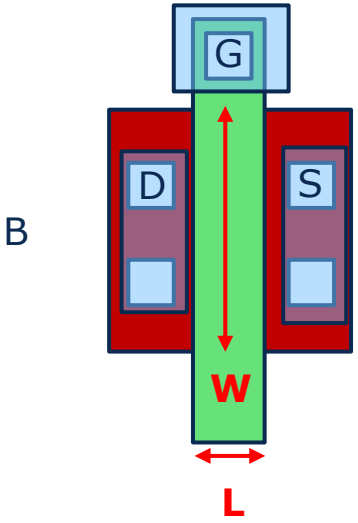
CMOS Layout Beispiel



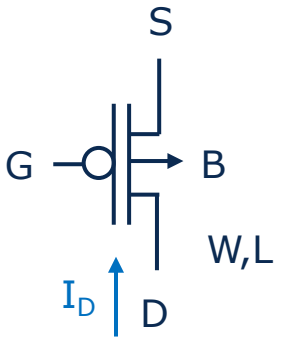
NMOS und PMOS Transistoren

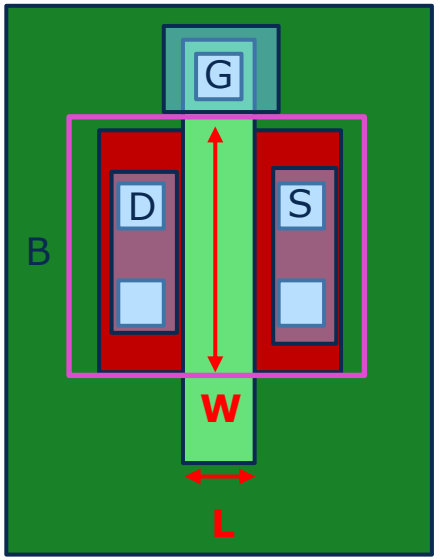
- NMOS Transistor:





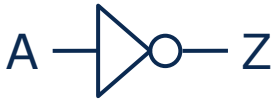
- PMOS Transistor:

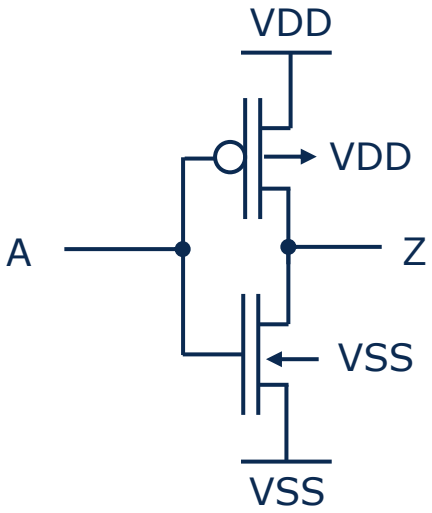


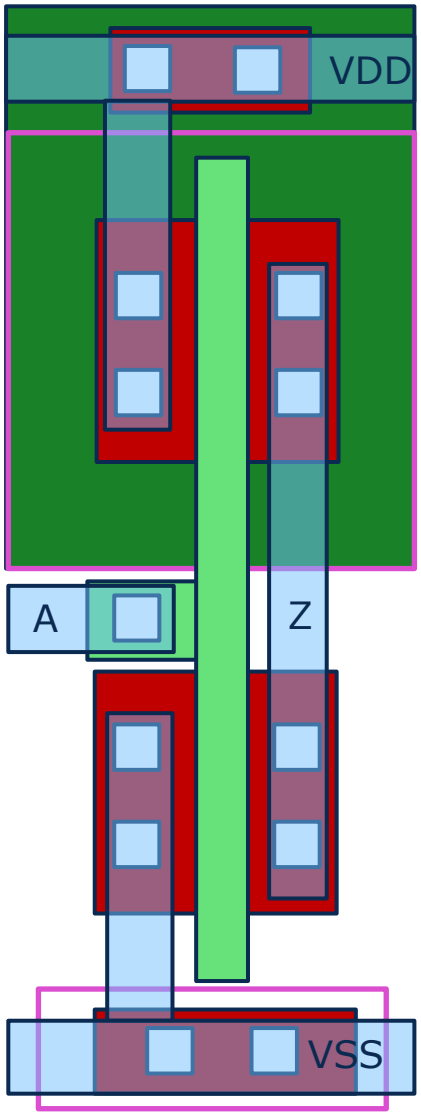


CMOS Inverter

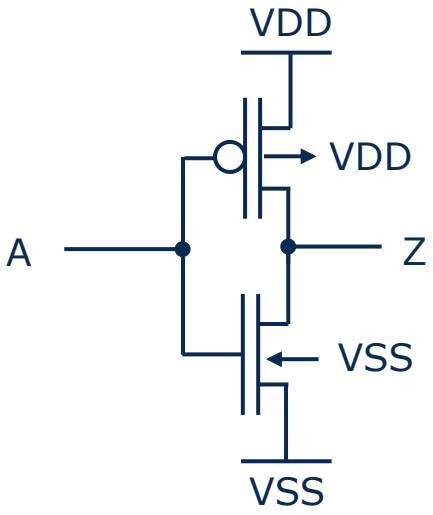
- Grundelement der CMOS Logik

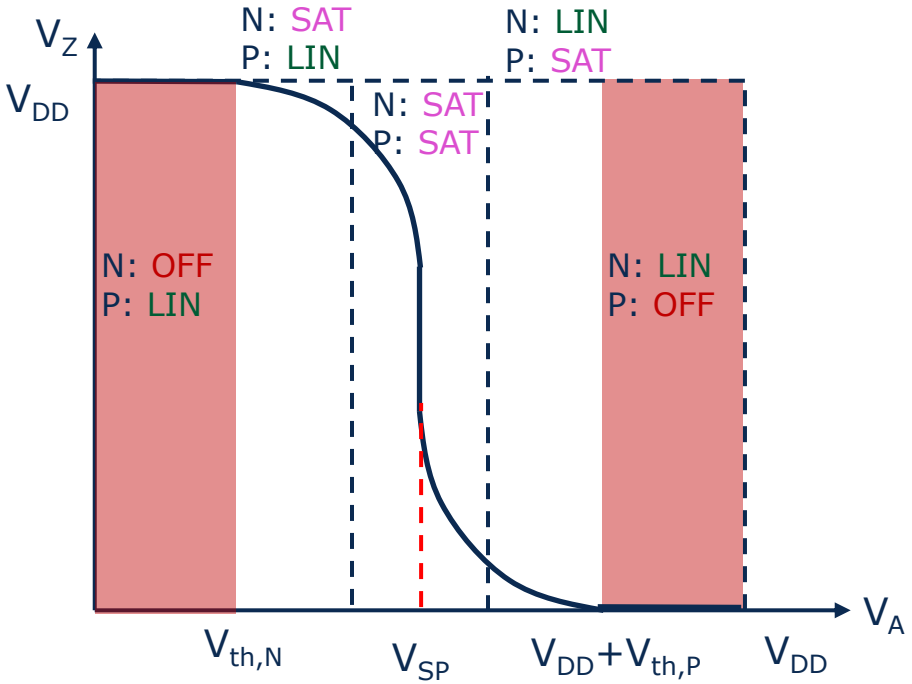






Statische CMOS Inverter Kennlinie

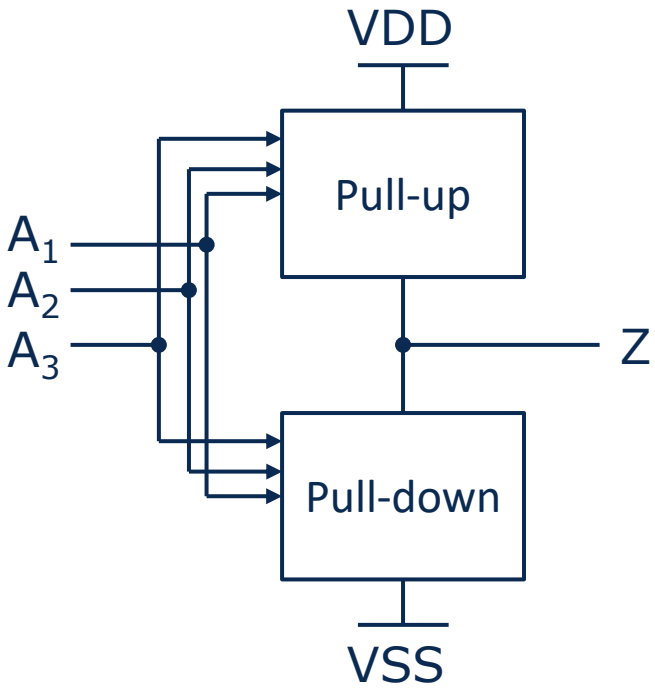




- Berechnung der Schaltschwelle (SP):
- N: SAT, PMOS: SAT (Annahme: λ=0)
  - $I_{D,N} = -I_{D,P}$
  - $\frac{\beta_N}{2}\left(V_{SP} - V_{th,N}\right)^2 = -\frac{\beta_P}{2}\left(V_{SP} - V_{DD} - V_{th,P}\right)^2$
  - $\rightarrow V_{SP} = \frac{(V_{DD}+V_{th,P}) - \sqrt{\frac{\beta_N}{-\beta_P}} \cdot V_{th,N}}{1 - \sqrt{\frac{\beta_N}{-\beta_P}}}$
  - $\rightarrow \frac{-\beta_P}{\beta_N} = \left(\frac{V_{SP} - V_{th,N}}{V_{SP} - V_{DD} - V_{th,P}}\right)^2$

CMOS Logik

- Pull-Up Netzwerke (PMOS):
  - $Z = \boldsymbol{F}(\overline{A_1}, \overline{A_2}, \overline{A_3}, \dots)$
- Pull-Down Netzwerke (NMOS):
  - $\bar{Z} = \boldsymbol{G}(A_1, A_2, A_3, \dots)$
- **UND** Verknüpfung durch Reihenschaltung von Transistoren
- **ODER** Verknüpfung durch Parallelschaltung von Transistoren

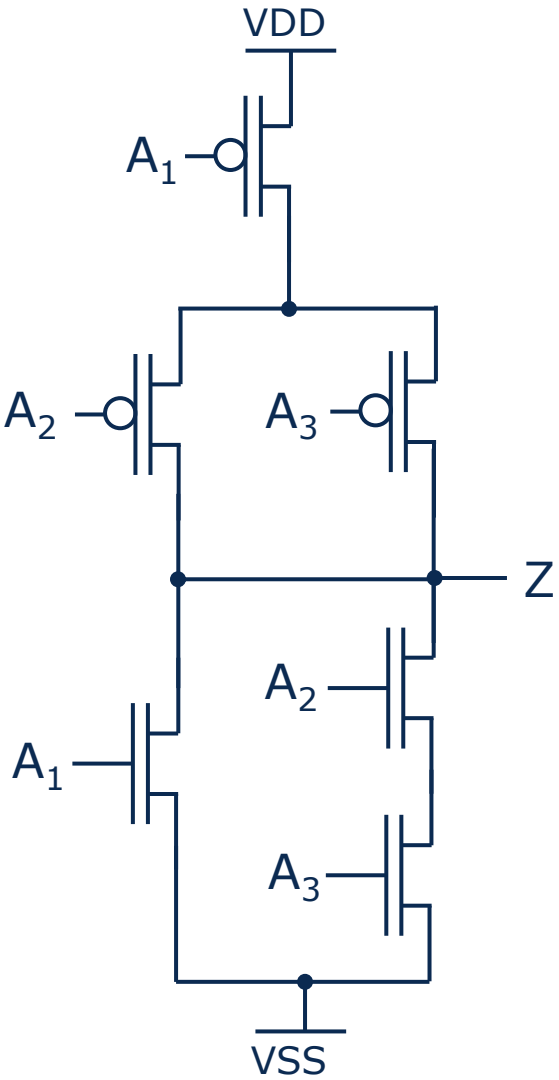


CMOS Logik Beispiel 1

- Logikfunktion: $\bar{Z} = A_1 + A_2 A_3$

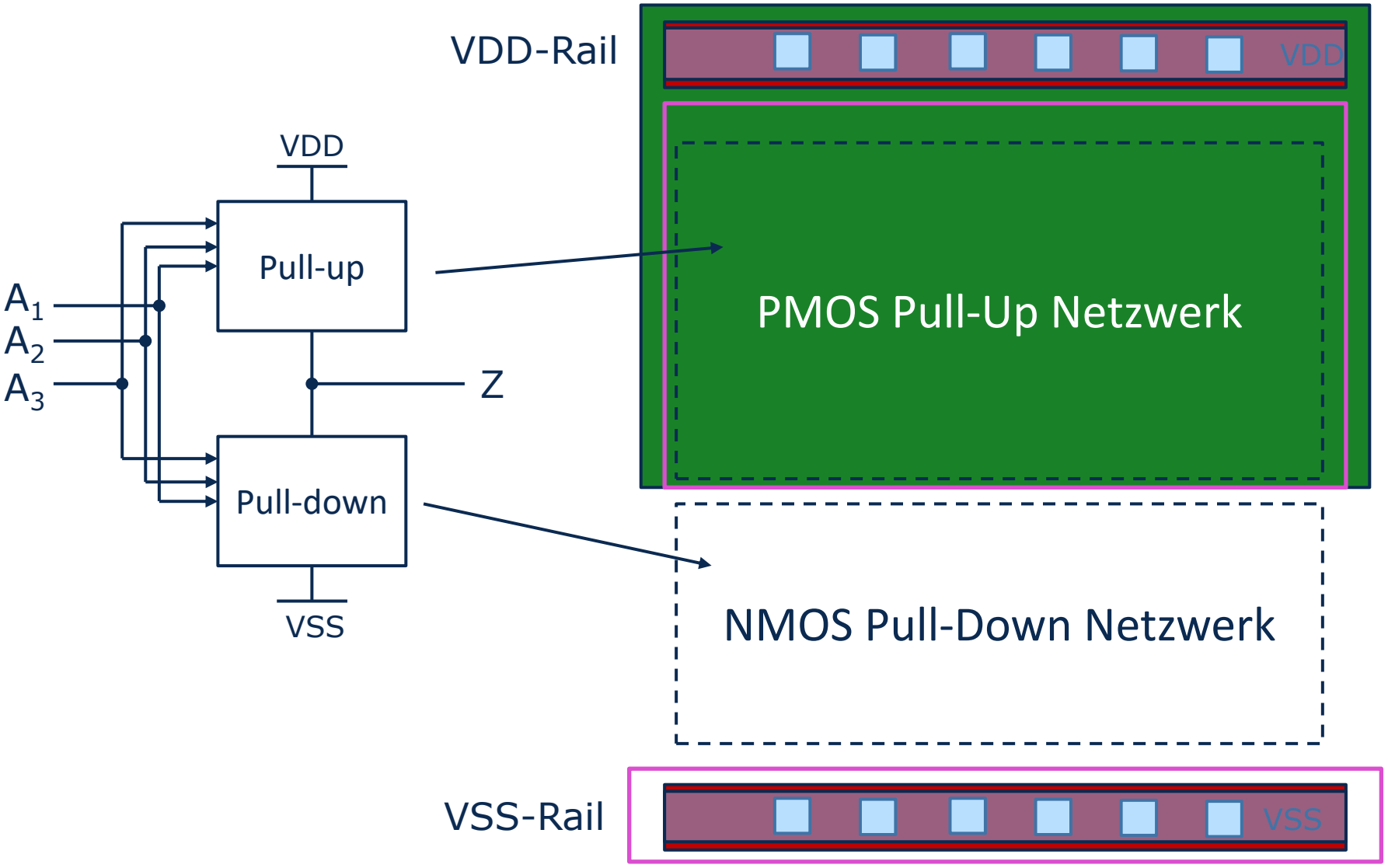
- Pull-Up Netzwerk:
  - $Z = \overline{A_1 + A_2 A_3} = \overline{A_1} \cdot (\overline{A_2} + \overline{A_3})$

- Pull-Down Netzwerk:
  - $\bar{Z} = A_1 + A_2 A_3$

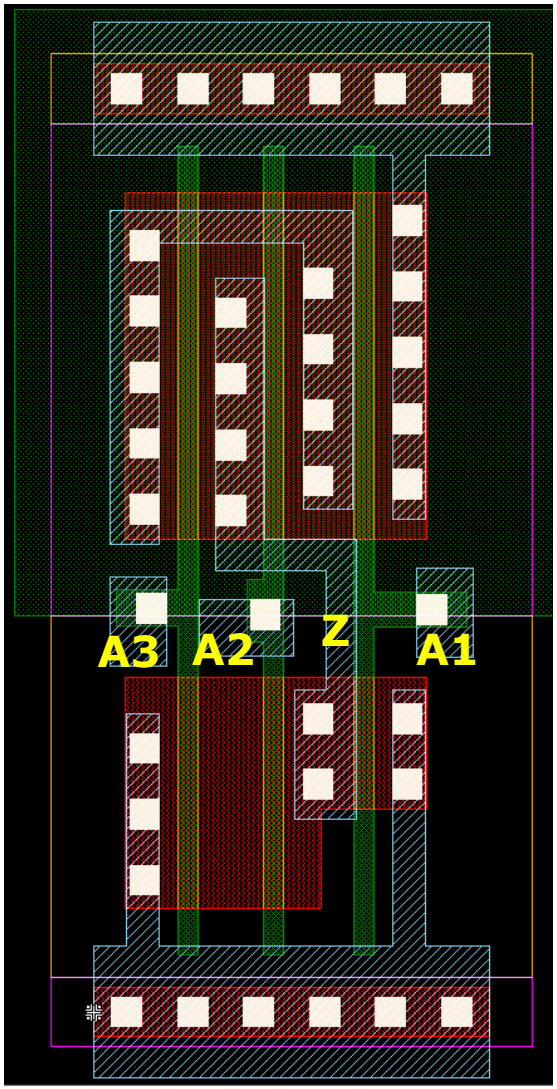


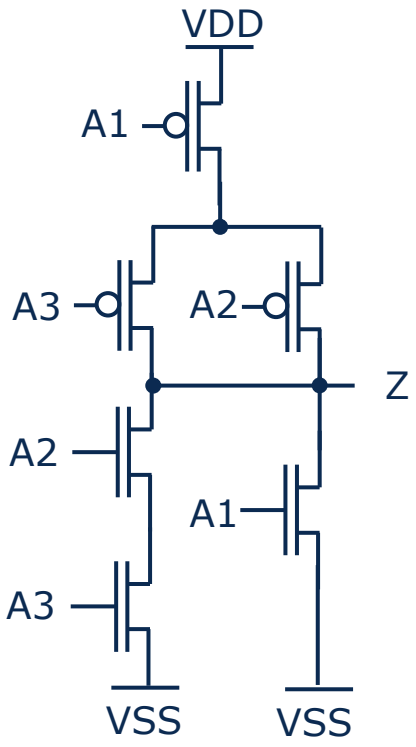
→ AOI12 Gatter

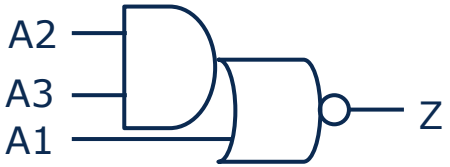
CMOS Logik Layout Realisierung



CMOS Gatter Beispiele 4



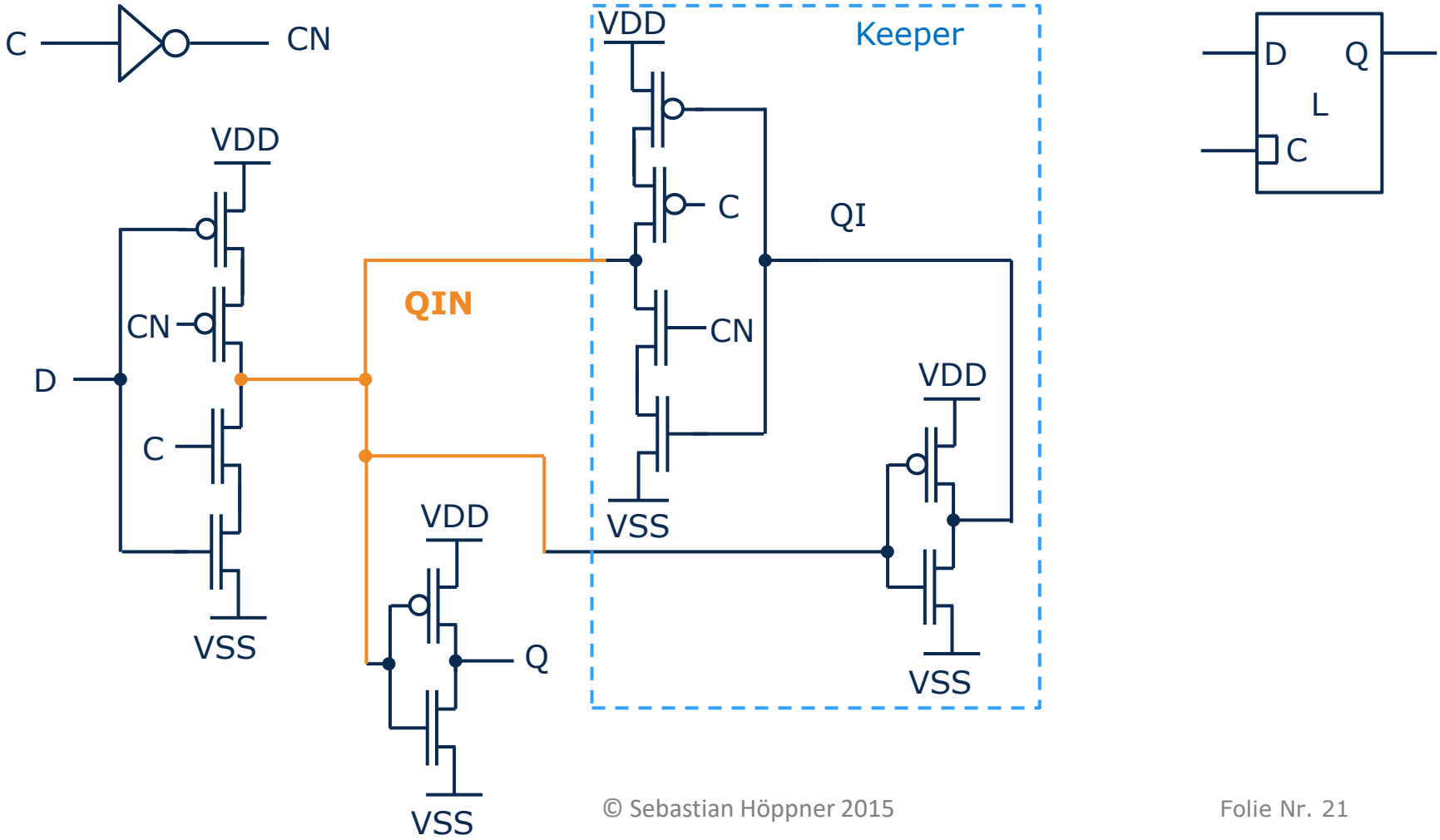




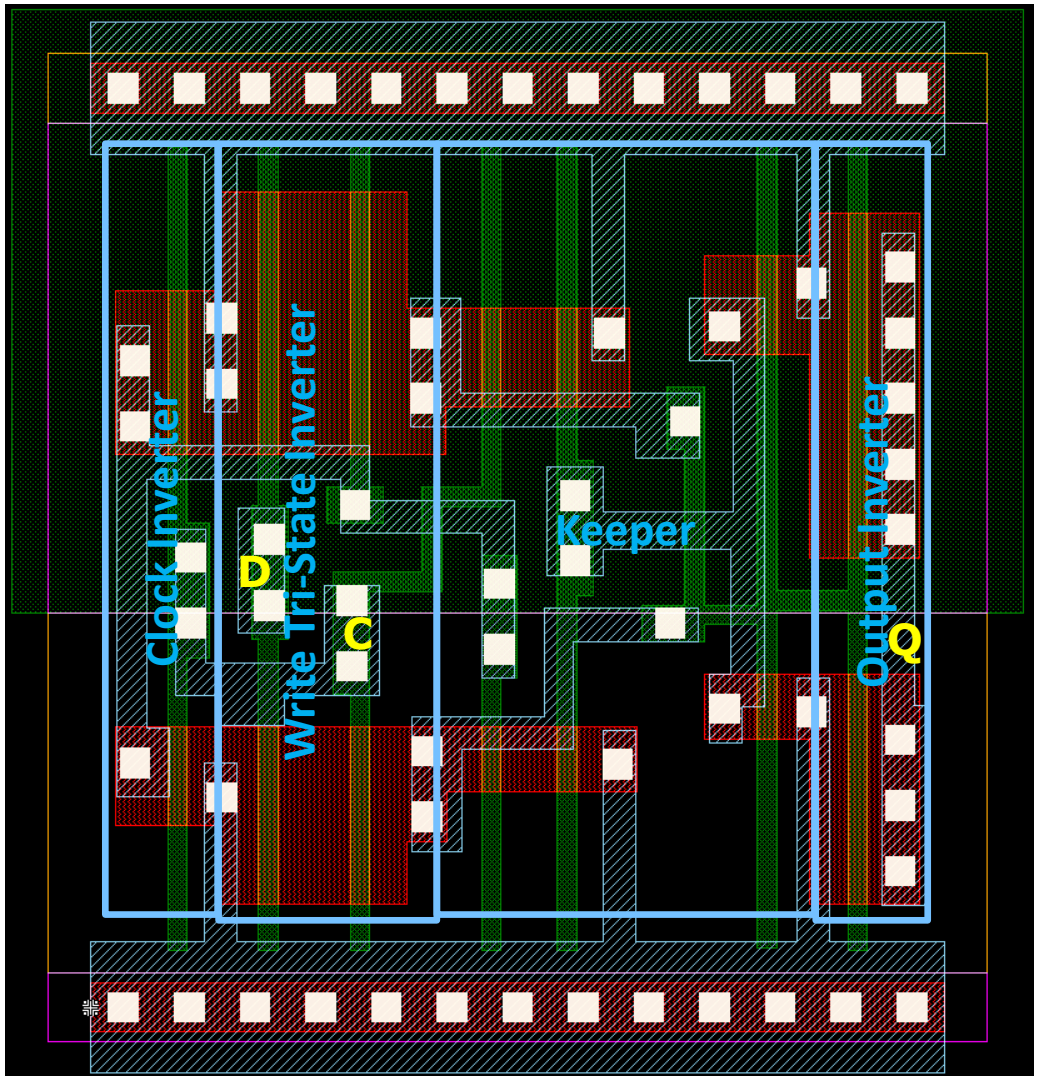
AOI2

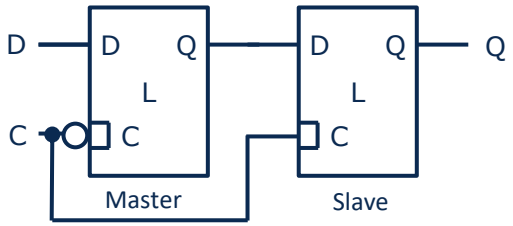
D-Latch

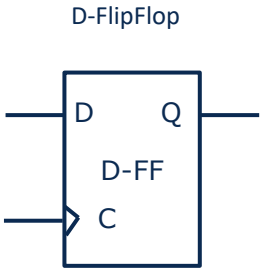
- Realisierung von des Schreibvorgangs auf einen **Speicherknoten** durch **Tri-State Treiber**
- Rückkopplung durch statische CMOS Logik → Keeper
  - Statischer Speicher → Kompensation von Leckströmen

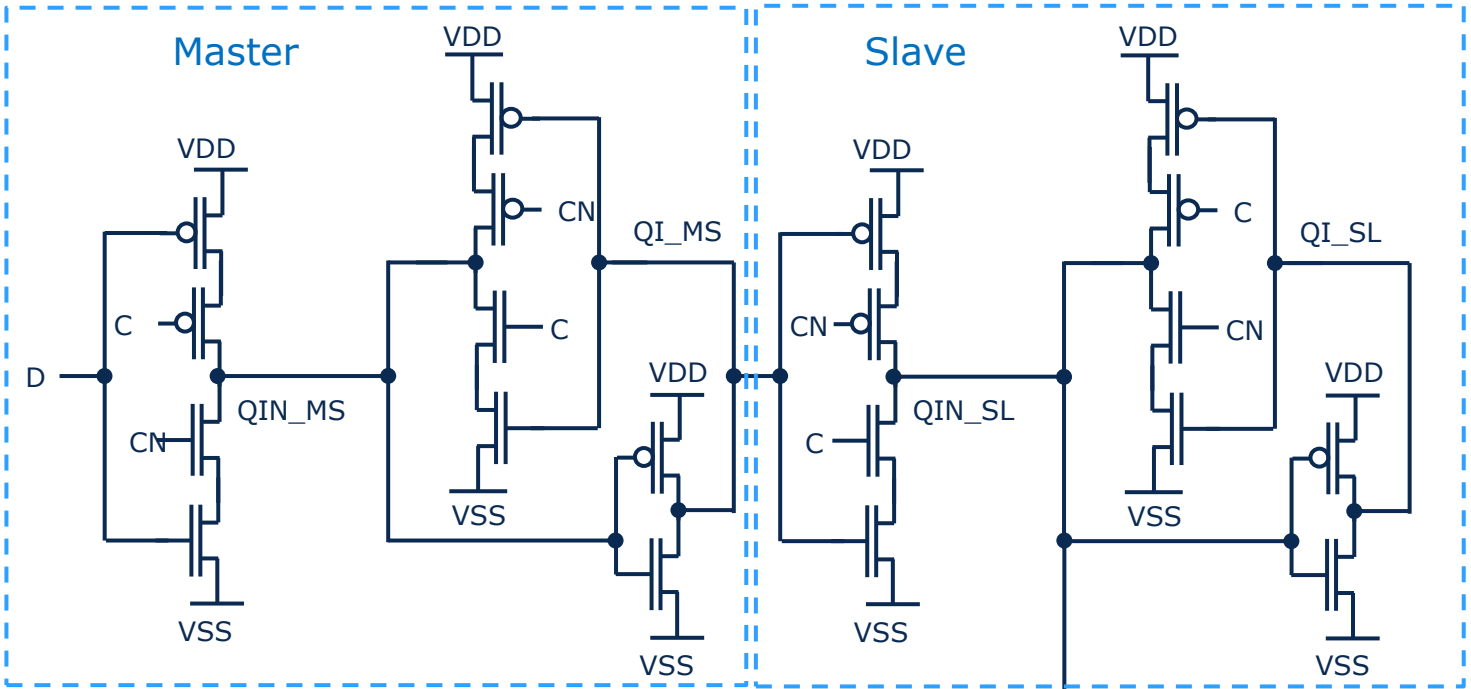


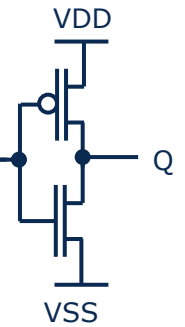
D-Latch Layout











D-FlipFlop Layout