MOCAST

THE 14TH INTERNATIONAL CONFERENCE ON MODERN CIRCUITS AND SYSTEMS TECHNOLOGIES

PROGRAM BOOKLET

11.06-13.06.25

DRESDEN, GERMANY

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We would be happy if you could share your photos or videos of the conference with everybody.

Please upload them here:

https://t1p.de/MOCAST2025-Uploads

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CONFERENCE AT A GLANCE

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09:00	Keynote 1: Themis Prodromakis
10:00	Coffee Break
10:30	Regular Session 1 Regular Session 2
12:36	Lunch
13:30	Keynote 2: Hai (Helen) Li
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14:45	Poster Session
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GENERAL CHAIRS' MESSAGES

Prof. Dr. Ronald Tetzlaff

General Co-Chair

Welcome to Dresden!

As we gather in the vibrant city of Dresden, the heart of Europe's microelectronics innovation, it is my great pleasure to extend a warm welcome on behalf of the Organizing Committee to all participants of the 14th International Conference on Modern Circuits and Systems Technologies (MOCAST). This conference has been a flagship of modeling, design, simulation, synthesis and implementation of circuits and systems since its inception in 2012, consistently exploring new directions in the field.

This MOCAST version is sponsored by the Institute of Electrical and Electronics Engineers (IEEE), the German Research Foundation (DFG), the School of Embedded Composite Artificial Intelligence (SECAI), Global Foundries (Platinum Sponsor), infineon (Gold Sponsor), ESMC (Silver Sponsor), and by TUD Dresden University of Technology. This year's MOCAST will be a rich ground for breakthrough ideas and pioneering research. The conference brings together cutting-edge research across a diverse range of topics, including Analog/RF and Mixed Signal Circuits, Sensors and Systems, and Emerging Memory Devices tailored for In-Memory AI applications. It highlights the latest advances in Device and Circuit Modeling, Trends in Modern Computer Arithmetic, and Digital Number Formats, fostering innovation in both theory and practical design. Special focus is also placed on breakthroughs in Memristive Neuromorphic Devices, Artificial Intelligence, Machine Learning, Nonlinear Circuits, Digital Systems, and Advanced Wireless Technologies, making it a premier forum for interdisciplinary collaboration and technological progress.

In addition, I am more than proud to welcome a number of outstanding invited speakers who are coming to Dresden to share their knowledge with the MOCAST audience.

All these talks and discussions are set against the backdrop of Dresden – rightfully dubbed as the Microelectronics Center of Europe – a city where history, culture, and technological innovation converge in a spectacular fashion. Dresden is proud of its dense concentration of semiconductor industries and synergistic academia-industry collaborations in microelectronics, supported by strategic geographical advantages and robust governmental support. This vibrant ecosystem not only reflects the city's rich technological heritage but also positions it at the forefront of global innovation and research in the microelectronics sector.

I would like to extend my heartfelt gratitude to all the members of the organizing and scientific boards, our funding organizations, our dedicated volunteers, and the vibrant community of researchers, without whom this conference would not have been possible. Your commitment, expertise, and passion are the pillars that uphold the spirit and success of MOCAST.
As we embark on this exciting journey over the next three days, I encourage you to engage, collaborate, and be inspired. Dresden offers a unique blend of historical richness and modern innovation – the perfect setting for fostering creative ideas and lasting connections.
Here's to a conference filled with enlightening discussions, groundbreaking insights, and, most importantly, joy and fun in the realm of circuits nad systems!
Welcome to IEEE MOCAST 2025 – where the future of circuits and systems is not just discussed but shaped.

Warm regards,
Ronald Tetzlaff

GENERAL CHAIRS' MESSAGES

Prof. Dr. Spiros Nikolaidis

General Co-Chair

Welcome to MOCAST!

It is a great honor and pleasure to welcome you to the 14th International Conference on Modern Circuits and Systems Technologies (MOCAST 2025), held this year in the beautiful and historic city of Dresden, Germany. MOCAST has consistently served as a dynamic and evolving platform that brings together leading researchers, academics, and industry professionals from around the world. The conference continues to foster the exchange of ideas, the presentation of cutting-edge research, and the exploration of innovative solutions across all aspects of circuits and systems. This year's edition promises to be no exception, offering a stimulating environment for collaboration and intellectual engagement.

The technical program of MOCAST 2025 reflects the wide breadth and depth of our field, spanning topics such as Analog/RF and Mixed-signal Circuits, Digital Circuits and Systems Design, Device and Circuit Modeling, High-performance Embedded Systems, Communication and Network Systems, Antenna Design, Power Management, Sensor Technologies, Nonlinear Systems, Emerging Technologies and Devices, Artificial Intelligence, Machine Learning and their Applications.

This year's conference also features several Special Sessions that highlight emerging directions in the field. Furthermore, we are proud to host high-level keynote speakers — internationally recognized experts in related topics —

who will share their insights and visions on the present and future of our discipline.

I would also like to extend my sincere gratitude to the members of the Program Committee for their invaluable contribution in reviewing the submitted papers. As every year, their support has been instrumental in ensuring the scientific quality and integrity of the conference. Quite simply, without their dedication, there would be no conference.

In addition to the rich technical content, MOCAST 2025 features a thoughtfully organized program designed to encourage networking, foster collaboration, and enhance the overall conference experience. I would like to thank the entire organizing committee for providing such a functional and well-balanced schedule — a key element that ensures the success of this year's edition. Whether you are joining us for the first time or are a long-standing member of the MOCAST community, I am confident that MOCAST 2025 will be both professionally enriching and personally memorable. We are proud to continue the tradition of excellence and innovation that defines MOCAST, and we look forward to sharing with you a new success story.

Warm regards,
Spiros Nikolaidis

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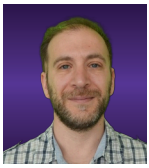

Dimitris Prousalis
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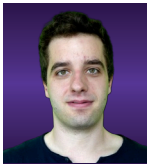

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Social Media Hashtag

#MOCAST2025

The Frauenkirche is a Lutheran church. It was founded in 1726 considered an outstanding example of Protestant sacred architecture, it featured one of the largest domes in Europe. After the destruction of the church in 1945, the remaining ruins were left for nearly half a century as a war memorial. The church was reconstructed between 1994 and 2005.

GENERAL INFORMATION

CONFERENCE VENUE

MOCAST 2025 will be held in the most modern lecture hall of TU Dresden, FOE/244, in the freshly renovated **Fritz-Förster-Bau**. Formerly used for the Faculty of Chemistry the building was build from 1921 until 1924 by the renowned architect Martin Dülfer, known for his contributions to architecture in the late 19th and early 20th centuries. Dülfer was a pioneer of the Jugendstil movement in Germany, which is the German equivalent of Art Nouveau, and his architectural style is noted for its innovative and decorative elements.

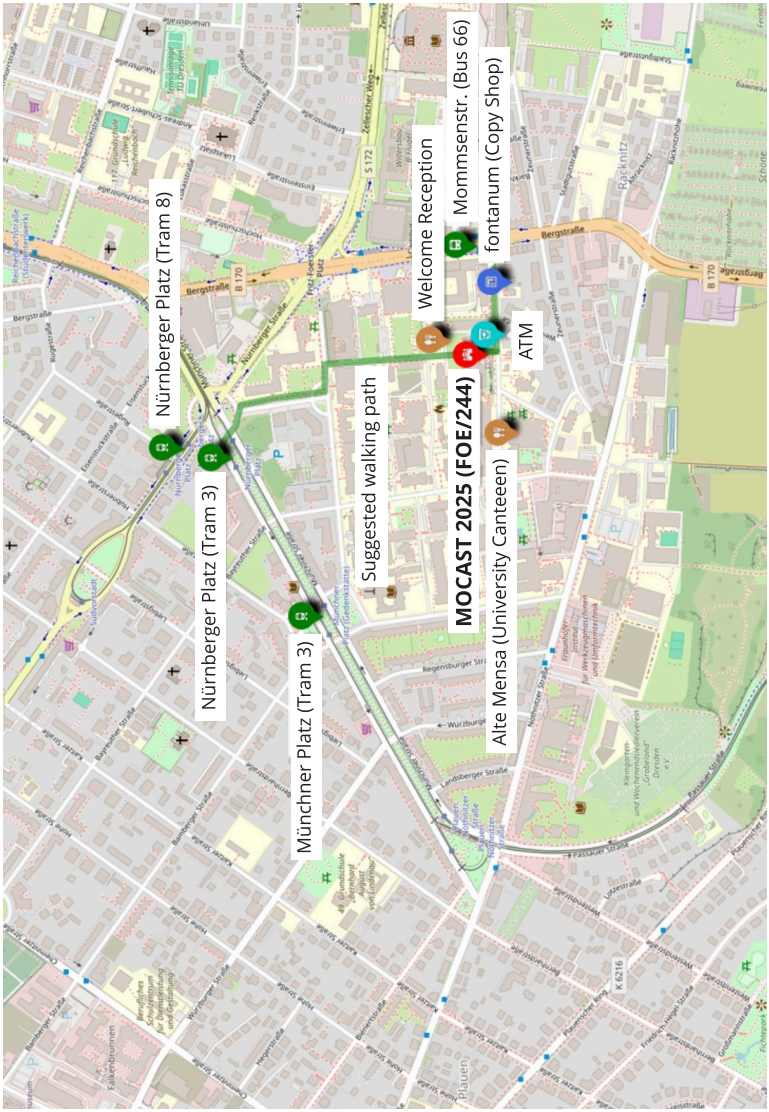
The name of the building is related to Fritz Förster (1866-1931), a former rector of TUD who was an electrochemist. The rectorate as well as the Alte Mensa (old university canteen) of TU Dresden are located close-by at Mommsenstreet that connects the venue also with the faculty of electrical and computer engineering.

Address

Fritz-Förster-Bau
Mommsenstraße 6
01069 Dresden

- Distance to main main station (by foot): 1.6 km
- Distance to Dresden airport (by car): 14 km
- Distance to the "Frauenkirche" (by foot): 3.4 km
- Distance to the "Zwinger/Alte Meister" (by foot): 3.4 km

CONFERENCE MAP



GENERAL INFORMATION

CONFERENCE REGISTRATION DESK

The Conference Registration Desk is located inside Fritz-Förster-Bau in front of the auditorium FOE/244:

Wednesday, June 11:	08:30 - 17:30
Thursday, June 12:	08:30 - 17:00
Friday, June 13:	08:30 - 17:00

ON-SITE REGISTRATION

On-site registration for the conference will be conducted during the registration desk hours by the registration chair.

DRESDEN

Dresden's beauty is inseparable from the natural beauty of the Elbe valley. City and landscape have developed harmoniously over centuries. Its architectural character has been shaped by masterpieces from numerous eras. The best-known historical attractions of the old city include the Zwinger, the Cathedral, the Semper Opera House, the Royal Palace, and the Frauenkirche, which was reconstructed with donations from all over the world. The Neustadt district is furthermore the largest wholly preserved late-19th-century city quarter in Germany.

Actually, Dresden has over 563.000 inhabitants and is one of the biggest cities of Saxony. We hope that you will enjoy your stay here in our beautiful city of Dresden.

For further information about Dresden please follow the link below:
https://www.dresden.de/index_en.php

CURRENCY EXCHANGE AND CREDIT CARDS

Only Euros (€) are accepted in stores and restaurants. Most German services accept major credit cards. However, smaller shops tend to prefer cash. You can obtain Euros (€) at automated teller machines (ATMs), at foreign exchange banks and other authorized money exchanges. Banks are closed on Saturdays and Sundays.

ELECTRICITY, INTERNET / WIFI & HYBRID ATTENDANCE

The electricity supply in Germany is 230 V, 50 Hz. Since MOCAST 2025 will be held within the facilities of TU Dresden, we expect most of the participants to have a strong WiFi connection via **eduroam**. If you do not have such access, please let us know so we can prepare special *guest credentials* for you.

Registered participants can access the MOCAST 2025 video conference online via the following link:
https://t1p.de/MOCAST2025-Conference

INSURANCE

The conference organizers cannot accept liability for personal injuries sustained, for loss of or damage to property belonging to conference participants (or their accompanying persons), either during or as a result of the conference. Please check the validity of your own insurance.

OFFICIAL LANGUAGE

English will be used for all presentations and printed materials. No interpretation service will be provided.

TIME DIFFERENCE

The time in Germany during summer is Central European Summer Time (CEST = UTC+2). In Germany, the 24-hour clock is used instead of AM or PM. Days run from 00:00 (midnight) to 23:59, so for example, 14:00 means 2:00 PM. This helps avoid confusion.

LUNCHES, DINNER AND COFFEE BREAKS

Lunches, Coffee breaks, Welcome Reception and Gala Dinner are included in the registration fee.

HELPFUL PHONE NUMBERS

Police	110
Emergency rescue / fire fighters	112
Taxi	+49 351 211 211

CONFERENCE BAG

GIFT BAG

The bag was specially designed for the conference. The skyline of Dresden is placed in between lines that can be interpreted as circuit wires and the MOCAST logo. In addition, logos of the main organizing and supporting institutions as well as sponsors are shown. The bag contains the USB flash drive with conference information as well as Dresden typical gifts and sweets.

LOCAL SWEETS

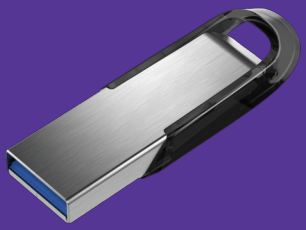
Dresden is renowned as the birthplace of milk chocolate, with its chocolate history dating back to 1839 when the local company Jordan & Timaeus crafted the very first milk chocolate using donkey milk. This innovation transformed chocolate from a bitter drink into a smooth, sweet treat and marked a turning point in confectionery history. Today, Dresden has a rich legacy in chocolate production from which we want to show just a a glimpse.

Among them is *Dinkelchen*, a key element in Dresden's chocolate heritage that blends traditional recipes with locally sourced organic ingredients. Another example are chocolate bars from the Dresden startup *nucao* — a symbol of both artisanal excellence and modern innovation —which continues to enrich Dresden's sweet legacy.

DRESDEN PANORAMA

The view from Carola Bridge offers a breathtaking panorama of Dresden's old city, where history and modern revival gracefully intertwine. From this vantage point, you can admire the elegant baroque facades, the delicate silhouettes of reconstructed landmarks like the Frauenkirche, and the gentle curves of the Elbe reflecting the city's storied past. Until you can enjoy this view again on your own we want to offer you this printed panorama on photo paper.

USB FLASH DRIVE



The 32GB USB flash drive, that you have found in your MOCAST gift bag, is special. On the one hand, it contains this program booklet and the conference proceedings, which is common. On the other hand, it contains a Live-USB operating system that we call "Uni flash drive" - another unique aspect of TUD Dresden University of Technology. The flash drive is based on Linux Debian and contains more than 150 free and open source software (FOSS) apps that are valueable for students and scientists.

Try it by booting from this flash drive! More information: https://fsfw-dresden.de/uni-stick

WELCOME RECEPTION EVENING

AGENDA

Wednesday, 11.06.2025

17:30	End of sessions in the building
18:00	Start of Welcome Reception in the inner courtyard of Fritz-Förster-Bau

LIVE BAND "SAMMELSURIUM"

Founded 15 years ago by Dresden students, the rock-pop cover band *Sammelsurium* delivers performances with a diverse repertoire spanning multiple genres and decades, usually for weddings or dancing partys. They cover timeless classics as well as global hits to enjoy the audience with handmade music in every played note.

http://band-sammelsurium.de

FLYING BUFFET

Gildamaestro is an innovative caterer renowned for setting new culinary standards with creative menu concepts and exceptional service. They blend traditional cuisine with modern influences to transform every event into a memorable gastronomic experience. Whether it's an intimate gathering or a large celebration, Gildamaestro crafts unique, unforgettable culinary moments.

GILDAMAESTRO

by Florian Gildemeister

https://gildamaestro.de/

BBQ

The grill sticks from *Sindbad*, a renowned Lebanese restaurant in Dresden, are a standout dish. Marinated in a blend of aromatic spices and herbs, they will be grilled to perfection, offering the perfect balance between juicy tenderness and a smoky char. This halal dish embodies the authentic flavors of Lebanese cuisine, making it a must-try for anyone seeking a genuine taste of the Middle East in Dresden.

https://sindbad-dresden.de/

SINDBAD
Libanesisches Restaurant

GALA DINNER EVENING

AGENDA

Thursday, 12.06.2025

19:00 Start Dinner at the restaurant Anna im Schloss

RESTAURANT "ANNA IM SCHLOSS"

The "*Anna im Schloss*" Restaurant is the perfect place to meet in the historic heart of Dresden, whether for lunch, coffee or dinner. It is located in the former court cellar of Dresden's Royal Palace "Residenzschloss". The Dresden Royal Palace is the former main residence of the Electors and Kings of Saxony in Dresden and now is a museum. The museum complex in the palace comprises the *Old* and *New Green Vaults*, the *Coin Cabinet*, the *Copper Engraving Cabinet* and the *Armoury with the Turkish Chamber*, all of which belong to the Dresden State Art Collections. The palace also houses the Art Library for specialised art history literature.

LIVE BAND "SUNSHINE BRASS"

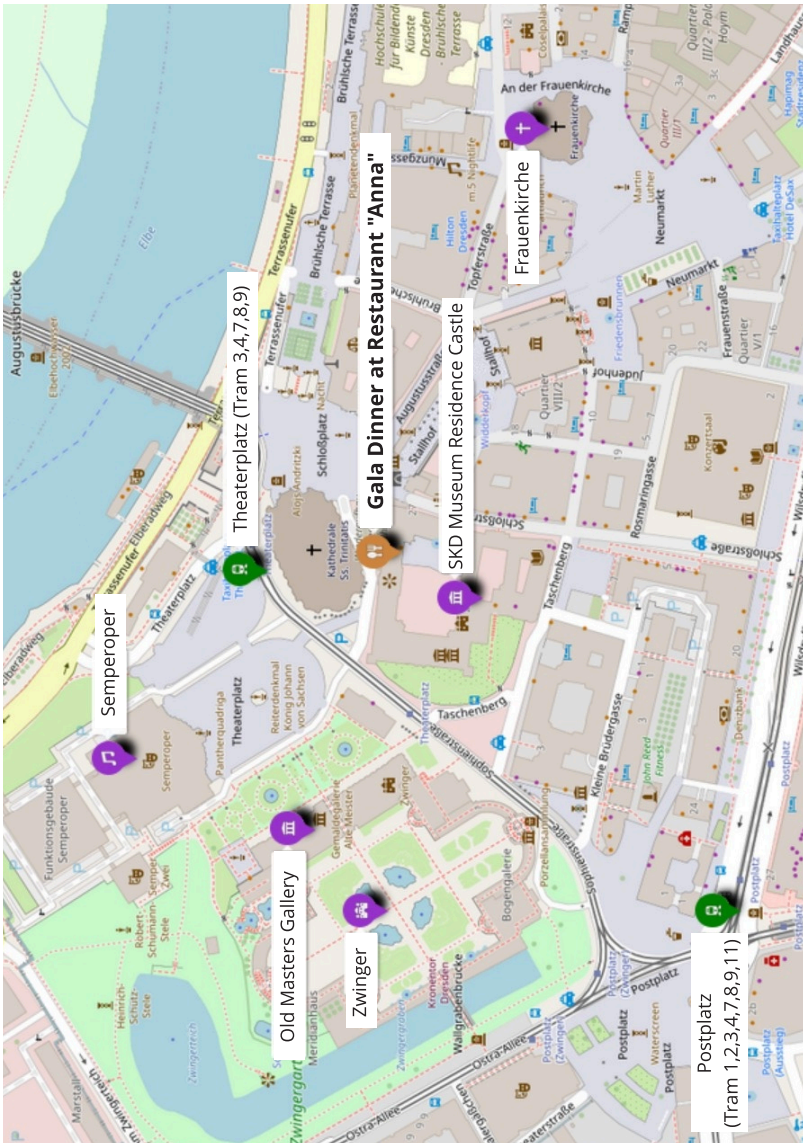
SUNSHINE BRASS has been touring the country as a humorous Dixieland band since 2001. They now enjoy cult status. Armed with trumpets, clarinets, saxophones, trombones, banjos, sousaphones, drums and a megaphone, the gentlemen of the orchestra present handmade music that is unrivalled in its originality and diversity. They entertain their audience in a charming way: cheeky, clever and warm-hearted at the same time, they invite listeners to clap, sing along, dance and celebrate. Whether on stage with technical equipment, in the middle of the audience on tables and benches, or discreetly in the background at elegant parties: the spontaneity of the six passionate musicians and their closeness to the audience inspire enthusiasm.

https://sunshinebrass.de/

◎ ◎ ◎ Adress of Gala Dinner:

Schlossstraße 27, 01067 Dresden

◎ ◎ ◎ MAP - TRAM STATIONS AND MEETING POINT



PLENARY SPEAKER

KEYNOTE 1

Time: Wednesday, 09:00 - 10:00

"Innovations across AI and Semiconductors"

Themis Prodromakis
Regius Chair of Engineering,
Centre for Electronics Frontiers, Institute for Micro Nano Systems, University of Edinburgh in Edinburgh (UK)

Chair: Ronald Tetzlaff

Abstract
The 21st century is defined by increasingly intelligent machines and a drive to use them for augmenting human capability. On one side, developments in Artificial Intelligence (AI) are more and more inspired by nature's efficiency. On the other hand, advances in medical interventions are increasingly driven by ever more intelligent electronics. Innovation in engineering underpins both on a fundamental level.
A novel nanoelectronic technology, known as the memristor, proclaims to hold the key to all, being both smaller and simpler in form than transistors, low-energy, and with the ability to retain data by 'remembering' the amount of charge that has passed through them – akin to the behaviour of synaptic connections in the human brain. In this talk Professor Prodromakis will present the attributes of memristive technologies that make this emerging technology attractive for a variety of applications – ranging from bio-inspired memories to compressing sensing and even embedding "AI on chip".

Short Bio
Professor Themis Prodromakis holds the Regius Chair of Engineering at the University of Edinburgh and is Director of the Centre for Electronics Frontiers. His work focuses on developing metal-oxide Resistive Random-Access Memory technologies and related applications and is leading an interdisciplinary team comprising 30 researchers with expertise ranging from materials process development to electron devices and circuits and systems for embedded applications. He holds a Royal Academy of Engineering Chair in

Emerging Technologies and a Royal Society Industry Fellowship. He is an Adjunct Professor at UTS Australia, visiting Professor at the Department of Microelectronics and Nanoelectronics at Tsinghua University, and Honorary Fellow at Imperial College London. He is Fellow of the Royal Society of Chemistry, the British Computer Society, the IET and the Institute of Physics and is also Senior Member of the IEEE. He served as the Director of the Lloyds Register Foundation International Consortium for Nanotechnology and Co-Director of the UKRI Centre for Doctoral Training in Machine Intelligence for Nano- Electronic Devices and Systems (MINDS). In 2015, he established ArC Instruments Ltd that delivers high-performance testing infrastructure for automating characterisation of novel nanodevices in over 21 countries and in 2019 he founded SoneT.ai that is building new power-efficient AI hardware solutions. His contributions in memristive technologies and applications have brought this emerging technology one step closer to the electronics industry for which he was recognised as

KEYNOTE 2

Time: Wednesday, 13:30 - 14:30

"Big AI for Small Devices"

Hai (Helen) Li
Professor
Department Chair of the Electrical and Computer Engineering Department, Duke University in Durham (US)

Chair: Spiros Nikoladis

Abstract

As artificial intelligence (AI) transforms industries, state-of-the-art models have exploded in size and capability. However, deploying these models on resource-constrained edge devices remains a significant challenge. Smartphones, wearables, and IoT sensors face stringent limitations on computing, memory, power, and communication, creating a big gap between demanding AI models and edge hardware capabilities that hinders the deployment of intelligence. In this talk, we will re-examine techniques to bridge this gap and embed big AI on small devices.

PLENARY SPEAKER

We will begin by discussing how the properties of various hardware platforms impact the design strategies of efficient deep neural network (DNN) models, such as quantization and pruning. Next, we will discuss techniques aimed at reducing the inference and training costs of distributed collaborative edge AI systems. Finally, we will delve into the underlying design philosophies and their evolution toward efficient, scalable, robust, and secure edge computing systems.

Short Bio

Hai (Helen) Li is the Marie Foote Reel E'46 Distinguished Professor and Department Chair of the Electrical and Computer Engineering Department at Duke University. She received her B.S. and M.S. degrees from Tsinghua University, and her Ph.D. degree from Purdue University. Her research interests include neuromorphic circuits and systems for brain-inspired computing, machine learning acceleration and trustworthy AI, conventional and emerging memory design and architecture, and software and hardware co-design. Dr. Li served/serves as the Associate Editor-in-Chief and Associate Editor for multiple IEEE and ACM journals. She was the General Chair or Technical Program Chair of multiple IEEE/ACM conferences and the Technical Program Committee member of over 30 international conference series.

Dr. Li has received many awards, including the IEEE Edward J. McCluskey Technical Achievement Award, Ten Year Retrospective Influential Paper Award from ICCAD, TUM-IAS Hans Fischer Fellowship from Germany, ELATE Fellowship, nine best paper awards, and another ten best paper nominations from IEEE/ACM. Dr. Li is a fellow of IEEE, ACM, and NAI.

PLENARY SPEAKER

KEYNOTE 3

Time: Thursday, 09:00 - 10:00

"ESMC – a light house project of the European chips act in Silicon Saxony"

Christian Koitzsch

President and managing director of the European Semiconductor Manufacturing Company (ESMC), Dresden

Chair: Ronald Tetzlaff

Abstract

ESMC, a joint venture between Bosch, Infineon, NXP and TSMC, is establishing an advanced logic foundry operation in Dresden, Germany. The facility will be a first-of-its-kind 12 nm FINFET open EU foundry. The talk will present the current status and future plans of the project. Special emphasis is given to sustainability and talent development.

Short Bio

Dr. Christian Koitzsch has been the president and managing director of the European Semiconductor Manufacturing Company (ESMC) since beginning of 2024. He was raised in Thueringia, is married and is father of two children. He studied Electrical Engineering at Technische Universität Ilmenau and North Carolina State University in Raleigh (US) and received a PhD in solid state physics from the University of Neuchâtel, Switzerland.

PLENARY SPEAKER

KEYNOTE 4

Time: Thursday, 13:30 - 14:30

"Diffusive and drift memristors for neuromorphic and analog computing"

J. Joshua Yang
Professor of Department of Electrical and Computer Engineering at the University of Southern California (USC) in Los Angeles (US).

Chair: Alon Ascoli

Abstract
Memristors can be broadly categorized into diffusive memristors and drift memristors, based on their reset switching mechanisms. Diffusive memristors reset via the diffusion of mobile species under zero electrical bias, exhibiting dynamics that closely mimic biological ion behavior. This unique characteristic enables efficient neuromorphic computing. In contrast, drift memristors reset through the drift of mobile ions under an electric field, offering highly stable analog resistance levels ideal for constructing neural networks for analog computing. This presentation will highlight recent advancements in memristor devices, arrays, and their application demonstrations, showcasing their potential in emerging computing paradigms.

Short Bio
J. Joshua Yang is the Arthur B. Freeman Chair Professor in the Department of Electrical and Computer Engineering at the University of Southern California (USC). His research focuses on post-CMOS hardware for neuromorphic computing, machine learning, and artificial intelligence, in which he has published several pioneering papers and holds over 120 granted U.S. patents. Dr. Yang is the Founding Chair of the IEEE Neuromorphic Computing Technical Committee, Director of the USC–Air Force Center of Excellence on Neuromorphic Computing, and Co-Founder of TetraMem Inc. He has received numerous honors, including the Powell Faculty Research Award, the UMass Distinguished Faculty Lecturer Award, and the UMass Chancellor's Medal—the highest honor bestowed by the University of Massachusetts. He serves as an Associate Editor for associate editor of Science Advances (AAAS), ED-M (IEEE), PNAS (NAS). Dr. Yang is a Clarivate™ Highly Cited Researcher and ranked among the Top Scientists by Research.com. He is a Fellow of IEEE and the NAI, recognized for his seminal contributions to resistive switching materials and devices for non-volatile memory and neuromorphic computing.

PLENARY SPEAKER

KEYNOTE 5

Time: Friday, 09:00 - 10:00

"AI chips. How about safety and security?"

Jaan Raik

Professor at the Department of Computer Systems, Head of the Center for Dependable Computing Systems, Tallinn University of Technology (TalTech) in Tallinn (EE)

Chair: Spiros Nikoladis

Abstract

The recent breakthrough of Artificial Intelligence (AI) has been partly enabled by the advances in chip technology and computer architectures as well as by the emergence of dedicated hardware accelerator chips. However, the probabilistic nature of the AI-based systems block their application in safety-critical applications. In this talk we will review the challenges to the safety and security of the AI chips and will show how these aspects can be accurately assessed in a fast and scalable manner and also enhanced. It will be shown that many effective robustness enhancement methods turn out to have low cost in terms of additional resources. Moreover, new, safety aware pruning methods will be presented that in fact result in reduced neural network model sizes with increased levels of robustness. The talk is based on recent advances in the research of safe and secure AI chips by the Taltech team and researchers world-wide.

Short Bio

Jaan Raik is a Full Professor and Head of the Center for Dependable Computing Systems at the Tallinn University of Technology (Taltech), Estonia, where he received his M.Sc. and Ph.D. degrees in 1997 and in 2001, respectively. His research interests cover a wide area in electrical engineering and computer science domains including reliability of deep learning, hardware test, functional verification, fault-tolerance and security as well as emerging computer architectures. He has co-authored more than 400 scientific publications. He is the National Contact for the Estonian Chip Competence Center KIIP, a member of ISO PAS 8800 standardization committee (AI functional safety for automotive), a EUROPRACTICE and ARM Academic Access representative, a member of IEEE Computer Society, HiPEAC and of Steering/Program Committees of numerous

conferences within his field. He has been active in organizing top-level international conferences at the General Chair (IEEE European Test Symposium'25,'20, IFIP/IEEE VLSI-SoC'16, DDECS'12), Vice General Chair (IEEE European Test Symposium'24, DDECS'13), Program Co-Chair (DDECS'23,'15, CDN-Live'16) and Local Organization Chair (IEEE European Test Symposium'05) levels. He was awarded the Global Digital Governance Fellowship at Stanford University (2022), HiPEAC Paper Award (2020), the Order of the White Star 4th class medal by the President of Estonia (2016) and Estonian Academy of Science's Bernhard Schmidt Award for innovation (2007). He coordinated several European-level research and collaboration actions including the Horizon 2020 RIA IMMORTAL, the Horizon 2020 Twinning TUTORIAL and the FP7 DIAMOND.

KEYNOTE 6

Time: Friday, 13:30 - 14:30

"In-Memory Sensing by Switching Devices"

Sandro Carrara

Professor and Head of the Bio/CMOS interfaces laboratory at the EPFL in Lausanne (CH)

Chair: Jens Trommer

Abstract

During the past two decades, a number of switching devices have been demonstrated in literature. They typically exhibit hysteric behavior in the current-to-voltage characteristics when driven by the source-drain potential in two-terminal configurations, or when driven by a proper potential to the program gate. Literature called them memristors in the first case, or reconfigurable transistors in the second. The switching capability of these devices made them particularly well-suited for applications to in-memory computing or in-memory sensing. The aim of this perspective keynote is then twofold. On one hand, it seeks to provide a comprehensive examination of the existing switching devices.

On the other hand, it proposes CMOS architectures based on switching devices with aim to develop new non-Von-Neumann computing machines that can seamlessly integrate sensing and computing within memory units. Therefore, this keynote aims to demonstrate practical applications of such an innovative approach to the realm of cancer diagnostics, by exploiting the modern concept of simultaneously employing multiple cancer biomarkers to enhance the efficiency of diagnostic processes in cancer medicine.

Short Bio

Sandro Carrara is an IEEE Fellow (F'15) and the recipient of the IEEE Sensors Council Technical Achievement Award in 2016, and the Scientist Medal by the International Association of Advanced Materials in 2024. He is Professor at the EPFL in Lausanne (CH), and Head of the Bio/CMOS interfaces laboratory. He is also a former professor at the Universities of Genoa and Bologna (IT). He holds a PhD in Biochemistry and Biophysics from University of Padua (IT), a master degree in physics from University of Genoa (IT), and a diploma in Electronics from National Institute of Technology in Albenga (IT). Along his career, he published 7 books with prestigious publishers such as Springer/NATURE and Cambridge University Press. He has more than 400 scientific publications and is author of 19 patents/patent-requests. He is former Editor-in-Chief of the IEEE Sensors Journal, one of the largest journals among 220 IEEE publications, and Associate Editor of IEEE Transactions on Biomedical Circuits and Systems. He is also former Founding Editor-in-Chief of the Springer/NATURE journal titled NanoBioScience. He is a member of the IEEE Sensors Council and his Executive Committee. He was a member of the Board of Governors (BoG) of the IEEE Circuits And Systems Society (CASS). He has been appointed as CASS Distinguished Lecturer for the years 2013-2014, and IEEE Sensors Council Distinguished Lecturer for the years 2017-2019. His work has constantly received international recognition with several best-cited papers and best conference papers. He has been the General Chairman of the premier worldwide international conference in the area of circuits and systems for biomedical applications, IEEE BioCAS, in 2014. He also has been the General Chairman of the 16th Edition of IEEE International Symposium on Medical Measurements and Applications, IEEE MeMeA, in 2021.

INDUSTRY PANEL

PANELISTS (ALPHABETICAL ORDER)

Dr. Jürgen Daleiden

VP Product Development
GlobalFoundries, Dresden

Dr. Christian Koitzsch

President and managing director of the European Semiconductor Manufacturing Company (ESMC), Dresden

Prof. Dr. Ronald Tetzlaff
Co-Founder of CMC Chua Memristor Center, Chief Officer Technology Transfer and Internationalisation (CTIO) of TUD

J. Joshua Yang

Cofounder & Scientific Board Chief Advisor
TetraMem, USA

AGENDA

- 14:45-15:45 Panelist Talks
- 15:45-16:00 Coffee Break
- 16:00-17:15 Panel Discussion

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REGULAR SESSION 1:
ANALOG/RF AND MIXED SIGNAL CIRCUITS

CHAIRS : GEORGIOS PANAGOPOULOS / MARIA PAPADOPOULOU

Monolithic Integrated GaN Circuit for Temperature Compensated Biasing

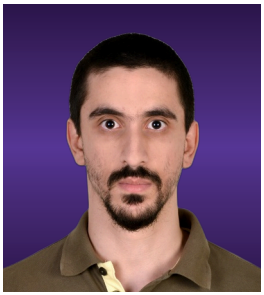
Time: Wednesday 10:30 - 10:48

Keywords: bandgap reference, GaN HEMT, temperature compensation, temperature sensor

Eleftherios Sarris (Circuits Integrated Hellas), Vasileios Christodoulou (Circuits Integrated Hellas), Errikos Lourandakis (Circuits Integrated Hellas), Nikolaos Makris (Foundation for Research & Technology - Hellas (FORTH), Inst. Electronic Structure & Laser, Heraklion, Greece), Antonios Stavrinidis (Foundation for Research & Technology - Hellas (FORTH), Inst. Electronic Structure & Laser, Heraklion, Greece), Athanasios Kostopoulos (Foundation for Research & Technology - Hellas (FORTH), Inst. Electronic Structure & Laser, Heraklion, Greece), Evangelos Aslanidis (Foundation for Research & Technology - Hellas (FORTH), Inst. Electronic Structure & Laser, Heraklion, Greece), Giannis Kontogiannopoulos (Circuits Integrated Hellas) and Paolo Fioravanti (Circuits Integrated Hellas)

Abstract

This paper presents a monolithic integrated circuit for temperature compensated biasing. The design is based on Gallium Nitride (GaN) high electron mobility transistors (HEMTs) on silicon (Si). The GaN process developed for this design currently provides only depletion-mode (D-mode) HEMTs. A proportional to absolute temperature voltage is created as well as a constant over temperature reference voltage, both are provided as output signals over a temperature range of −60 C up to 250 C. A temperature sensor is also integrated into the biasing circuit design, as an extra feature, with a sensitivity of −50mV / C and a full scale linearity of 6.5%. The biasing circuit operates on a 24V supply voltage, with a direct current (DC) power consumption of 165mW.



Design Cycle Speed up of Product Level Voltage References

Time: Wednesday 10:48-11:06

Keywords: Simulated annealing, Dual annealing, Nelder-Mead, Automated circuit sizing

Savvas Karipidis (Aristotle University of Thessaloniki), Andi Buzo (Infineon Technologies AG), Georg Pelz (Infineon Technologies AG) and Thomas Noulis (Aristotle University of Thessaloniki)

Abstract

In this work a methodology mainly consisting of a targeted combination of non-linear, direct-search algorithms is being utilized, the dual annealing and the Nelder-Mead ones, enabling high level of integrated circuit design automation with nearly zero user input. The methodology's efficiency is demon- strated via a 21 parameter bandgap reference circuit. The result is 0.84 ppm, 91% lower than the standard methodology applied to the same circuit with 12 μW, 40% less power consumption. It is achieved through 1260 simulations, in roughly 26 minutes.

REGULAR SESSION 1:
ANALOG/RF AND MIXED SIGNAL CIRCUITS

CHAIRS: GEORGIOS PANAGOPOULOS / MARIA PAPADOPOULOU

A Cuff-Less Blood Pressure Estimation System Based On Low-Power Analog Integrated Neural Network.

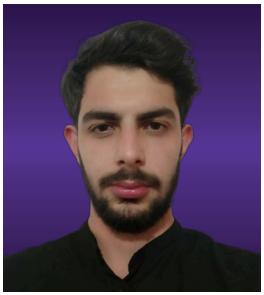
Time: Wednesday 11:06 - 11:24

Keywords: analog integrated design, low-power architecture, cuff-less blood pressure classifier, artificial

Vassilis Alimisis (National Technical University of Athens), Anna Mylona (National Technical University of Athens), Konstantinos Cheliotis (National Technical University of Athens), Vasileios Moustakas (National Technical University of Athens), Zisis Foufas (National Technical University of Athens) and Paul P. Sotiriadis (National Technical University of Athens)

Abstract

In this work, a power-efficient analog integrated artificial neural network architecture is presented. The high-level architecture consists of circuits that operate in the sub-threshold region, such as the sigmoid function circuit, Euclidean distance circuit, tunable current mirrors and a current comparator. The proposed artificial neural network is tested on a cuff-less blood pressure estimation classification task. The total power consumption is equal to 512nW and it achieves a mean accuracy of 95.1%. The proposed architecture is implemented and tested using the TSMC 90nm CMOS process, using the Cadence IC Suite for both schematic and layout design. To confirm the robustness of the proposed solution, both Monte Carlo and corner analysis are conducted. Additionally, post-layout results are compared with both software implementations and existing analog hardware solutions in terms of power and efficiency.



A Low-Power Analog Integrated Decision Tree for Diabetic Retinopathy Detection.

Time: Wednesday 11:24 - 11:42

Keywords: analog integrated design, low-power architecture, decision tree classifier, diabetic retinopathy

Vasileios Moustakas (National Technical University of Athens), Vassilis Alimisis (National Technical University of Athens), Zisis Foufas (National Technical University of Athens), Konstantinos Cheliotis (National Technical University of Athens), Anna Mylona (National Technical University of Athens) and Paul P. Sotiriadis (National Technical University of Athens)

Abstract

A power-efficient analog integrated decision tree classifier is presented in this work. Circuits that function in the sub-threshold region, including the argmax operator circuit and the Gaussian function circuit, constitute up the high-level architecture. A diabetic retinopathy detection classification task is used to evaluate the proposed classifier. It achieves a mean accuracy of 89.21% and consumes 1645nW. The Cadence IC Suite is used for both schematic and layout design in the implementation and testing of the proposed design, utilizing the TSMC 90nm CMOS process. Both Monte Carlo and corner analysis are used to verify the robustness of the proposed solution. In terms of power and efficiency, post-layout results are also compared with software implementations and existing analog hardware solutions.

REGULAR SESSION 1: ANALOG/RF AND MIXED SIGNAL CIRCUITS

CHAIRS: GEORGIOS PANAGOPOULOS / MARIA PAPADOPOULOU

Low-Rank Equilibrium Propagation: an on-line Incremental Learning Architecture for analog-based Hardware-Accelerators

Time: Wednesday 11:42 - 12:00

Keywords: analog neural networks, equilibrium propagation, memristors, machine learning, low-rank

Mohamed Watfa (LIRMM, Univ Montpellier, CNRS), Alberto Garcia Ortiz (University of Bremen) and Gilles Sassatelli (LIRMM, Univ. Montpellier II / CNRS)

Abstract

Edge machine learning is emerging as a fundamental technology to address the rapid growth of smart devices and sensors; however, deploying deep learning at the edge remains challenging due to limited memory and computational capacity. Among analog processing solutions, Equilibrium Propagation (EP) has gained attention as a promising alternative to backpropagation, offering significant potential for embedded systems, yet its practical implementation remains difficult. In this work, we introduce a novel method to overcome EP's limitations by proposing a low-rank approximation of the EP algorithm, enabling efficient, end-to-end online incremental training on analog neuromorphic accelerators—crucial for handling aging effects, imprecise memristor programming, and other hardware imperfections. While EP provides a unified forward and backward process, its standard form requires storing a gradient per device, resulting in substantial area and power overhead. Our proposed Low-Rank Equilibrium Propagation (LOREP) scheme mitigates this issue by approximating gradients with low-rank factors, reducing the need for high-precision storage and minimizing read–write cycles. Experimental results on two popular datasets show that LOREP recovers 2–3% in accuracy despite significant gradient approximation, highlighting its promise for deployment in resource-constrained environments.

Power Amplifier Design With 8 dBm Saturated Output Power in D-band in 22-nm FDSOI Technology

Time: Wednesday 12:00 - 12:18

Keywords: D-band, power amplifier, stability

Hatem Mahmoud Elsayed Elfekey (Chair of High Frequency Electronics, RWTH Aachen University), Xun Chen (Chair of High Frequency Electronics, RWTH Aachen University), Muh-Dey Wei (Chair of High Frequency Electronics, RWTH Aachen University), Kareem Khattab (Chair of High Frequency Electronics, RWTH Aachen University), Mohamed Elsayed (Chair of High Frequency Electronics, RWTH Aachen University), Jonas Winkelhake (Chair of High Frequency Electronics, RWTH Aachen University), Adrian Arnold (Chair of High Frequency Electronics, RWTH Aachen University), David Bierbüsse (Chair of High Frequency Electronics, RWTH Aachen University) and Renato Negra (Chair of High Frequency Electronics, RWTH Aachen University)

Abstract

D-band power amplifiers (PAs) are critical components for 6G communications. While unconditional stability in the frequency band of interest is regularly taken into account in the design process, the stability at lower frequencies are also required to be evaluated to avoid possible oscillation problems. In this paper, we propose a power amplifier in D-band stabilized from DC to fmax in simulation by introducing custom inductors at the gate terminals of the pseudodifferential stage with cross-coupled neutralization capacitance, CN. The design methodology of the PA and the implementation of the inductors are comprehensively discussed. By cascading four stages with transformer matching networks, the PA achieves a gain of 16.2 dB, 8 dBm of saturated output power, and an OP1dB of 3.6 dBm.

REGULAR SESSION 1:
ANALOG/RF AND MIXED SIGNAL CIRCUITS

CHAIRS: GEORGIOS PANAGOPOULOS / MARIA PAPADOPOULOU

A 28 GHz Low-Phase Noise QVCO in 22nm FD-SOI using Back-Gate Coupling

Time: Wednesday 12:18 - 12:36

Keywords: QVCO, Back-gate Feedback, Active Coupling, Phase Noise, CMOS 22nm FDSOI, Frequency

Georgios Panagopoulos (ECE, National Technical University of Athens), Vasileios Chondrorizos (ECE, TU Delft), Vasileios Manouras (ECE, National Technical University of Athens) and Yannis Papananos (ECE, National Technical University of Athens)

Abstract

This paper presents a quadrature VCO with an output frequency centered at 28 GHz, making it well-suited for 5G and 6G applications. A novel feedback technique utilizing the transistors' back-gate is proposed to couple the two VCOs. The core of the two LC-tuned QVCOs is optimized to achieve superior phase noise, making it highly suitable for mmWave frequency synthesizers. Developed in 22nm FDSOI technology, the proposed VCO operates from 27 GHz to 29.2 GHz, achieving a phase noise of -113 dBc/Hz at a 1 MHz offset relative to the 28 GHz carrier frequency. It demonstrates an excellent FoM of -196 dBc/Hz and a tuning range of 8%, while consuming 4 mW from a 0.8V supply.

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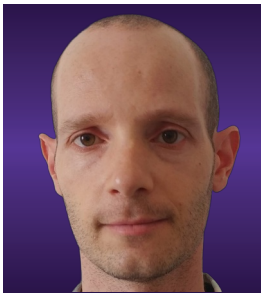
REGULAR SESSION 2: SENSORS AND SYSTEMS

CHAIRS: RICHARD SCHROEDTER / CARSTEN KNOLL



Implementation of Novel Multi-Step Bridge Fault Current Limiter for Transient Stability Enhancement of DFIG-Based Wind Turbines

Time: Wednesday 10:30 - 10:48

Keywords: Fault current limiter, Power system stability, wind turbine

Slava Demin (Shamoon College of Engineering, Tallinn University of Technology), Eduard Petlenkov (Tallinn University of Technology), Juri Belikov (Tallinn University of Technology), Eli Barbie (Shamoon College of Engineering), Svetlana Bronshtein (Shamoon College of Engineering) and Dmitry Baimel (Shamoon College of Engineering)

Abstract

The increasing integration of wind energy necessitates robust fault management strategies to enhance grid stability. This paper proposes a multistep bridge-type FCL with dynamic impedance regulation to improve transient stability in DFIG-based wind turbines. The proposed FCL effectively limits fault currents, stabilizes DC-link voltage, and minimizes torque and power oscillations. Simulation results confirm that the proposed FCL outperforms conventional solutions, including the SDBR and BFCL, by achieving superior fault suppression and system recovery. The stepwise impedance control reduces switching losses, component stress,and electromagnetic interference, ensuring a cost-effective and practical implementation. Future work will focus on experimental validation and large-scale integration.

Direction of Arrival Estimation Using Compressive Sensing and Green's Function Interpretation for a Frequency-Diverse Metasurface

Time: Wednesday 10:48 - 11:06

Keywords: DoA, metasurface, compressive sensing, green's function, single pixel antenna, frequency diverse wave chaotic

Mohammed Hassan Arif (Chair of High Frequency Electronics, RWTH Aachen University), Firas Dawod (School of Science and Engineering, University of Missouri-Kansas City), Renato Negra (Chair of High Frequency Electronics , RWTH Aachen University) and Sayan Roy (School of Science and Engineering, University of Missouri-Kansas City)

Abstract

This paper presents the theoretical foundation of an advanced direction of arrival (DoA) method by integrating a single-pixel metasurface, Green's function, and compressive sensing (CS). Using a metasurface for DoA estimation reduces hardware complexity by enabling single-port feeding and eliminating the need for phase shifters to generate multiple radiation patterns. The study begins with the design of a frequency-diverse metasurface composed of only two types of unit cells, followed by a detailed derivation of the associated transfer matrix using Green's function. The spatial characteristics of incident waves in the 26.5 GHz to 28.5 GHz range are analyzed by solving the forward model using CS. Experimental validation using MATLAB under various angles of incidence and signal-to-noise ratio (SNR) levels demonstrates that the proposed method accurately identifies multipath DoAs, showcasing its effectiveness and precision.

REGULAR SESSION 2: SENSORS AND SYSTEMS

CHAIRS: RICHARD SCHROEDTER / CARSTEN KNOLL

Federated Learning for Workload Forecasting for Network Service Management

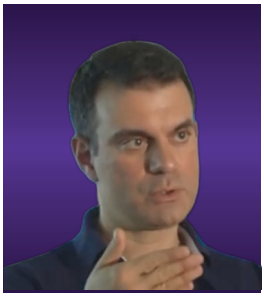
Time: Wednesday 11:06 - 11:24

Keywords: time-series forecasting, federated learning, computing continuum

Dimitrios Brodimas (University of Patras), Dimitrios Kapolos (University of Patras), Eleftherios Mylonas (University of Patras), Alexios Birbas (University of Patras) and Michael Birbas (University of Patras)

Abstract

The continuous expansion and transformation of next-generation networks poses significant challenges for management and orchestration (MANO) frameworks to efficiently address the growing computational demands, especially at the network edge. To enhance MANO decision-making, it is crucial to proactively identify both periodic and aperiodic patterns that influence network behavior. This paper introduces a computational load forecasting method aimed at equipping MANO frameworks with predictive insights into infrastructure conditions. The forecasting approach utilizes machine learning models such as LSTMs and Bi-LSTMs, integrated with the FedOpt family of federated learning algorithms to enable distributed training. Experimental results show that the proposed federated strategy achieves performance on par with centralized learning methods while substantially reducing the volume of data exchanged between edge nodes and the cloud.



Victim Detection Using a Robot-Mounted UWB-Radar Platform

Time: Wednesday 11:24 - 11:42

Keywords: Radar sensors, Victim detection, Search-and-Rescue, Robotic platforms, Machine learning

Antonios Periklis Michalopoulos (University of West Attica), Efstratios N. Paliodimos (University of West Attica), Fotios Papadopoulos (University of West Attica), Grigoris Nikolaou (University of West Attica), Charalampos Patrikakis (University of West Attica) and Stylianos A. Mytilinaios (University of West Attica)

Abstract

Search-and-Rescue (SAR) operations typically rely on sensor platforms to detect victims behind walls, obstacles etc. Thermal and acoustic sensors often struggle to detect victims in obstructed environments, but Ultra-wideband (UWB) radar may play a crucial role in penetrating obstacles and detecting subtle movements and breathing of surviving victims. Meanwhile, robots may enhance disaster response by improving the speed and efficiency of SAR operations, especially in hazardous environments. This paper presents a robotic platform equipped with UWB radar to detect and locate victims behind obstacles by identifying respiration. To achieve this, we developed a dataset of breathing patterns from victim actors behind a wall, and propose two machine learning techniques for detection and victim range estimation. The system incorporates LiDAR and a camera for navigation and controller operation, while a visualization method for victim localization is showcased. Experimental results indicate an F1-score of 94% for victim detection and a Mean Absolute Error (MSE) of 0.083 for distance estimation.

REGULAR SESSION 2: SENSORS AND SYSTEMS

CHAIRS: RICHARD SCHROEDTER / CARSTEN KNOLL

Sparse-KSVD for Blind Decomposition on Task-Related fMRI Data: A Comparative Analysis with ICA and MCA-KSVD

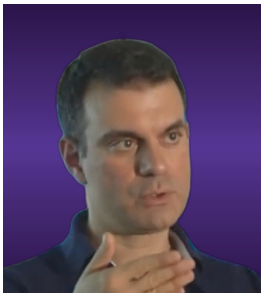
Time: Wednesday 11:42 - 12:00

Keywords: independent component analysis, morphological component , sparse dictionary learning, KSVD, fMRI network decomposition, task-related fMRI

Phuc Truong Loc Nguyen (Friedrich-Alexander-Universität Erlangen-Nürnberg) and Phuoc Khang Nguyen (Technische Universität Dresden)

Abstract

Functional MRI (fMRI) data analysis enables researchers to partition the brain into distinct regions, offering valuable insights into neurological disorders. A widely used decomposition technique is Independent Component Analysis (ICA), which identifies functional brain networks by assuming statistical independence between components. However, this assumption may not fully align with the physiological characteristics of fMRI data. To address these limitations, this study explores Sparse-KSVD, a KSVD-based method with limited prior application in fMRI research, for identifying functional brain networks. Sparse-KSVD is systematically compared to MCA-KSVD, another KSVD-family method, and the conventional ICA using task-related fMRI data. The analysis shows that Sparse-KSVD accurately identifies functional brain networks with results comparable to those of ICA and MCA-KSVD. Furthermore, Sparse-KSVD outperforms both in signal localization and spatial resolution under optimal parameter settings. These findings demonstrate that Sparse-KSVD is a promising alternative to ICA and MCA-KSVD. However, careful parameter tuning is essential to achieve its full potential.



A radar-based berthing-aid system (R-BAS).

Time: Wednesday 12:00 - 12:18

Keywords: FMCW radar, obstacle detection, maritime safety, autonomous navigation, clustering, tracking, sensor fusion

Fotios Papadopoulos (University of West Attica), Efstratios Paliodimos (University of West Attica), Antonios-Periklis Michalopoulos (University of West Attica), Ioannis Christopoulos (University of West Attica), Charalampos Patrikakis (University of West Attica), Alexandros Simopoulos (Attica Group S.A.) and Stylianos A. Mytilinaios (University of West Attica)

Abstract

Safe berthing is a critical challenge for maritime vessels. This paper presents a proof-of-concept system using Frequency-Modulated Continuous Wave (FMCW) radars to detect, cluster, and track obstacles—mainly the dock—behind a ferry. The proposed system consists of a waterproof enclosure with four radar sensors at the 60-67 and 77-81 GHz frequency bands, incorporating an edge processing unit, various environmental sensors, a GPS sensor, as well as a sub-module for off-site remote control, data monitoring and telemetry. A video camera is used for visualization purposes, whereas radar and video data are captured at 20 fps and locally stored. At the post-process, radar detected points are clustered using the DBSCAN algorithm, while Kalman filtering is used for consistent cluster tracking and identification. Real-world experiments were conducted on an operational Ro-Ro / Passenger Ship under various weather conditions. Test results confirmed the feasibility of consistent dock detection using the proposed radar system and provide a proof-of-concept for short-range maritime obstacle detection, with potential applications in autonomous navigation.

SPECIAL SESSION 1: EMERGING MEMORY DEVICES FOR IN-MEMORY AI: FROM MATERIALS TO SYSTEM INTEGRATION

CHAIRS: THOMAS KÄMPFE / ALPTEKIN VARDAR

A Vertical Memristive MoS2-exfoliated Device for Applications in Artificial Synapses

Time: Wednesday 16:00 - 16:18

Keywords: Neuromorphic computing, Memristor, Molybdenum disulfide, Exfoliation, Schottky barrier height modulation

Dejanira Fejzaj (Chair of Nanoelectronics, TU Dresden), Richard Schroedter (Chair of Fundamentals of Electrical Engineering, TU Dresden), Thomas Mikolajick (NaMLab gGmbH; Chair of Nanoelectronics, TU Dresden) and André Heinzig (Chair of Nanoelectronics, TU Dresden).

Abstract

Extensive research is directed towards neuromorphic computing, a hardware-based processing paradigm inspired by the human brain, to satisfy the need for more efficient computing. State-of-the-art resistive switching devices also called memristors use 2D transitional metal dichalcogenide materials as a switching material and can potentially be used as next-generation neuromorphic devices. Two-dimensional transitional metal dichalcogenides prepared by chemical vapor deposition are the most employed in resistive switching devices since the layers contain defects like vacancies and grain boundaries that can induce resistive switching effects. However, only a few studies have investigated resistive switches based on exfoliated layers and exploited the superior crystalline quality. In this work, a vertical memristor based on exfoliated molybdenum disulfide is demonstrated, which reveals a resistive switching mechanism based on Schottky barrier height modulation. The devices exhibit a forming-free, gradual resistive switching characteristic. We attribute the switching mechanism to either the motion of sulfur vacancies induced by a voltage bias applied to the device or charge trapping, which modulates the molybdenum disulfide/metal barrier. We present the characteristic quasi-static I-V behavior as well as synaptic potentiation and depression, demonstrating the potential of being a basic device to realize synapses for neuromorphic systems.

Nucleation-limited-switching based compact models for Hf-based ferroelectric devices and their applications in memory arrays

Time: Wednesday 16:18 - 16:36

Keywords: FTJs, FeCAPs, compact model, NLS, memory array, IMC

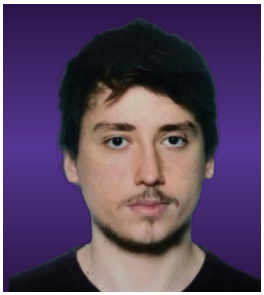
Chong Peng (NaMLab gGmbH), Suzanne Lancaster (NaMLab gGmbH), Luca Carpentieri (NaMLab gGmbH), Athira Sunil (NaMLab gGmbH), Thomas Mikolajick (NaMLab gGmbH, Dresden, Germany) and Stefan Slesazeck (NaMLab gGmbH, Dresden, Germany)

Abstract

In-memory computing is a promising approach for realizing energy-efficient computing engines for artificial inteligence hardware accelerators. Among various memory technologies, ferroelectric devices stand out as strong candidates for in-memory computing due to their nonvolatile nature, low energy consumption, and multi-bit capability. For large-scale ferroelectric device-based memory circuit design, accurate and efficient compact models are essential. However, modeling these devices remains challenging due to their complex switching dynamics, which involve nucleation process of multiple domains and intricate interface states. This work presents a compact model based on the Nucleation-Limited Switching theory for simulating ferroelectric capacitors and ferroelectric tunnel junctions. By incorporating flexible mathematical models for current, these models accurately capture the switching kinetics and I-V characteristics of discrete devices. Moreover, their simple mathematical structure ensures high stability and robustness in memory circuit simulations, which is verified in an FTJ-based 32×32 crossbar array.

SPECIAL SESSION 1: EMERGING MEMORY DEVICES FOR IN-MEMORY AI: FROM MATERIALS TO SYSTEM INTEGRATION

CHAIRS: THOMAS KÄMPFE / ALPTEKIN VARDAR



People Counting and Positioning Using Low-Resolution Infrared Images for Resource-Constrained Edge Devices

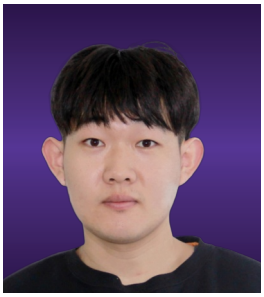
Time: Wednesday 16:36 - 16:54

Keywords: Infrared imaging, People counting, Indoor positioning, Edge inference, YOLO, Quantization, Pruning

Alptekin Vardar (Fraunhofer IPMS), Li Zhang (Fraunhofer IPMS), Marc Lupp (Heimann Sensor GmbH), Alexander Rehmer (Heimann Sensor GmbH), Nandakishor Yadav (Fraunhofer IPMS) and Thomas Kämpfe (Fraunhofer IPMS)

Abstract

This paper presents a people counting and indoor positioning system using low-resolution infrared video from a thermopile sensor, optimized for deployment on resource-constrained edge devices. A lightweight YOLOv3-tiny network is trained on a custom thermal dataset and enhanced through quantization-aware training and structured pruning. Pre-processing techniques such as Otsu thresholding and morphological filtering are used to suppress noise and reduce image size by over 80 percent with minimal accuracy loss. The final model—quantized to 4 bits and pruned by 50 percent—achieves 57.71 precent mAP at 0.5 while significantly lowering memory and compute demands. Results validate the system's suitability for privacy-preserving, low-power applications in smart environments.



Thermal-Compensated MRAM Sensing: Dynamic TMR Stabilization Across Wide Temperature Range

Time: Wednesday 16:54 - 17:12

Keywords: SOT-MRAM, Temperature-Adaptive, Reliability, stabilized TMR

Tuo Zhang (Beihang University), Xinpeng Jiang (Beihang University), Chao Wang (Beihang University), Bi Wang (Beihang University), Hongxi Liu (Truth Memory Corporation), Kaihua Cao (Beihang University), Xuan Li (Truth Memory Corporation), Hui Jin (Beihang University), Gefei Wang (Truth Memory Corporation), Zhaohao Wang (Beihang University), Weisheng Zhao (Beihang University) and He Zhang (Beihang University)

Abstract

The Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM) demonstrates significant potential for high-speed, low-power applications, garnering considerable attention from both academia and industry. However, due to the physical properties of magnetic tunnel junction (MTJ) itself, tunnel magnetoresistance ratio (TMR) will decrease with increasing temperature, thereby reducing the reliability of MRAM and posing a key challenge to the application of MRAM chips. To address this issue, this paper proposed a reliable temperature-adaptive Sensing Scheme (TASS) for SOT-MRAM, which can stabilize TMR across a wide temperature range from -40°C to 125°C by dynamically adjust read voltage. Simulation results at 28nm indicate that TASS reduces the TMR degradation from 25% to 5% as the temperature increases from -40°C to 125°C, while exhibiting a current adjustment capability of 142%. Furthermore, the proposed readout circuit ensures a lower worst-BER over the same temperature range, providing a substantial enhancement in read reliability by 3 orders of magnitude

SPECIAL SESSION 1: EMERGING MEMORY DEVICES FOR IN-MEMORY AI: FROM MATERIALS TO SYSTEM INTEGRATION

CHAIRS: THOMAS KÄMPFE / ALPTEKIN VARDAR

Integrating P-bits in MTJs: A Bridge to Efficient Stochastic Computing

Time: Wednesday 17:12 - 17:30

Keywords: Stochastic Computing, Probabilistic bits, Compute-In-Memory-, MTJ, neural network, non-volatile memory, MAC

Nellie Laleni (Fraunhofer IPMS), Sina Ranjbar (Fraunhofer IPMS), Ran Zhang (Fraunhofer IPMS), Andreas Tsiougkos (Aristotle University of Thessaloniki), Nandakishor Yadav (Fraunhofer IPMS), Vasilis Pavlidis (Aristotle University of Thessaloniki) and Thomas Kämpfe (Fraunhofer IPMS / TU Braunschweig)

Abstract

Probabilistic computing has emerged as a promising paradigm to tackle computational challenges in artificial intelligence (AI), machine learning (ML), and optimization tasks. Unlike deterministic computing, it leverages controlled randomness to enhance efficiency and scalability. This paper explores the integration of probabilistic bits (p-bits) within magnetic tunnel junction (MTJ) devices, utilizing their inherent stochastic switching behavior to implement probabilistic computing architectures. We demonstrate how MTJs enable energy-efficient, hardware-compatible solutions by eliminating the need for complex pseudo-random number generators. A crossbar-based p-bit array is proposed, incorporating a digital-to-analog converter (DAC) and a sense amplifier (SA) to facilitate probabilistic operations. This work highlights MTJ-based probabilistic computing as a viable alternative for future low-power, high-performance AI accelerators.

REGULAR SESSION 3: DEVICE AND CIRCUIT MODELING

CHAIRS: IOANNIS MESSARIS / DIMITRIS PROUSALIS

Empirical Programming Protocol and Monitor-Free Multi-Level Modulation for Memristors

Time: Wednesday 16:00 - 16:18

Keywords: Stochastic memristor, empirical protocol, multi-level programming, monitor-free

Lijie Xie (Department of Electrical and Electronic Engineering, Imperial College London), Qianyi Zhang (Independent researcher) and Christos Papavassiliou (Department of Electrical and Electronic Engineering, Imperial College London)

Abstract

Hands-on memristor operations for multi-level applications present significant challenges due to the inherent uncertainty in memristor responses and the frequent occurrence of device failures. For practical implementation, memristors must demonstrate well-defined bipolar and multi-level modulation behaviours that remain reproducible over extended operations. To facilitate rapid and comprehensive multi-level memristor characterisation, this paper introduces an empirical tuning protocol. Building on the memristor's ability to achieve voltage-dependent saturation resistance, the concept of monitor-free multi-level programming is proposed, with an 8-level experimental attempt conducted for validation.

REGULAR SESSION 3: DEVICE AND CIRCUIT MODELING

CHAIRS: IOANNIS MESSARIS / DIMITRIS PROUSALIS

Verilog-A look-up table model of a TIG-RFET compatible with 22 nm FDSOI design rules satisfying Gummel Symmetry

Time: Wednesday 16:18 - 16:36

Keywords: Verilog-A, Three-Independent-Gate Transistor, Reconfigurable Electronics, RFETs, Source-Drain Symmetry, Device Modelling

Juan Martinez (NaMLab gGmbH), Niladri Bhattacharjee (NaMLab gGmbH), Yuxuan He (NaMLab gGmbH), Giulio Galderisi (NaMLab gGmbH), Nima Kavand (Chair of Processor Design, TU Dresden, Helmholtzstraße 18, 01069 Dresden, Germany), Akash Kumar (Chair of Embedded Systems, Ruhr-Universität Bochum, 44801 Bochum, Germany), Thomas Mikolajick (Chair for Nanoelectronics, TU Dresden, Nöthnitzer Str. 64, 01187 Dresden, Germany) and Jens Trommer (NaMLab gGmbH)

Abstract

The advent of AI has brought massive demands on electronic hardware. This has motivated the development of in-hardware computation, where the circuit elements mimic parts of the brain cognitive processes. Three-independent-gate reconfigurable transistors are a promising technology due to its built-in adaptability and potential for low current operation. However, the development of circuit level applications is limited due to a lack of suitable models. The complexity of multiple gates has limited the development of compact models, while TCAD simulation tools are not suitable to model blocks comprising several transistors. A model compatible with circuit design tools like Cadence Virtuoso is needed. This work presents a Verilog-A look-up table model of an RFET device fully compatible with the 22nm FDSOI industrial platform. The table is populated from TCAD structural simulations. Crucially, a design solution is discussed to enable swapping of the physically symmetric source and drain terminals during simulations, without modifying the functionality, which is validated by passing the Gummel Symmetry Test.

Coexistence of resistive capacitive and virtual inductive effects in memristive devices

Time: Wednesday 16:36 - 16:54

Keywords: Compact model, Capacitive effects, Inertia effects, ReRAMs, interface-type switching

Sahitya Yarragolla (Chair of Applied Electrodynamics and Plasma Technology, Ruhr University Bochum, Bochum, Germany), Torben Hemke (Chair of Applied Electrodynamics and Plasma Technology, Ruhr University Bochum, Bochum, Germany), Jan Trieschmann (Theoretical Electrical Engineering, Faculty of Engineering, Kiel University, Kaiserstraße 2, 24143 Kiel, Germany) and Thomas Mussenbrock (Chair of Applied Electrodynamics and Plasma Technology, Ruhr University Bochum, Bochum, Germany)

Abstract

This paper examines the coexistence of resistive, capacitive, and virtual inductive effects in memristive devices, focusing on ReRAM devices, specifically the interface-type analog switching devices. A physics-inspired compact model is used to effectively capture the underlying mechanisms governing resistive switching in oxide-based memristive devices. The model includes different capacitive components in metal-oxide-metal structures to simulate capacitive effects. Drift and diffusion of particles are modeled and correlated with particles' inertia within the system. The inertial lag between particle drift velocity and the applied electric field is analyzed. Using the model, we obtain the \textit{I}-\textit{V} characteristics of devices that show good agreement with experimental findings and the corresponding \textit{C}-\textit{V} characteristics. This model also replicates observed non-zero crossing hysteresis in perovskite-based devices. Additionally, the study examines how the reactance of the device changes in response to variations in the device area and length.

REGULAR SESSION 3: DEVICE AND CIRCUIT MODELING

CHAIRS: IOANNIS MESSARIS / DIMITRIS PROUSALIS

RRAM-based Hardware Implementation of P Systems

Time: Wednesday 16:54 - 17:12

Keywords: P Systems, Bio-inspired Computing, Resistive Switching, RRAM

Emmanouil Stavroulakis (Department of Electrical and Computer Engineering, Democritus University of Thrace), Alexandros Mavropoulis (Department of Electrical and Computer Engineering, Democritus University of Thrace), Iosif-Agelos Fyrigos (Department of Electrical and Computer Engineering, Democritus University of Thrace), Konstantinos Rallis (Department of Electrical and Computer Engineering, Democritus University of Thrace), Panagiotis Dimitrakis (National Center for Scientific Research ``Demokritos'') and Georgios Sirakoulis (Department of Electrical and Computer Engineering, Democritus University of Thrace)

Abstract

Conventional computing architectures face significant challenges in efficiently handling highly parallel models like Spiking Neural P (SNP) systems due to the inherent limitations of von Neumann architectures. Existing software simulators for P systems fail to fully exploit their parallelism, leading to limited scalability and high computational overhead. To address these issues, this work proposes a novel hardware implementation of SNP systems using Resistive Random Access Memory (RRAM) technology, which offers non-volatile, analog, and threshold-based computation by combining memory and processing capabilities. Leveraging these features, we introduce a hardware architecture that maps SNP system behavior onto RRAM-based interconnected circuits. The design comprises two main components: a spike counter subcircuit that encodes intercepted spikes in a neuron through RRAM conductance states, and a rule assessment subcircuit that employs threshold switching to evaluate and apply specific firing rules. Simulations based on the JART VCM RRAM model confirm the correct functionality of the proposed circuits,

demonstrating their capability to efficiently simulate SNP dynamics in hardware. This approach harnesses the unique properties of RRAM and paves the way for real-time, bio-inspired computing applications that transcend the limitations of traditional von Neumann systems.

Towards Formal Representation of Memristor-Related Domain Knowledge -- A Pragmatic Attempt

Time: Wednesday 17:12 - 17:30

Keywords: memristor, memristive device, ontology, knowledge graph, formal knowledge representation, RDF

Carsten Knoll (TUD Dresden University of Technology), Julius Fiedler (TUD Dresden University of Technology), Christian Bruchatz (TUD Dresden University of Technology), Richard Schroedter (TUD Dresden University of Technology) and Ronald Tetzlaff (TUD Dresden University of Technology)

Abstract

Computational ontologies (or knowledge graphs) are powerful established technologies to represent knowledge of a certain domain in a formal (i.\,e. machine-processable) way. While in the life sciences the usage of those technologies has been common for decades they are rarely applied to engineering domains. Especially for young and highly active sub-fields like the investigation of memristive devices and the related theory, formal knowledge representation promises a significant benefit for the consolidation of terminology and for knowledge transfer both within the scientific community and also towards practitioners. In this contribution we conduct a case study to create an experimental prototype -- the Ontology of Memristor Technology (OMT). We present a pragmatic approach based on two simple question answering use-cases. To achieve this we semi-automatically incorporate knowledge from certain overview papers and background knowledge from Wikidata. Based on a critical discussion of our results we also outline directions for further research.

SPECIAL SESSION 2: TRENDS IN MODERN COMPUTER ARITHMETIC AND DIGITAL NUMBER FORMATS

CHAIRS: JOCHEN RUST / MORITZ BÄRTHEL

Application-specific Arithmetic (Extended Abstract)

Time: Thursday 10:30 - 11:06

Keywords: computer arithmetic, accelerator, FPGA, ASIC

Martin Kumm (Fulda University of Applied Sciences) and Florent de Dinechin (CITI, INSA de Lyon, Université de Lyon, INRIA)

Abstract

Mainstream computer arithmetic is tailored to the microprocessor which has to be as universal and versatile as it can be. However, the end of Moore's law triggered the development of many hardware accelerators that are customized to very specific algorithms. The arithmetic operators in those accelerators do not need to be versatile nor universal, they need to do one thing for one application, and do it well (faster, cheaper, more accurately, or with less energy). Here, application-specific arithmetic designers have to face several degrees of freedom. Any precision can be designed, any number encoding, but also any operation and function, provided you are clever enough to implement it efficiently as a circuit. Based on our recently published book "Application-specific Arithmetic", this talk will give a survey of the opportunities offered by this freedom, and some of the key methodologies and tools that allow a designer to build and compose application-specific operators.

Please find the full abstract on the USB Flash drive!

Approximate Arithmetic Circuits Enabling Energy-efficient Edge Computing

Time: Thursday 11:06 - 11:24

Keywords: AI Computing, Arithmetic Circuits, Approximate Computing, Reconfigurable Architectures

Salim Ullah (TU Dresden), Siva Satyendra Sahoo (IMEC, Leuven) and Akash Kumar (Ruhr University Bochum)

Abstract

Approximate Computing (AxC) has emerged as a powerful technique for enabling efficient AI/ML workloads on resource-constrained edge devices. By judiciously introducing controlled inaccuracies, AxC leverages the inherent resilience of AI/ML models to unlock substantial gains in power, performance, and area (PPA). Nonetheless, the widespread adoption of AxC is hampered by the need for application-specific designs, which increase design and implementation complexity. To address this, we highlight advanced techniques for approximate arithmetic operator design—focusing on LUT-level optimizations, automated operator modeling, and design-space exploration on FPGAs. Through these methods, AI-enabled Electronic Design Automation (EDA) can effectively reduce development complexity and drive large-scale AxC adoption, paving the way for energy-efficient, scalable AI computing at the edge.

SPECIAL SESSION 2: TRENDS IN MODERN COMPUTER ARITHMETIC AND DIGITAL NUMBER FORMATS

CHAIRS: JOCHEN RUST / MORITZ BÄRTHEL

Streamlining SIMD ISA Extensions with Takum Arithmetic: A Case Study on Intel AVX10.2

Time: Thursday 11:24 - 11:42

Keywords: SIMD, ISA, AVX10.2, takum arithmetic, IEEE 754, floating-point numbers

Laslo Hunhold (University of Cologne)

Abstract

Modern microprocessors extend their instruction set architecture (ISA) with Single Instruction, Multiple Data (SIMD) operations to improve performance. The Intel Advanced Vector Extensions (AVX) enhance the x86 ISA and are widely supported in Intel and AMD processors. The latest version, AVX10.2, places a strong emphasis on low-precision, non-standard floating-point formats, including bfloat16 and E4M3/E5M2 float8 (OCP 8-bit Floating Point, OFP8), primarily catering to deep learning applications rather than general-purpose arithmetic. However, as these formats remain within the IEEE 754 framework, they inherit its limitations, introducing inconsistencies and added complexity into the ISA.

This paper examines the recently proposed tapered-precision takum floating-point format, which has been shown to offer significant advantages over IEEE 754 and its derivatives as a general-purpose number format. Using AVX10.2 as a case study, the paper explores the potential benefits of replacing the multitude of floating-point formats with takum as a uniform basis. The results indicate a more consistent instruction set, improving readability and flexibility while offering potential for 8- and 16-bit general-purpose SIMD arithmetic.

A Formal Evaluation of the Design Space for SORN Arithmetic Datatypes.

Time: Thursday 10:30 - 11:06

Keywords: computer arithmetic, number formats, SORN, FPGA

Moritz Bärthel (Universität Bremen), Yixuan Yao (Universität Bremen), Nils Hülsmeier (Universität Bremen) and Steffen Paul (Universität Bremen).

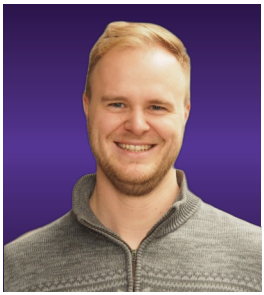
Abstract

The Sets of Real Numbers (SORN) format is a low-complex and low-latency approach for computer arithmetic based on intervals. The application-specific nature of the format was shown to be beneficial for several use cases, particularly regarding their hardware performance. However, a potentially large design space has to be evaluated per application for determining the best-suited SORN datatype configuration. In order to generalize this approach and to allow for more-flexible designs, this work describes a formal evaluation of the design space of SORN datatypes, analyzes how many configurations exists per bitwidth, and to what extend shared-logic SORN operations can be implemented.

After deriving a general approach to determine all different SORN datatypes per bitwidth, a comprehensive evaluation of the hardware implementation of SORN datatypes for low bitwidths up to 11 bit is carried out for the arithmetic operations of addition and multiplication. The results show that the proposed shared-logic implementation of multi-datatype SORN operations significantly reduces the required hardware resources, compared to the instantiation of multiple single-datatype modules.

SPECIAL SESSION 2: TRENDS IN MODERN COMPUTER ARITHMETIC AND DIGITAL NUMBER FORMATS

CHAIRS: JOCHEN RUST / MORITZ BÄRTHEL



Multiplier-Free Neural Networks: An Exploration of SORN-based Neural Networks on Hardware

Time: Thursday 12:00 - 12:18

Keywords: FPGA, hardware, Hybrid SORN, SORN, neural network, machine learning, MNIST

Nils Hülsmeier (University of Bremen), Jannik Steenken (University of Bremen), Moritz Bärthel (University of Bremen), Jochen Rust (HAW Hamburg) and Steffen Paul (University Bremen)

Abstract

Hardware implementations of neural networks are gaining attention across various application domains, yet traditional reliance on fixed- and floating-point multipliers leads to highly complex architectures. This paper explores an alternative approach using the Sets-Of-Real-Numbers (SORN) format, a binary number representation that operates on coarse interval resolutions to enable ultra-fast, low-complexity computation. SORN arithmetic — including multiplications and activation functions — can be realized using simple Boolean logic, eliminating the need for traditional multipliers. We present two multiplier-free feedforward neural network architectures for MNIST classification on FPGA, combining SORN arithmetic with fixed-point adders. Compared to half-precision floating-point implementations, our designs incur only a modest accuracy drop of 0.66% and 0.39%, respectively, while achieving substantial hardware savings: LUT usage is reduced by 87.8% and 91.4%, with no DSP usage, and throughput increases by factors of 20.4 and 15.98.

SORN-based Cross-Correlation for SCG Signal Peak Detection in Resource-Constrained Systems

Time: Thursday 12:18 - 12:36

Keywords: Computer Arithmetic, SORN, FPGA, SCG

Kazi Mohammad Abidur Rahman (Hamburg University of Technology), Ulf Kulau (Hamburg University of Technology) and Jochen Rust (Hamburg University of Applied Sciences)

Abstract

In this paper, a novel computation scheme of the cross-correlation for seismocardiography (SCG) peak detection in resource-constrained systems is proposed. As cost-optimized FPGAs are usually considered in this scope that contain only a small number of DSPs, the excessive use of multipliers quickly exceeds the available fabric resources. To overcome this drawback, Sets-Of-Real-Numbers (SORNs) are taken into account, which generally lead to a significant reduction of complexity at the cost of precision impairments. For evaluation, cross-correlation hardware architecture is implemented in VHDL considering SORN-based mutipliers into account and compared to standard fixed-point. The results show a reduction in complexity for LUTs of up to 46%, highlighting our approach as a very feasible solution for resource-constrained systems.

SPECIAL SESSION 3: ADVANCES IN MEMRISTIVE NEUROMORPHIC DEVICES AND CIRCUITS FOR ARTIFICIAL INTELLIGENCE & EDGE COMPUTING

CHAIRS: AHMET SAMIL DEMIRKOL / ALON ASCOLI

Memristor-Based Logic Gates and Circuits for Artificial Intelligence

Time: Thursday 10:30 - 10:48

Keywords: LTSPICE models, memristor logic gates, hard-switching mode, memristor-MOS transistor logic circuits

Stoyan Kirilov (Technical University of Sofia, Bulgaria, Dept. Fundamentals of Electrical Engineering) and Valeri Mladenov (Technical University of Sofia, Bulgaria, Dept. Fundamentals of Electrical Engineering)

Abstract

Memristors are novel electronic components in the nano-range, having good switching and memory properties, low power operation, and a compatibility to CMOS integrated circuits. Memory crossbars, neural nets, and many other schemes are some of their potential applications. This paper offers simple memristor-based logical gates for artificial intelligence, analyzed in LTSPICE and MATLAB. A plain and fast-operating modified memristor model is offered for the related analyses. It is tuned according experimental i-v relations of Self-directed channel Knowm memristors. A correct operation of considered logic functions is confirmed by the obtained results. During the analyses, several mainly used standard and modified memristor models are applied for comparison of their operation and properties. The suggested memristor-based logic gates are a significant step towards manufacturing of complex logic functions and schemes for artificial intelligence integrated circuits with ultra-high-density.

Model-based write algorithm for memristive crossbar arrays

Time: Thursday 10:48 - 11:06

Keywords: Model-based write algorithm, Memristive crossbar array, Analog switching compact memristor model

Richard Schroedter (Chair of Fundamentals of Electrical Engineering, TUD Dresden University of Technology), Ahmet Samil Demirkol (Chair of Fundamentals of Electrical Engineering, TUD Dresden University of Technology), Ioannis Messaris (Chair of Fundamentals of Electrical Engineering, TUD Dresden University of Technology), Christian Bruchatz (Chair of Fundamentals of Electrical Engineering, TUD Dresden University of Technology), Eter Mgeladze (NaMLab gGmbH), Stefan Slesazeck (NaMLab gGmbH), Thomas Mikolajick (NaMLab gGmbH) and Ronald Tetzlaff (Chair of Fundamentals of Electrical Engineering, TUD Dresden University of Technology)

Abstract

In this paper, we propose a model-based write algorithm for memristive crossbar arrays employing 1R analog-switching devices significantly improving write process efficiency over the conventional write-and-verify tuning algorithm. Leveraging a physics-based compact memristor model, we evaluate the V/2, V/3 and floating crossbar writing schemes and implement the novel developed algorithm based on the pulse time. Simulations of various crossbar sizes are conducted, assessing critical parameters including energy consumption, conductance overshoot, write time, number of iterations, and unselected cell error. We developed a versatile simulation platform that enables simulation of any SPICE-compatible memristor models, incorporating parasitic circuit elements like capacitances. The proposed algorithm significantly reduces the number of write iterations and time by half, while also lowering energy consumption and enhancing overall write accuracy.

SPECIAL SESSION 3: ADVANCES IN MEMRISTIVE NEUROMORPHIC DEVICES AND CIRCUITS FOR ARTIFICIAL INTELLIGENCE & EDGE COMPUTING

CHAIRS: AHMET SAMIL DEMIRKOL / ALON ASCOLI

A Simple Analog Neuron with Memristor Based Synapses and SATLINS Transfer function

Time: Thursday 11:06 - 11:24

Keywords: neural networks, circuits and systems, modeling and simulation, LTSPICE memristor models, memristor based neural networks, modified window

Georgi Tsenov (Technical University of Sofia, Bulgaria, Dept. Fundamentals of Electrical Engineering), Stoyan Kirilov (Technical University of Sofia, Bulgaria, Dept. Fundamentals of Electrical Engineering) and Valeri Mladenov (Technical University of Sofia, Bulgaria, Dept. Fundamentals of Electrical Engineering)

Abstract

Memristors are unique nano-length elements, having sound memorizing and switching features and due to their low power consumption and a compatibility with existing CMOS high-density integrated circuits, they have applications in analog low-power neural networks, memory arrays, and in various electronic circuits. In this work, a simple neuron with memristor synapses is proposed, with only one memristor for each weight utilized. The saturation linear symmetric activation function (satlins) is used for it's good approximation mapping properties. The schematic is implemented in LTSPICE and on a breadboard. A simple memristor model with activation threshold is utilized. The adder is based on two op-amps, one for inputs attached to negative weights and one for positive weights. Each synaptic weight is realized by only one memristor, suggesting a strongly reduced circuit complexity. Due to the reduced memristor operational voltage range a scaling is needed and scaling circuits are based on voltage dividers. The applied activation function is implemented with a simple circuit with a single op-amp. The memristor neuron is analyzed in LTSPICE and MATLAB. After a comparison, the derived results are verified. The offered neuron is a significant step towards engineering of complex memristor neural networks in very high-density integrated circuits.

Preventing False Activations in Autonomous Vehicles: A Memristive Associative Learning Approach with Selective Sensor Pairing

Time: Thursday 11:24 - 11:42

Keywords: Associative learning, Autonomous Vehicle, Digital circuit, Memristor, Fault tolerance

Kapil Bhardwaj (Faculty of Information Technology and Communication Sciences, Tampere University, Tampere, Finland), Dmitrii Semenov (Faculty of Electrical Engineering and Communication, Brno University of Technology), Roman Sotner (Faculty of Electrical Engineering and Communication, Brno University of Technology) and Sayani Majumdar (Faculty of Information Technology and Communication Sciences, Tampere University).

Abstract

Autonomous vehicles rely on multi-sensor fusion for accurate perception and decision-making. However, conventional sensor-based learning circuits struggle to differentiate between incomplete and valid sensor inputs, leading to erroneous activations. This paper presents a memristive associative learning circuit with selective sensor pairing and temporal validation to enhance fault tolerance in autonomous driving. Unlike existing associative learning circuits that generate outputs in untrained states with partial sensor data, the proposed design enforces a strict, electronically adjustable temporal window between sensor inputs before triggering an output. This mechanism prevents false activations from isolated or delayed signals, ensuring decisions are based on complete situational awareness. The circuit implemented using a memristor, operational amplifiers (OP-AMPs), logic gates, and latches, achieves power consumption below 300 mW, making it a low-power and efficient solution. Simulation results show that the proposed circuit reduces erroneous activations by 60%, achieving an average error rate of 0.96%, compared to 30.98% in a traditional associative learning circuit during pedestrian detection scenarios. Our finding demonstrates that selective sensor pairing, and temporal validation significantly improve the reliability and safety of autonomous vehicle navigation, particularly in challenging environments where sensor signals may be delayed or partially available.

SPECIAL SESSION 3:
ADVANCES IN MEMRISTIVE NEUROMORPHIC DEVICES AND CIRCUITS FOR ARTIFICIAL INTELLIGENCE & EDGE COMPUTING

CHAIRS: AHMET SAMIL DEMIRKOL / ALON ASCOLI

2-MOSFET Dynamic Threshold-Based Reversible & Bipolar Unbiased Inverse-Memristor Emulator

Time: Thursday 11:42 - 12:00

Keywords: Memristor, Pinched hysteresis loop, Process corner

Pushkar Srivastava (Department of Electronics Engineering Indian Institute of Technology Dhanbad Jharkhand-826004, India), Prashant Kumar (Department of Electronics Engineering Indian Institute of Technology Dhanbad Jharkhand-826004, India) and Rajeev Kumar Ranjan (Department of Electronics Engineering Indian Institute of Technology Dhanbad Jharkhand-826004, India)

Abstract

This work presents a novel DC-bias-free memristor emulation unit (MEU) with zero standby power and an inverse frequency feature. The design, based on an n-type Dynamic Threshold MOSFET (DTMOS), an n-type MOSFET, and an adjustable capacitor, enables both incremental and decremental non-volatility traits. It operates in floating and grounded conditions up to 50 MHz, with a memristance range of ≈ 206 kΩ to ≈ 33 MΩ and a CMOS layout occupying a silicon area of ≈ 62.93 μm2. The MEU demonstrates robust noise performance, process variation tolerance, and is experimentally validated using an ALD1116 MOSFET array and UA741 IC.

NDR Effects in a Locally-Active Memristor Induce Small-Signal Amplification in a Simple Cell

Time: Thursday 12:00 - 12:18

Keywords: Local Activity, Edge of Chaos, Threshold Switch, Small-Signal Amplification

Alon Ascoli (Politecnico di Torino), Emanuele Gemo (Politecnico di Torino), Fernando Corinto (Politecnico di Torino), Michele Bonnin (Politecnico di Torino), Marco Gilli (Politecnico di Torino), Pier Paolo Civalleri (Politecnico di Torino), Ahmet Samil Demirkol (TUD Dresden University of Technology), Ioannis Messaris (TUD Dresden University of Technology), Vasileios Ntinas (TUD Dresden University of Technology), Dimitrios Prousalis (TUD Dresden University of Technology), Ronald Tetzlaff (TUD Dresden University of Technology), Stefan Slesazeck (NaMLab gGmbH), Thomas Mikolajick (NaMLab / TU Dresden) and Leon Chua (University of California, Berkeley)

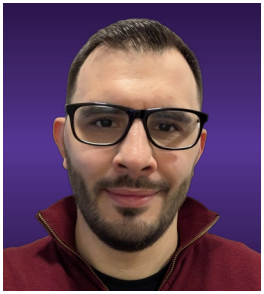
Abstract

The Pt/NbOx/Nb2O5/Pt threshold switch developed at NaMLab exhibits negative differential resistance (NDR) when biased within a specific region of its DC characteristic, achieved by placing the device in series with a suitable linear resistor. This configuration stabilizes the operating point on a branch where the slope is negative, making the device locally active and capable of acting as a source of local energy. Previous studies have harnessed this property to trigger significant dynamic behaviors in otherwise passive circuits, such as supercritical Hopf and pitchfork bifurcations—leading to the emergence of oscillations or new stable states. In contrast, this study explores how the same local energy, released near the NDR point, can amplify small-signal sine wave inputs to generate larger oscillations across the resistor than those directly induced by the input source. While this paper presents the key results from numerical simulations, the complete theoretical framework and experimental validation will be detailed in a forthcoming journal publication.

Pfunds Molkerei in Dresden is renowned for being one of the most beautiful dairy shops in the world. Steeped in history and adorned with exquisite Art Nouveau detailing, the shop features intricately hand-painted ceramics and lavish decor that create a truly immersive shopping experience. Beyond offering a wide array of premium dairy products, Pfunds Molkerei stands as a unique cultural landmark, seamlessly blending culinary tradition with artistic brilliance.

REGULAR SESSION 4: ARTIFICIAL INTELLIGENCE, MACHINE LEARNING AND THEIR APPLICATIONS

CHAIRS: VASILEIOS NTINAS



Efficient Selection of Rare Pathology Samples from Unlabeled Medical Data via Deep Active Learning

Time: Friday 10:30 - 10:48

Keywords: Artificial Intelligence, Active Learning, Medical Imaging, Class Imbalance, Computer Vision

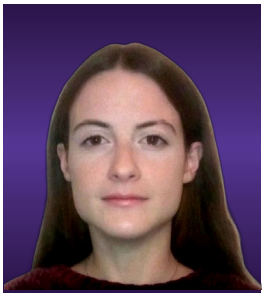
Ioannis Kafetzis (Interventional and Experimental Endoscopy, University Hospital of Wurzburg, Germany), Alexander Hann (Interventional and Experimental Endoscopy, University Hospital of Wurzburg Wurzburg, Germany) and George Fragulis (University of Western Macedonia)

Abstract

Artificial intelligence in medicine holds the potential to enhance diagnostic accuracy and efficiency, yet its progress is often limited by scarce labeled data and significant class imbalances in medical datasets. Active learning provides a promising solution by focusing annotation efforts on the most informative samples. In this work, we propose a novel active learning strategy that dynamically adjusts sample selection based on class prevalence and model prediction confidence, thereby improving representation of underrepresented classes. Experiments on X-ray datasets demonstrate that our method outperforms existing approaches, achieving higher model performance with fewer labeled samples and facilitating more efficient AI deployment in clinical environments.

REGULAR SESSION 4: ARTIFICIAL INTELLIGENCE, MACHINE LEARNING AND THEIR APPLICATIONS

CHAIRS: VASILEIOS NTINAS



Early-Stage Prediction of Electromigration Stress Using Extreme Gradient Boosting Algorithm

Time: Friday 10:48 - 11:06

Keywords: Electromigration (EM), hydrostatic stress, Power Delivery Networks, XGBoost

Eleni Tselepi (University of Thessaly), Olympia Axelou (University of Thessaly), Alberto Garcia-Ortiz (University of Bremen) and George Floros (University of Thessaly).

Abstract

As technology scales to smaller nanometer nodes, Electromigration (EM) has become one of the most significant challenges in the EDA industry. Due to the reduction of the interconnect dimensions, a preliminary assessment in early design cycles is essential to identify potential reliability risks. While established methodologies compute the transient response of EM stress, in early design cycles it is typically enough to ensure that the chip remains functional for its intended lifetime. For this purpose, in this paper, we propose a very fast EM calculation method based on XGBoost for lifetime prediction. Our approach is well-suited for early design cycle optimizations, as it relies on key features that dominantly influence stress distribution and can be extracted early in the design process. Experimental results on IBM benchmarks demonstrate that our approach achieves high accuracy, with predictions closely matching reference values. The consistently strong agreement between predicted and actual EM stress confirms the effectiveness of our method, making it a promising solution for fast and reliable early-stage EM-aware design automation.

Low Cost Platelet-Rich Plasma Facilities Creation with AI-Driven Cardiovascular Disease Assessment Using Raman Spectroscopy

Time: Friday 11:06 - 11:24

Keywords: Platelet-Rich Plasma, Low-cost, PRP, Raman, Spectroscopy, Deep Learning, Cardiovascular Diagnosis, Costeffective Healthcare

Athanasios Delis (National Technical University of Athens), Kris Koutsi (National Technical University of Athens) and Panayiotis Tsanakas (National Technical University of Athens)

Abstract

This paper presents a novel, low-cost solution for establishing a platelet-rich plasma (PRP) facility that combines affordable Raman spectroscopy with advanced machine learning techniques for automated cardiovascular disease diagnosis. By reviewing economical PRP production protocols, we show that high-quality PRP can be prepared using standard laboratory equipment at a cost of less than USD 5 per session. The integration of a low-cost Raman spectrometer, priced between USD 3,000 and USD 3,800, enables real-time analysis of PRP samples. Surface-enhanced Raman spectroscopy (SERS) data of platelets are processed using deep learning algorithms to identify subtle biomarkers indicative of cardiovascular conditions. Experimental results demonstrate that our deep learning models achieved consistent 100% test accuracy under optimal training conditions, validating the system's reliability and its strong potential for early, cost-effective clinical diagnostics. The proposed setup supports automated cardiovascular diagnosis along with other PRP-related procedures. Our preliminary results indicate that this integrated infrastructure holds significant promise for early, automated cardiovascular screening while maintaining overall low-cost operations.

REGULAR SESSION 4: ARTIFICIAL INTELLIGENCE, MACHINE LEARNING AND THEIR APPLICATIONS

CHAIRS: VASILEIOS NTINAS

PID-Controlled Active Half Car Suspension System with AI Based Shock Absorber

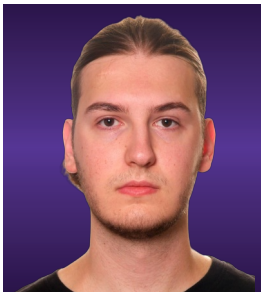
Time: Friday 11:24 - 11:42

Keywords: PID Active Control, Nonlinear Shock absorber, Half Car, Simulink

Vijay Barethiye (Veermata Jijabai Technological Institute Mumbai, India)

Abstract

Artificial intelligence (AI) is a foremost technology of the current phase in automotive industry. AI-based modeling is the key to build complex and nonlinear systems. However, developing an effective AI model is a challenging task due to the dynamic nature and variations in data. Modeling and control of automotive suspension system are highly significant from passenger comfort to road handling. In this work, efforts have been made to develop a PID-controlled active suspension system for a passive system using an AI-based shock absorber model, which describes the complex behavior of the shock absorber more effectively and precisely due to its hysteresis characteristics. Simple linear and piecewise linear models of the shock absorber cannot accurately capture vehicle performance; hence, an advanced model is required to predict vehicle responses to road disturbances. PID controller is used to suppress the vibrations generated from the road unevenness. The nonlinearity of model is contributed by using AI-based modeling of shock absorber which are located at front and rear axle of the half car model. The nonlinear hysteresis property of the shock absorber are captured by using a neural network (NN) technology. The modeling and simulation of passive and active suspension system is carried out by using simulink software for bump road perturbation. PID controller is used to decrease vertical car body displacement and achieve suitable control signal, hence it will be more comfortable conditions for passengers. The comparative analysis show that the active suspension system with PID control, exhibits a noteworthy outcomes to the passenger comfort.



Towards a Soft Robotic Glove for Physical Rehabilitation Featuring Adjustable Agonist/ Antagonist Muscle Support

Time: Friday 11:42 - 12:00

Keywords: hand rehabilitation, stroke, wearable computing, microcontroller, biomedical engineering, virtual reality, haptic feedback

Filip Ivanis (American College of Thessaloniki), Georgia Beleli (American College of Thessaloniki), Vasiliki Fiska (Aristotle University) and Alexander Astaras (American College of Thessaloniki)

Abstract

Stroke is estimated to affect about 5,500,000 people annually worldwide, with 60-80% of survivors left with unilateral weakness in their extremities. Other diseases and accidents also contribute to limited mobility and paralysis for millions of patients worldwide. This paper presents the design of a wearable glove that has capability to curl, extend and resist finger movement by providing forces similar to those produced by agonist and antagonist muscles. The aim of the device is to assist with physical rehabilitation while also providing haptic feedback to the patient. This is achieved by utilizing a pneumatic soft robotic actuation system to provide the curling force (agonistic movement) and a tendon-based pulley system to provide the opposing force (antagonistic movement). This technological choice allows for flexibility as well as gentle, soft feeling of the device, reducing the chances of injury during the rehabilitation process. The design aims to enrich existing physical rehabilitation repetitive motion training routines, utilizing haptic feedback and limiting the range of finger curling utilizing simulated tendons.

REGULAR SESSION 4: ARTIFICIAL INTELLIGENCE, MACHINE LEARNING AND THEIR APPLICATIONS

CHAIRS: VASILEIOS NTINAS

Electrical Components Detection in Images with YOLO Model Architectures using Slicing-Aided Hyper Inference.

Time: Friday 12:00 - 12:18

Keywords: Object Detection, Electronic Components Detection, YOLOv8, YOLOv11, RTMDet, SAHI

Athanasios Delis (National Technical University of Athens), Antonios Alexiadis (National Technical University of Athens) and Panayiotis Tsanakas (National Technical University of Athens)

Abstract

This study addresses the challenge of accurately identifying electronic components in images of printed circuit boards (PCBs) and circuit schematics — a task where traditional object detection methods often fall short due to limited receptive fields or insufficient feature resolution. To overcome these limitations, we propose the integration of Slicing-Aided Hyper Inference (SAHI) with state-of-the-art object detectors. SAHI partitions input images into overlapping 256×256 slices, enabling focused analysis on small, densely packed components. We trained three models — YOLOv8, YOLOv11, and RTMDet — on datasets comprising PCB and schematic images. Experimental results show that SAHI-based inference consistently improves detection performance, with higher bounding box mean Average Precision compared to full-image inference. These gains highlight the effectiveness of image slicing and result aggregation in enhancing the localization of small components. Designed for seamless integration into Mixture of Experts (MoE) frameworks and Large Language Model (LLM) assistants, these models serve as domain-specific visual modules, providing accurate component localization during inference and supporting automated circuit design workflows.

Efficient Deployment of CNN Models on multiple In-Memory Computing Units

Time: Friday 12:18 - 12:36

Keywords: Convolutional neural networks, In-memory computing, FPGAs Emulation

Eleni Bougioukou (University of Patras) and Theodore Antonakopoulos (University of Patras)

Abstract

In-Memory Computing (IMC) offers a transformative approach to deep learning acceleration by reducing data movement bottlenecks and exploiting the inherent parallelism of memory-centric computations. Efficient deployment of Convolutional Neural Networks (CNNs) on IMC-based hardware requires advanced task allocation strategies to fully harness available resources. In this work, we utilize an IMC Emulator (IMCE) equipped with multiple Processing Units (PUs) to explore the impact of CNN model deployment in a multi-processing environment on performance metrics such as processing rate and latency. To this end, we introduce the Load-Balance-Longest-Path (LBLP) algorithm, which dynamically assigns CNN computational nodes across IMCE PUs to maximize processing throughput and minimize latency through optimized resource utilization. We benchmark LBLP against alternative scheduling strategies across various CNN models, and experimental results validate the superior performance of our approach, demonstrating its effectiveness in enhancing computational efficiency in IMC systems.

REGULAR SESSION 5
NONLINEAR CIRCUITS AND SYSTEMS
CHAIRS: AHMET SAMIL DEMIRKOL / DIMITRIS PROUSALIS

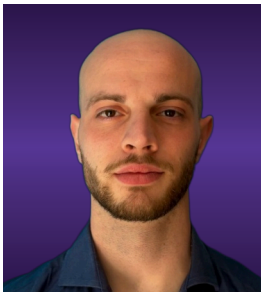
Quantitative description of the stochastic resonance in Chua circuit using the DFT of switch-phase difference distribution

Time: Friday 10:30 - 10:48

Keywords: stochastic resonance, Chua circuit, switch-phase difference, DFT, spike train

Wojciech Korneta (Univeristy of Lomza), Iacyel Silva (Industrial Engineering and Construction Dept. Universitat de les Illes Balears Palma de Mallorca, Spain), Rodrigo Picos (Industrial Engineering and Construction Dept. Universitat de les Illes Balears Palma de Mallorca, Spain) and Carol de Benito (Industrial Engineering and Construction Dept. Universitat de les Illes Balears Palma de Mallorca, Spain)

Abstract
Stochastic resonance (SR) is a phenomenon where the response of nonlinear dynamical systems to weak input signal is enhanced by the presence of noise tuned to the optimal level. Some widely used measures to quantify SR effect are the signal-to-noise ratio, the output autocorrelation function, the residence time distribution, the input-output correlation function and mutual information. Here, the SR in Chua electronic circuit operating in chaotic regime forced by unknown periodic signal and a Gaussian white noise is experimentally observed and qualitatively described by measures determined from DFT of switch-phase difference distribution. The benefits of this method are: it is simple to implement, can be used in parallel processing and requires no prior knowledge of the input periodic signal. It allows to determine the optimal noise intensity for SR and decode amplitude modulated signals encoded in voltage impulses generated by switches between chaotic attractors.



A New Analog Circuit Implementation of the Izhikevich Neuron

Time: Friday 10:48 - 11:06

Keywords: neuron dynamics, spiking behavior, circuit implementation, Izhikevich model

Lamberto Carnazza (University of Catania), Carlo Famoso (University of Catania) and Arturo Buscarino (University of Catania)

Abstract

Control systems based on neuromorphic structures are continuously gaining in the automatic control community. These structures are based on neuronal systems and their spiking behavior with the aim of exploiting intrinsic robustness and rapid information processing. The fundamental block of neuromorphic control systems is the specific neuron dynamics adopted. This choice is particularly relevant in view of practical implementations, as it must provide a suitable level of flexibility, reconfigurability, and low power consumption. In this paper, a novel analog circuit implementation of the Izhikevich neuron model is presented, bearing in mind these specifications. The proposed circuit is based on simple standard components, thus it can be implemented without adopting specific integration processes, and its behavior can be easily tuned. A complete characterization in terms of the interspike interval of the observed dynamics will also be presented.

REGULAR SESSION 5
NONLINEAR CIRCUITS AND SYSTEMS
CHAIRS: AHMET SAMIL DEMIRKOL / DIMITRIS PROUSALIS

Complex Dynamics and Implementation of Neuron Models Coupled Via Second Order Memristor

Time: Friday 11:06 - 11:24

Keywords: Second order memristor, Chaotic Dynamics, Multistability, DSP implementation

Eduardo E. Rodríguez (Instituto Potosino de Investigación Científica y Tecnologíca A.C.), Irwin A. Díaz (Instituto Potosino de Investigación Científica y Tecnologíca A.C.), José de J. Gómez (Instituto Potosino de Investigación Científica y Tecnologíca A.C.) and Juan G. Barajas (Instituto Potosino de Investigación Científica y Tecnologíca A.C.)

Abstract

We investigate a two-neuron model coupled with a second-order memristor by examining its time series, bifurcation diagram, and Lyapunov exponents. The study reveals that the coupling strength significantly influences membrane potential evolution, leading to period-doubling bifurcations and chaotic behavior. Additionally, the proposed memristive-synapse coupled system is implemented and validated using a digital signal processor platform, confirming its feasibility.

Efficient Chaotic Image Encryption with Circular Shifting and Soboleva-Modulo Map

Time: Friday 11:24 -11:42

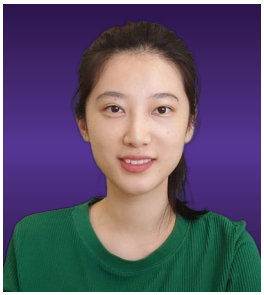
Keywords: chaos, encryption, pseudo random number generator, bit level, bit plane, Soboleva, chaotification

Lazaros Moysis (University of Western Macedonia), Marcin Lawnik (Silesian University of Technology), Wassim Alexan (German University in Cairo), Sotirios Goudos (Aristotle University of Thessaloniki), Murilo S. Baptista (University of Aberdeen) and George F. Fragulis (University of Western Macedonia)

Abstract

This work presents a chaotic image encryption algorithm that acts on the binary level of the image for effective permutation, and on the byte level for substitution. The permutation step combines actions of bit plane rearranging, and bit shuffling via circular shift operations, to reduce the execution time. For the encryption, a Soboleva hyperbolic tangent based map is used, along with a chaotic pseudo random number generator. The encryption process shows a good performance under various tests, and has also a low execution time, 0.0145s for a 256 x 256 image, and 0.0565s for a 512 x 512 image.

REGULAR SESSION 5
NONLINEAR CIRCUITS AND SYSTEMS
CHAIRS: AHMET SAMIL DEMIRKOL / DIMITRIS PROUSALIS



Spectrum: A holistic evaluation framework for nonlinear system modeling methods

Time: Friday 11:42 - 12:00

Keywords: excitation spectrum, nonlinear system, system identification, system modeling

Jinming Sun (University of Bremen) and Alberto Garcia-Ortiz (University of Bremen)

Abstract

System identification plays a crucial role in engineering and many other scientific fields, yet comparative evaluations of identification methods remain limited. Many existing approaches assess model performance primarily through one-step-ahead prediction accuracy. While convenient, this metric alone does not adequately determine whether a model truly captures the system dynamics. To address this limitation, we propose a standardized evaluation framework that incorporates the accuracy of horizon prediction. Additionally, our framework highlights the importance of sufficient excitation spectrum in training data. A model trained on data with a narrow excitation range or using identification techniques with poor generalization capabilities may struggle with new input dynamics, even if the training dataset is large. Our open-source framework offers a comprehensive training and evaluation strategy, facilitating both research advancements and practical applications in system identification.

A Generalized Attention Deficit Disorder Chaotic Model With Soboleva Hyperbolic Tangent Functions

Time: Friday 12:00 - 12:18

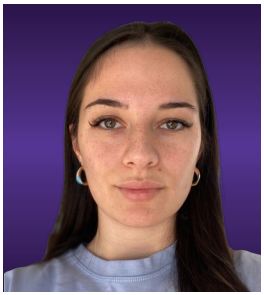
Keywords: Attention deficit disorder, chaos, Soboleva activation function, neural network

Lazaros Moysis (University of Western Macedonia), Marcin Lawnik (Silesian University of Technology), Konstantinos-Filippos Kollias (University of Western Macedonia), Christos Volos (Aristotle University of Thessaloniki), Murilo S. Baptista (University of Aberdeen), Sotirios Goudos (Aristotle University of Thessaloniki), Radoglou-Grammatikis Panagiotis (University of Western Macedonia), Evangelos Mourikis (K3Y), Panagiotis Sarigiannidis (University of Western Macedonia) and George F. Fragulis (University of Western Macedonia).

Abstract

This work investigates the modeling of Attention Deficit Disorder (ADD) using a previously established one-dimensional map, modified by replacing its two hyperbolic tangent activation functions with Soboleva hyperbolic tangent functions. This modification introduces four additional control parameters, significantly enhancing the model's flexibility and expressiveness. The impact of these new parameters is analyzed using nonlinear dynamical tools such as bifurcation diagrams, Lyapunov exponents, and phase portraits. The results reveal a strong tendency toward chaotic behavior, highlighting the model's sensitivity to external perturbations. Complex dynamical phenomena including crises, antimonotonicity, and chaotic shrimps are also observed. This enriched model provides a deeper understanding of the chaotic dynamics underlying behavioral disorders such as ADD.

REGULAR SESSION 5
NONLINEAR CIRCUITS AND SYSTEMS
CHAIRS: AHMET SAMIL DEMIRKOL / DIMITRIS PROUSALIS



A Generalized Chaotic Neural Network Model for Epilepsy Using Soboleva Hyperbolic Tangent Functions

Time: Friday 12:18 - 12:36

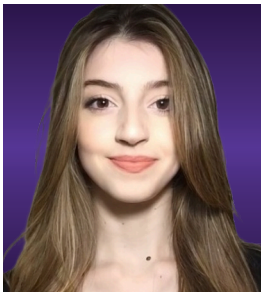
Keywords: chaos, biological systems, neural network model, epilepsy, Soboleva activation function

Alexandra Choumpaev (University of Western Macedonia), Lazaros Moysis (University of Western Macedonia), Marcin Lawnik (Silesian University of Technology) and George Fragulis (University of Western Macedonia)

Abstract

This work studies a generalized version of a chaotic neural network model for epilepsy. The model consists of several activation functions that are coupled to simulate the neuronal stimulation. The system is in a chaotic regime for normal behavior, and in a periodic regime for epilepsy. By replacing the hyperbolic tangent activation functions with the Soboleva hyperbolic tangent activation, the model is generalized through the introduction of four new control parameters for each neuron. The new model is studied through bifurcation and Lyapunov exponent diagrams, and reveals a collection of interesting dynamical phenomena. The use of the Soboleva function opens up a new direction towards the generalization of artificial neural networks for modeling neurological behaviors.

REGULAR SESSION 6
DIGITAL CIRCUITS AND SYSTEMS
CHAIRS: ALBERTO GARCIA-ORTIZ / VALERI MLADENOV



Optimizing Lightweight Cryptographic Schemes for Enhanced Security in RFID and Wireless Sensor Networks

Time: Friday 14:45 - 15:03

Keywords: lightweight cryptography, radio frequency identification (RFID), wireless sensor networks (WSNs), related key attacks, Internet of Things (IoT), hardware optimization, FPGA implementation, Hummingbird-2

George Ntakos (SCYTALE Group, Computer Engineering & Informatics Department, University of Patras), Evangelia Konstantopoulou (SCYTALE Group, Computer Engineering & Informatics Department, University of Patras) and Nicolas Sklavos (SCYTALE Group, Computer Engineering & Informatics Department, University of Patras)

Abstract

The rapid development of the Internet of Things (IoT) has integrated resource-constrained devices with demands of high speed, low power consumption, and enhanced level of security into everyday life. To address these needs, lightweight cryptographic schemes have been proposed that balance efficiency and low-area consumption, making them highly suitable for wireless sensors and Radio Frequency Identification (RFID) devices. In this paper, security-enhancing optimizations against related-key attacks are applied to ultra-lightweight cipher Hummingbird-2. Moreover, performance-driven pipelined architectures are proposed to improve the achievable throughput. The security module is implemented on a Field Programmable Gate Array (FPGA) device of the Artix-7 family, xc7a200tffg1156-3, and can operate at a maximum frequency of 385 MHz.

REGULAR SESSION 6
DIGITAL CIRCUITS AND SYSTEMS
CHAIRS: ALBERTO GARCIA-ORTIZ / VALERI MLADENOV

Periodic Online Testing for Sparse Systolic Tensor Arrays

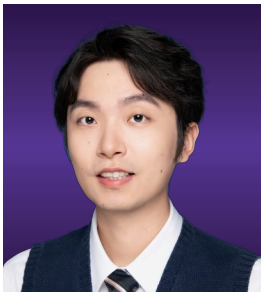
Time: Friday 15:03 - 15:21

Keywords: Error-checking, Fault-tolerance, Structured sparsity, Sparse systolic tensor array

Christodoulos Peltekis (Department of Electrical and Computer Engineering, Democritus University of Thrace), Chrysostomos Nicopoulos (Department of Electrical and Computer Engineering, University of Cyprus) and Giorgos Dimitrakopoulos (Department of Electrical and Computer Engineering, Democritus University of Thrace)

Abstract

Modern Machine Learning (ML) applications often benefit from structured sparsity, a technique that efficiently reduces model complexity and simplifies handling of sparse data in hardware. Sparse systolic tensor arrays – specifically designed to accelerate these structured-sparse ML models – play a pivotal role in enabling efficient computations. As ML is increasingly integrated into safety-critical systems, it is of paramount importance to ensure the reliability of these systems. This paper introduces an online error-checking technique capable of detecting and locating permanent faults within sparse systolic tensor arrays before computation begins. The new technique relies on merely four test vectors and exploits the weight values already loaded within the systolic array to comprehensively test the system. Fault-injection campaigns within the gate-level netlist, while executing three well-established Convolutional Neural Networks (CNN), validate the efficiency of the proposed approach, which is shown to achieve very high fault coverage, while incurring minimal performance and area overheads.



Research on the Simulation Acceleration Method of System-Level Single-Event Effects Based on Register Fault Injection

Time: Friday 15:21 - 15:39

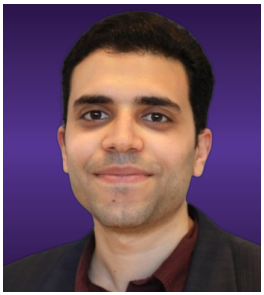
Keywords: single-event effect, aerospace integrated circuits, fault injection method

Yi Liu (Shenzhen Institute of Technology, Xidian University), Zeyu Huang (Guangzhou Institute of Technology, Xidian University), Changqing Xu (Guangzhou Institute of Technology, Xidian University), Ruijing Chen (Guangzhou Institute of Technology, Xidian University), Chenglin An (Guangzhou Institute of Technology, Xidian University), Fanquan Mu (Shenzhen Institute of Technology, Xidian University) and Xinfang Liao (Guangzhou institute of technology, Xidian University)

Abstract

With the increase in the scale of aerospace chip circuits and the complexity of circuit design, radiation-hardening technology has become more complex and difficult to evaluate. This paper adopts a system-level single-event effect simulation method based on register error injection to study the simulation acceleration methods from two dimensions: simulation scale and injection strategy. This paper studies a fault set reduction method based on stuck-at fault simulation, which reduces the fault set in terms of space and time dimensions. Secondly, it studies a multi-point fault injection simulation method based on confidence level for dynamic fault set reduction. By analyzing the error rate of registers in different simulation rounds, this method dynamically optimizes the fault set and adjusts the number of multi-point fault injections, thereby improving the simulation efficiency. This paper builds a SoC system based on the LEON2 processor to verify the proposed single-event effect simulation method. Data shows that compared with random fault injection simulation, this method can detect 51.18% more faults in the same time. Compared with full traversal fault injection simulation, this method only uses 2% of the time and can detect 95.05% of the faults. This technology can be applied to the sensitivity analysis of single-event effect in various modules of integrated circuit design, providing guidance for the optimization of radiation-hardening design of chips.

REGULAR SESSION 6
DIGITAL CIRCUITS AND SYSTEMS
CHAIRS: ALBERTO GARCIA-ORTIZ / VALERI MLADENOV



VUSA: Virtually Upscaled Systolic Array Architecture to Exploit Unstructured Sparsity in AI Acceleration

Time: Friday 15:39 - 15:57

Keywords: Systolic Array, Unstructured Sparsity, AI Acceleration, Edge AI, Computer Architecture

Shereef Helal (NXP Semiconductors), Alberto Garcia-Ortiz (University of Bremen) and Lennart Bamberg (NXP Semiconductors)

Abstract

Leveraging high degrees of unstructured sparsity is a promising approach to enhance the efficiency of deep neural network (DNN) accelerators---particularly important for emerging Edge-AI applications. We introduce VUSA, a systolic-array architecture that virtually grows based on the present sparsity to perform larger matrix multiplications with the same number of physical multiply-accumulate (MAC) units. The proposed architecture achieves saving by 37% and 68% in area and power efficiency, respectively, at the same peak-performance, compared to a baseline systolic array architecture in a commercial 16-nm technology. Still, the proposed architecture supports acceleration for any DNN with any sparsity---even no sparsity at all. Thus, the proposed architecture is application-independent, making it viable for general-purpose AI acceleration.

Quantized Semantic Segmentation for Efficient Spectrum Sensing on FPGAs

Time: Friday 16:00 - 16:15

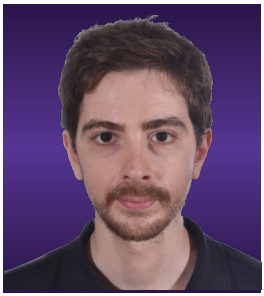
Keywords: Spectrum sensing, semantic segmentation, deep learning, quantization, FPGA, real-time

Wegdan Ali (German University in Cairo), Ahmed Kamaleldin (TUD Dresden University of Technology), Diana Goehringer (TUD Dresden University of Technology) and Mohamed Abd El Ghany (German University in Cairo, TU Darmstadt)

Abstract

Spectrum sensing is a vital component of dynamic spectrum access, enabling efficient wireless communication by accurately distinguishing between occupied and vacant spectrum bands. This paper presents a quantized semantic segmentation model tailored for spectrum sensing and optimized for real-time FPGA deployment with minimal resource utilization. The model is trained and quantized to both 16-bit and 8-bit precision, then deployed using the FINN framework to enable efficient hardware acceleration. Experimental results demonstrate that the proposed method achieves high accuracy—over 90% in controlled environments and above 70% on real-world datasets—while significantly reducing latency and hardware resource usage. These findings highlight the viability of our approach for real-time spectrum monitoring in energy-constrained and performance-critical scenarios.

REGULAR SESSION 6
DIGITAL CIRCUITS AND SYSTEMS
CHAIRS: ALBERTO GARCIA-ORTIZ / VALERI MLADENOV



Trade-offs in the Sleep Mode Management of the RP2040 Microcontroller

Time: Friday 16:15 - 16:33

Keywords: low-power, wake-up, sleep, dormant, RP2040, energy consumption

Ioannis Sofianidis (Aristotle University of Thessaloniki), Vasileios Konstantakos (Aristotle University of Thessaloniki) and Spyridon Nikolaidis (Aristotle University of Thessaloniki)

Abstract

Optimizing energy efficiency in microcontroller-based IoT systems requires strategic management of sleep modes to balance energy savings against application-specific timing constraints. This study investigates the trade-offs between sleep modes available on the RP2040 microcontroller—using either an external crystal clock or an internal ring oscillator—under varying core supply voltages (0.85–1.30 V) and operating frequencies (140–416 MHz). The crystal clock enables faster wake-up times in the sub-millisecond range but consumes higher sleep currents, whereas the ring oscillator minimizes idle power at the cost of longer wake-up delays. A key contribution of this work is the identification of a break-even time TEQ beyond which the ring oscillator's reduced sleep current compensates for its higher wake-up energy, making it more efficient for longer sleep intervals. This threshold shifts to longer durations as the supply voltage increases, while temperature variations have minimal effect. The results offer a practical framework for selecting optimal sleep strategies based on idle time and timing requirements, providing valuable insights for energy-efficient design in IoT applications with variable duty cycles, such as sensor networks and wearable devices.

SPECIAL SESSION 4
ADVANCED TECHNOLOGIES, SYSTEMS, AND APPLICATIONS FOR EXPANDING WIRELESS COMMUNICATIONS HORIZONS

CHAIRS: ACHILLES BOURSIANIS / GEORGE TSOULOS

Low-Loss GSG Bondwire Chip-to-Chip Interconnects from DC to 330 GHz

Time: Friday 14:45 - 15:03

Keywords: chip-to-chip interconnect, GSG interface, bondwire, millimeter wave, sub-THz, ultra-broadband

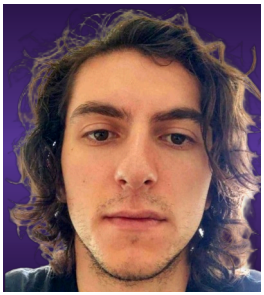
Franz Alwin Dürrwald (TUD Dresden University of Technology), Florian Protze (TUD Dresden University of Technology), Darko Cvetkovski (IHP - Leibniz-Institut für innovative Mikroelektronik), Tilo Meister (TUD Dresden University of Technology), Rolf Kraemer (Brandenburgische Technische Universität Cottbus-Senftenberg) and Frank Ellinger (TUD Dresden University of Technology)

Abstract

This research work provides a measurement-backed analysis of a single-ended chip-to-chip bondwire interface with a signal pattern of ground-signal-ground (GSG) designed for minimum insertion loss. Different approaches to reducing the bondwire length and signal disturbing factors at the intersection of two microchips (such as the scribe lines and sealrings) are investigated and compared. Reproducible, seamless measurements from DC to 330GHz have successfully demonstrated that GSG bondwire interconnects with only 3 dB insertion loss at 300 GHz can be realized without the need for tailored on-chip structures, which are typically area-intensive and can significantly limit the bandwidth and universal applicability of the chip.

SPECIAL SESSION 4
ADVANCED TECHNOLOGIES, SYSTEMS, AND APPLICATIONS FOR EXPANDING WIRELESS COMMUNICATIONS HORIZONS

CHAIRS: ACHILLES BOURSIANIS / GEORGE TSOULOS



Machine Learning-Based In-Car KPI Predictions for Cellular Networks

Time: Friday 15:03 - 15:21

Keywords: Field trials, KPI Estimation, Machine Learning

Vasileios Tsoulos (Wireless and Mobile Communications Lab, University of Peloponnese), George Tsoulos (University of Peloponnese) and Georgia Athanasiadou (University of Peloponnese)

Abstract

The swift rollout of 4G and 5G networks presents challenges in monitoring and optimizing network performance, especially in dynamic vehicular environments. Key Performance Indicators (KPIs) for coverage and quality play crucial role in assessing network performance. However, due to mobility constraints and measurement limitations, KPI data collection is often difficult or incomplete. This paper explores machine learning-based approaches to predict missing KPI values and estimate network performance at unmeasured positions inside a vehicle.

Measured data for three operators with test devices positioned at different locations within a moving vehicle were preprocessed before training four machine learning models: CatBoost, Extra Trees, LightGBM, and XGBoost. Model evaluation showed Extra Trees achieving the highest accuracy for the KPI estimation, while LightGBM demonstrated the most consistent performance across vehicle positions. Results indicated that front vehicle positions exhibit stronger but more variable signals, while back positions provide more stable yet weaker signals. The analysis highlights the importance of position-aware AI models for network optimization in vehicular settings.

ML methods for SNR Prediction in Vehicular Communications

Time: Friday 15:21 - 15:39

Keywords: Vehicular communications, ITS, V2I, SNR, machine learning.

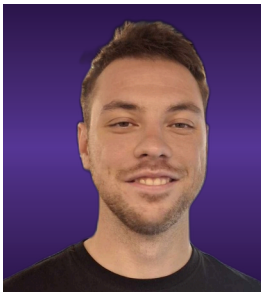
Vasileios Rekkas (School of Physics, Aristotle University of Thessaloniki), Achilles Boursianis (School of Physics, Aristotle University of Thessaloniki), Maria Papadopoulou (International Hellenic University), Thomas Lagkas (Democritus University of Thrace), Panagiotis Sarigiannidis (University of Western Macedonia) and Sotirios Goudos (Aristotle University of Thessaloniki)

Abstract

Vehicular communication technology forms the backbone of Intelligent Transportation Systems (ITS), enabling seamless data exchange between vehicles (V2V) and between vehicles and infrastructure (V2I). This communication paradigm is pivotal for improving traffic flow, enhancing road safety, and optimizing vehicle operations—driving the evolution of modern transportation systems. The success of ITS depends on a high-speed, low-latency communication framework capable of reliably transmitting critical vehicular and environmental data in real time, thereby supporting adaptive and resilient network performance. This research presents a comprehensive analysis of various machine learning (ML) techniques to develop predictive models for estimating the Signal-to-Noise Ratio (SNR) in V2I communication networks, with the goal of improving network reliability and performance.

SPECIAL SESSION 4
ADVANCED TECHNOLOGIES, SYSTEMS, AND APPLICATIONS FOR EXPANDING WIRELESS COMMUNICATIONS HORIZONS

CHAIRS: ACHILLES BOURSIANIS / GEORGE TSOULOS



Two-layered Ultra-Wideband and High Gain Metamaterial Antenna for 5G Ka-Band Applications Using the Mountain Gazelle Optimizer

Time: Friday 15:39 - 15:57

Keywords: 5G, Antennas, Optimization methods, Metasurfaces, Evolutionary Algorithms

Georgios Korompilis (Aristotle University of Thessaloniki), Hlias Tzouras (University of Patras), Achilles Boursianis (Aristotle University of Thessaloniki), Panagiotis Sarigiannidis (University of Western Macedonia), Stavros Koulouridis (University of Patras) and Sotirios Goudos (Aristotle University of Thessaloniki)

Abstract

As the demand for high-speed telecommunications continues to grow, systems operating at higher frequencies are increasingly being introduced. In this paper, we propose a high-gain, ultra-wideband two-layer 5G antenna operating in the Ka-Band, covering a 10 GHz bandwidth from 32 to 43 GHz. The metamaterial-based antenna design consists of two substrates separated by an air gap and features a radiating structure composed of a large central patch surrounded by an array of smaller patches. The final antenna configuration is the outcome of an optimization process aimed at achieving ultra-wideband performance while preserving high gain within the 5G Ka-Band. The Mountain Gazelle optimization algorithm was employed due to its strong performance in recent studies, which is further validated by the results of this work—demonstrating stable operation across the full 32–43 GHz range with consistently high gain.

Non-Volatile Memristor as a Backscattering Circuit Element: High-Frequency Analysis and Preliminary Theoretical Considerations

Time: Friday 16:00 - 16:15

Keywords: non-volatile memristor, high-frequency circuits, backscattering systems, AWR circuit simulation tool, SPICE model

Riccardo Colella (National Research Council), Alon Ascoli (Politecnico di Torino), Fernando Corinto (Politecnico di Torino) and Giuseppe Grassi (University of Salento)

Abstract

This paper examines the frequency-domain response of memristors under high-frequency excitation, assessing their potential for backscattering applications. The study aims to characterize the impact of RF signals on memristor behavior and establish theoretical considerations for their feasibility as backscattering elements. The analysis considers variations in both the amplitude and frequency of the applied signal. SPICE simulations of the memristor model in AWR are performed to analyze these effects in the frequency domain. Results indicate that amplitudes exceeding the activation threshold significantly alter the memristor state, primarily during the transient phase. Conversely, at a fixed amplitude above the activation threshold, different frequencies perturb the state and its mean value. Based on the simulation indications, theoretical considerations are derived to verify the dependence of the memristor state on the angular frequency ω.

River Elbe with the ensemble of the Elbe castles in the background.

POSTER SESSION

Low-Cost Versatile Power Management Unit for 6G Heterogeneous Phased Array Systems

Time: Wednesday 14:45 - 16:00

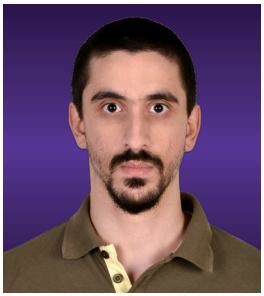
Keywords: Heterogeneous Circuit Systems, GaN Power Amplifier Protection, Phased Arrays, Power Management Unit (PMU)

Lukas Hüssen (Chair of High Frequency Electronics, RWTH Aachen University), Jonas Winkelhake (Chair of High Frequency Electronics, RWTH Aachen University), Muh-Dey Wei (Chair of High Frequency Electronics, RWTH Aachen University), Renato Negra (Chair of High Frequency Electronics, RWTH Aachen University)

Abstract

Many DC supply and bias voltages are needed in heterogeneous phased array systems, due to the high component count. We present a low-cost versatile power management unit for the supply of such a system. From a single DC input voltage it generates six fixed voltage levels, four adjustable low-voltage bias voltages, two adjustable negative bias voltages, and two adjustable high-voltage outputs. The adjustable voltages are controllable via SPI communication, for which a Teensy microcontroller was used in combination with Matlab to create a simple to use graphical user interface. Furthermore, to cater to the needs of gallium nitride (GaN) power amplifiers, a protection circuit is added to ensure that the high-voltage outputs can only be switched on as long as a negative bias output is present.

POSTER SESSION



Artificial Intelligence Based Bandgap Voltage Reference Design

Time: Wednesday 14:45 - 16:00

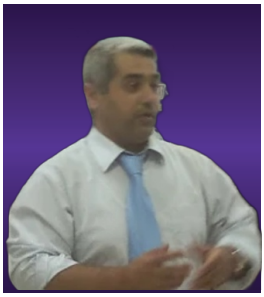
Keywords: Artificial Intelligence, Simulated Annealing, Dual Annealing, Nelder-Mead, Bandgap Reference

Savvas Karipidis (Aristotle University of Thessaloniki), Andi Buzo (Infineon Technologies AG), Georg Pelz (Infineon Technologies AG) and Thomas Noulis (Aristotle University of Thessaloniki)

Abstract

In this work, artificial intelligence algorithms are applied to the problem of minimizing the temperature coefficient of a bandgap reference voltage. To improve efficiency, the optimization process is divided into two stages. In the first stage, the dual annealing algorithm is used to determine the optimal operating point of the transistors. This algorithm is particularly suitable for navigating ill-defined integer surfaces, which justifies its selection. The output of this stage serves as the starting point for the second algorithm, where the optimization surface is better conditioned. The Nelder-Mead method is then employed to further refine the solution and reach the minimum. The entire process requires only a few hundred function evaluations, making it both fast and efficient, ultimately achieving a temperature coefficient of 30 ppm.

POSTER SESSION



A Hybrid Hashing for Securing Data of Water Distribution System

Time: Wednesday 14:45 - 16:00

Keywords: Blockchain, Decision Support Systems, Security, Water Distribution System

Aida Ataiwi (Jordan University of Science and Technology - Jordan) and Abdoul Rjoub (Jordan University of Science and Technology - Jordan)

Abstract

With the increasing demand for clean and drinkable water, it is imperative to to integrate advanced and cutting-edge technologies such as blockchain, IoT, Decision Support Systems (DSS), and Artificial Intelligence (AI) in water harvesting systems. A distributed systems data recording system was created to maintain water quality from treatment plants to customers. This paper propose the use of a hybrid cryptographic hash in the Blockchain process, using chemical rainfall statistics from the UK from 1986 to 2011. The Triple Data Encryption Algorithm (TDES) was used to encrypt data, while the Water Quality Index (WQI) was used to assess rainfall quality. The experiment showed that encryption improved data security and quality, enhancing overall system performance.

POSTER SESSION

Development of a Self-Powered AC-DC Conversion Circuit for Harvesting Energy From a Multilayer Piezoelectric Module

Time: Wednesday 14:45 - 16:00

Keywords: energy harvesting, wearable devices, piezoelectric generator, bridge rectifier, synchronous DC-DC converter, PWM, voltage control

Ivaylo Pandiev (Technical University of Sofia), Nikolay Kurtev (Technical University of Sofia) and Mariya Aleksandrova (Technical University of Sofia)

Abstract

This paper presents the structure and operational principle of a prototype of a micropower AC-DC conversion circuit for wearable battery-free power supply devices. The proposed circuit configuration is intended to use a multilayer rectangular piezoelectric module as a source of electrical energy, which converts spontaneous mechanical vibrations into piezo¬electric voltage. The electrical energy produced after conversion with a bridge rectifier is used to charge two series-connected low-power supercapacitors with a maximum voltage of up to 15V, used as energy storage elements. For the proposed circuit configuration, a synchronous step-down DC-DC conve¬rter with discrete components is implemented. The power control system is realized with a non-inverting error amplifier and a passive compensator. As a result of the operation of the amplifier with the negative feedback, an output voltage of 1.2V and a maximum output power of 2.4mW is established. The coefficient of overall energy efficiency achieved up to 82% at a power dissipation not greater than 20 W. To verify the efficiency of the proposed prototype of an AC-DC conversion circuit, a printed circuit board is designed and implemented on standard FR-4 material and on a flexible substrate.

POSTER SESSION

Development of Self-Powered SSHI Interface Circuits Integrated with Low-Power Monolithic AC-DC converters for Piezoelectric Energy Harvesting

Time: Wednesday 14:45 - 16:00

Keywords: energy harvesting, piezoelectric generator, brid¬ge rectifier, series-SSHI, parallel-SSHI, circuit testing, electronic converters

Nikolay Kurtev (Technical University of Sofia) and Ivaylo Pandiev (Technical University of Sofia)

Abstract

Piezoelectric energy harvesting has emerged as a viable solution for powering low-power electronic devices by converting ambient vibrations into electrical energy. However, conventional energy extraction circuits, such as the LT3588-1 IC, use a simple full-bridge rectifier (FBR) as a first stage, limiting the harvesting efficiency. This study investigates alternative interface circuits designed to improve the energy extraction capabilities of the LT3588-1 over a piezoelectric generator. Two discrete-component-based interface circuits are proposed and investigated through LTSpice. Both circuits are based on the Synchronized Switch Harvesting on Inductor (SSHI) technique. The simulation results indicate that the proposed circuits enhance the power extraction efficiency compared to the conventional LT3588-1 configuration by up to 20% at 60Hz vibration frequency, which permits the supply of more power to the load under the simulation conditions.

POSTER SESSION

Novel Environmental Electric Field Measurement Using A Drone

Time: Wednesday 14:45 - 16:00

Keywords: drone, environmental electric field, electric field sensor, overhead line, wireless sensing

Kun-Long Chen (National Taiwan University of Science and Technology) and Hong-Shuo Chen (National Taiwan Ocean University)

Abstract

This study proposes a new environmental electric field measurement technology based on a drone for the working environment adjacent to high-voltage overhead lines. A single-axis electric field sensor designed with a parallel capacitive plate structure can be used to measure the electric field value and its frequency around the measured overhead line. In order to ensure that the drone can maintain a safe distance from the measured overhead line, a laser distance sensor is installed on the drone. In addition, this measured distance can be used to mark the relative positional relationship between the overhead line and the measured electric field distribution. All sensing data will be acquired and processed by the embedded system on the drone. Finally, the processed sensing data will be wirelessly transmitted to the remote environmental electric-field monitoring platform via ZigBee for real-time display and storage.

POSTER SESSION

A Brushless DC Motor Driver Chip with Internal Bridge Driver

Time: Wednesday 14:45 - 16:00

Keywords: brushless DC motor, motor driver, bridge driver, gate driver, electronic commutation, charge

Yifeng Peng (Zhejiang University), Ao Li (Zhejiang University), Jianxiong Xi (Zhejiang University), Lenian He (Zhejiang University), Anming Gao (Zhejiang Starshine Semiconductor Corporation) and Wei Jiang (Zhejiang Starshine Semiconductor Corporation)

Abstract

This paper proposes a brushless DC (BLDC) motor driver chip with internal bridge driver. The performance of BLDC motor is determined by the performance of bridge driver. So Laterally Diffused Metal Oxide Semiconductor (LDMOS) is adopted as power transistors of bridge driver, which can withstand high voltage and current with low on-resistance. To ensure the consistency of high-side and low-side delay in bridge driver, a high-side gate driver with low delay is used. In addition, the chip has internal motor controller used for electronic commutation and dead time insertion of bridge driver. A charge pump is integrated for supplying power to high-side gate driver. The chip is designed and verified by using a 180nm SOI BCD Technology. It has 5A output current capability and 60V maximum operating voltage, having good driving capability.

POSTER SESSION

Novel Control Technique For Single Inductor Multiple Output Converters Operating with Fast Response and Reduced Cross-Regulation

Time: Wednesday 14:45 - 16:00

Keywords: SIMO, fast response, low cross regulation

Linxin Jiang (jianglinxin@zju.edu.cn), Lenian He (Zhejiang University), Jianxiong Xi (Zhejiang University), Zhongbo Han (Zhejiang University), Tao Wang (Zhejiang University), Anming Gao (Zhejiang Starshine Semiconductor Corporation) and Wei Jiang (Zhejiang Starshine Semiconductor Corporation)

Abstract

This paper proposes a Single-Inductor Multiple Output (SIMO) DC-DC converter based on a hybrid topology, which effectively enhances the system's transient response speed and reduces the cross-regulation between channels through an innovative control strategy. The proposed converter combines charge control mode with valley current adaptive conduction time control mode. It cascades Low Dropout Regulators (LDOs) with high Power Supply Rejection Ratio (PSRR) to suppress inter-channel cross-regulation. Meanwhile, the adaptive conduction time control mode improves the dynamic performance of the converter across a wide load range. The proposed converter is verified using the 250nm BCD process, achieving a peak efficiency of 93.5%.

POSTER SESSION

Design of a Non-Reciprocal Bandpass Filter Using Varactor based Spatio-Temporal Modulation in the UHF Band

Time: Wednesday 14:45 - 16:00

Keywords: Nonreciprocal, Spatio-Temporal Modulation, isolator, Varactor, intermodulation product

Suhail Afroz Mohammad (Dept. of ECE National Institute of Technology Warangal), Arun Kumar Gande (Dept. of ECE National Institute of Technology Warangal), David Chatzichristodoulou (Frederick Research Center and RF and microwave solutions LTD), Symeon Nikolaou (Frederick Research Center andDept. of ECE Frederick University), Photos Vryonides (Frederick Research Center and Dept. of ECE Frederick University) and Gopi Ram (Dept. of ECE National Institute of Technology Warangal)

Abstract

This paper presents the design of a three-pole lumped-element nonreciprocal band-pass filter (NR-BPF) oper- ating at 850 MHz. The filter, based on the principle of spatio-temporal modulation (STM), enables signal propagation in a single direction, effectively integrating the functions of an isolator and a band-pass filter into one device. Termed an 'isolating filter' it features a series of temporally modulated coupled resonators. The circuit's time-varying components generate intermodulation (IM) products, and by carefully selecting the modulation frequency (fm), modulation depth (ζ), and phase delay ( ), the signal power at the IM frequencies is constructively converted back to the RF frequency in the forward direction, forming a low-loss passband. Conversely, destructive interference in the reverse direction achieves isolation. For verifying the proposed design topology, we have designed, fabricated and measured a lumped-element filter demonstrating a forward insertion loss of 3.2 dB, high reverse isolation of 28 dB, and matching better than 20 dB at both ports. Such nonreciprocal filters have potential applications in wideband simultaneous transmit-and-receive radio front-end systems.

POSTER SESSION

High Gain Lens-Loaded Circularly Polarized Antennas for RF Jamming Applications

Time: Wednesday 14:45 - 16:00

Keywords: UAV Unmanned aerial vehicle, AR axial ratio, CP circular polarized

David Chatzichristodoulou (RF and Microwave Solutions and Fredeick Research Center), Photos Vryonides (Frederick Research Center, Frederick University, Dept. Electrical Computer Engineering and Informatics), Dimitris Mintis (NovaMechanics Ltd.), Christos Anastasiou (NovaMechanics Ltd), Antreas Afantitis (NovaMechanics Ltd) and Symeon Nikolaou (Frederick Research Center, Frederick University, Dept. Electrical Computer Engineering and Informatics)

Abstract

Two antenna designs for high gain RF jammer front-end are presented. The first design is an elliptical patch antenna combined with a 7-rings graded index planar lens. The second design is a 2x2 array of elliptical patches combined with a 9-rings graded index planar lens. Both lens are additively manufactured using a multi-filament printer and the different εr combinations are achieved using a similar dielectric constant Zetamix filament with a calculated infill percentage. The resulted dielectric index is an average value between the base material εr and the εr of the air. The lens-loaded antennas result in 16.6 dBi gain for the single element and 20.6 dBi gain for the 2x2 array. An offset feed point on the patches ensures circular polarization in the entire 5.725–5.850 GHz frequency band, and in addition 20o beam tilting is demonstrated by shifting the center of the disc-shaped planar lens accordingly.

POSTER SESSION

Acoustic Size Estimation of Pipeline Leakages Using k-Nearest Neighbors Algorithm

Time: Wednesday 14:45 - 16:00

Keywords: Metallic pipelines, Leakage size estimation, Vibroacoustic signals, Machine learning, k-Nearest Neighbors

Georgios-Panagiotis Kousiopoulos (Aristotle University of Thessaloniki) and Spyridon Nikolaidis (Aristotle University of Thessaloniki)

Abstract

A common problem in the operation of pipeline networks is the appearance of leaks. In order to protect a pipeline from leakages proper monitoring systems, able to timely detect and localize a leak, can be installed. A variety of methods regarding these matters already exists in the literature. However, the research concerning the estimation of the leak size, which is also crucial for the protection of a pipeline, is quite limited. The present paper aims to contribute to this field. Specifically, a novel leak diameter estimation method is presented, which uses vibroacoustic signals obtained by an accelerometer mounted externally on the pipeline. The method relies on machine learning, namely on the k-Nearest Neighbors (kNN) regression technique. The leak signals are separated into two groups: the first one is used for training and the second one for testing the model. Four different spectral descriptors (i.e. entropy, flatness, skewness and decrease) along with the RMS are employed for the kNN technique, thus forming a 5-dimensional feature space. The metric used in this space is the Euclidean distance between the training points and a certain test point. The output of the model is the leak diameter, which is calculated by averaging the leak diameter values corresponding to the k training points closest to the test point under consideration. The proposed method was tested under different noise levels and was found to provide efficient success rates, ranging between 85.7% and 100%.

POSTER SESSION

Design and Development of a Low-Cost Circuit for Soil Electrical Conductivity Measurement Using the Wenner Array Method

Time: Wednesday 14:45 - 16:00

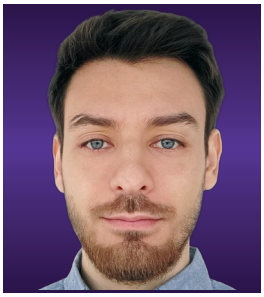
Keywords: Soil Electrical Conductivity, Wenner Array, Low-Cost Sensor, Precision Agriculture, Electronic Circuit

Vasileios D. Koufogeorgos (Department of Information and Electronic Systems Engineering - International Hellenic University), Argyrios T. Hatzopoulos (Department of Information and Electronic Systems Engineering - International Hellenic University), Kyriakos Tsiakmakis (Department of Information and Electronic Systems Engineering - International Hellenic University), Vassilis Vassios (International Hellenic University-Department of Information and Electronic Systems), Maria Papadopoulou (International Hellenic University) and Dimitrios K. Papakostas (International Hellenic University-Department of Information and Electronic Systems).

Abstract

Soil electrical conductivity (EC) is a key parameter for assessing soil salinity and soil health. This study presents the design and development of a low-cost, easy-to-use soil EC sensor based on the Wenner array method. While the traditional method uses bipolar pulse currents, the proposed circuit employs a sinusoidal signal that simplifies the design while maintaining measurement accuracy. The system consists of four galvanized electrodes, a function generator, a voltage-to-current converter and differential amplifiers for current and voltage measurements. Experimental validation was conducted on different soil types under varying moisture conditions, comparing results with a LCR meter and a commercial soil conductivity meter. The proposed circuit provides reliable and rapid measurements, suitable for precision agriculture and environmental monitoring. The simulation results confirm the circuit's accuracy and practical applicability.

POSTER SESSION



Towards the design of a Real-Time processing System for Forcecardiography Signals

Time: Wednesday 14:45 - 16:00

Keywords: forcecardiography (FCG), seismocardiography (SCG), electrocardiography (ECG), hardware implementation, real-time, FPGA, System on Chip

Efstratios Zacharelos (University of Salerno), Emilio Andreozzi (University of Napoli Federico II), Daniele Esposito (University of Salerno), Martino Giaquinto (University of Salerno) and Ettore Napoli (University of Salerno)

Abstract

Forcecardiography (FCG) is a novel technique for the non-invasive acquisition of cardiac and respiratory induced chest wall vibrations that has been recently proposed and demonstrated using innovative, non-invasive force sensors. FCG sensors capture additional infrasonic and audible vibrations that are not captured by other cardio-mechanical monitoring techniques like seismocardiography (SCG), thus offering richer informational content. However, the extraction of relevant vibrational components from FCG data requires dedicated processing that has been proposed and only demonstrated with off-line processing. This paper analyses the design trade-offs for the implementation of a compact processing system for the real-time extraction and wireless transmission of FCG components, which could enable home-care and telemedicine applications. The design target is an ARM/FPGA SoC board for acquiring, processing, and wireless transmission of the processed data. Preliminary results indicate that efficiently extracting various frequency bands in real time with a latency of less than 200 ms is feasible.

POSTER SESSION

Traffic Sign Recognition for Level-3 Autonomy: Efficient Deep Learning for Class-Imbalanced Datasets

Time: Wednesday 14:45 - 16:00

Keywords: Efficient deep Learning, Ensemble Learning, Level-3 autonomy

Myrsini Eleni Mita (Aristotle University of Thessaloniki), Lazaros Alexios Iliadis (Aristotle University of Thessaloniki), Sotirios Sotiroudis (Aristotle University of Thessaloniki), Achilles Boursianis (Aristotle University of Thessaloniki), Maria Papadopoulou (International Hellenic University) and Sotirios Goudos (Aristotle University of Thessaloniki)

Abstract

Autonomous driving is one of the technologies that will transform future transportation. However, fully autonomous vehicles are still far from being commercially deployed. Level-3 autonomy is a more realistic task but requires robust and accurate systems for interpreting road environments. Traffic sign recognition (TSR) is essential for improving safety and adherence to traffic laws by enabling cars to make educated decisions. The reliability of traditional TSR techniques is limited by their frequent struggles with partial occlusion, complicated backgrounds, and illumination fluctuations. This study employs efficient deep learning (DL) techniques to tackle these challenges, utilizing methodologies suitable for class-imbalanced datasets. An ensemble of two state-of-the-art lightweight models and a novel convolutional neural network (CNN) architecture is tested on the German Traffic Sign Recognition Benchmark (GTSRB) dataset. The proposed approach achieves 97.86 % accuracy with little computational cost, making it a suitable candidate for level-3 autonomous vehicles.

POSTER SESSION

LTSpice Based Stability Analysis of Boost Synchnronous DC-DC Converter

Time: Wednesday 14:45 - 16:00

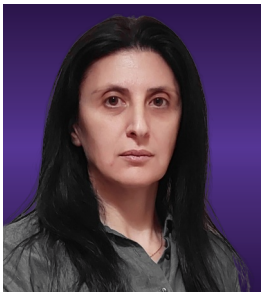
Keywords: DC-DC converters, energy efficiency, stability analysis, tolerance analysis

Gergana Vacheva (Technical University of Sofia), Plamen Stanchev (Technical University of Sofia) and Nikolay Hinov (Technical University of Sofia)

Abstract

This report presents a stability analysis of a synchronous boost DC-DC converter, performed using LTSpice – a software platform for simulation of analog electronic circuits. The purpose of the study is to evaluate the behavior and stability of the converter in different operating modes, by analyzing the frequency response of the feedback. The amplitude and phase margins, which serve as the main indicators of the stability of the system, were calculated using AC analysis. The report examines the influence of the regulator parameters, filtering components and load conditions on the dynamic response of the circuit. The presented simulation results demonstrate the importance of precise design of the regulator loop and confirm the effectiveness of LTSpice as a tool for preliminary verification and optimization of power systems. The analysis supports a better understanding of the principles of stable operation of DC-DC converters, which is essential for the modern electronics industry.

POSTER SESSION



Novel Periodic Structure Design Using African Vultures Optimization Algorithm for Smart Electromagnetic Environments

Time: Wednesday 14:45 - 16:00

Keywords: Frequency selective surface, periodic structure, unit cell, African Vultures optimization algorithm, smart electromagnetic surface

Pavlos Keramaris (Aristotle University of Thessaloniki), Maria Papadopoulou (International Hellenic University), Panagiotis Sarigiannidis (University of Western Macedonia), Theodoros Samaras (Aristotle University of Thessaloniki), Sotirios Goudos (Aristotle University of Thessaloniki) and Achilles Boursianis (Aristotle University of Thessaloniki)

Abstract

Frequency selective surfaces have been utilized in smart electromagnetic environments due to their diverse range of applications. The geometric configuration of these periodic structures can enable them to be used for reflectivity, absorption, or transmission of electromagnetic waves. In this work, we exploit their reflectivity in the Wi-Fi frequency bands (2.4 GHz, 5 GHz, and 6 GHz) and transmission in 5G NR FR1 n78, 3.3 – 3.8 GHz. A novel nature-inspired metaheuristic algorithm, i.e., the African Vultures optimization algorithm, has been assessed and exhibited satisfactory results in unimodal and multimodal functions. As a result, it is utilized as a promising candidate to optimize the geometry of the proposed surface. Numerical results demonstrate the effectiveness of the proposed approach in enhancing electromagnetic performance, validating its potential for real-world applications.

POSTER SESSION

Hardware-Accelerated Mode-Switching Polymorphic Encryption for Privacy Preserving Machine Learning

Time: Wednesday 14:45 - 16:00

Keywords: FPGA acceleration, polymorphic encryption, privacy-preserving machine learning, decision tree, hardware security

Rawan Hagag (German University in Cairo), Hassan Nassar (KIT), Jörg Henkel (KIT) and Mohamed Abd El Ghany (German University in Cairo)

Abstract

This paper presents a hardware-accelerated polymorphic encryption framework for privacy-preserving machine learning. The approach employs a mode-switching polymorphic encryption scheme, enabling secure data processing without decryption. We prototype a hardware-accelerated decision tree classifier that efficiently traverses encrypted data stored in FPGA BRAM, ensuring low-latency inference. Experimental results demonstrate the impact of encryption on classification accuracy and computational efficiency, providing a scalable solution for secure outsourced machine learning training.

POSTER SESSION

Towards digital horticulture with low-cost sensors

Time: Wednesday 14:45 - 16:00

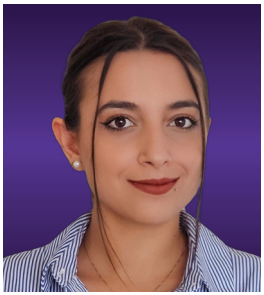
Keywords: precision agriculture, wireless sensors, cloud services, computer-aided decision support system

Theodoros Samaras (Aristotle University of Thessaloniki) and Athanasios Koukounaras (Aristotle University of Thessaloniki)

Abstract

Digital horticulture is the integration of digital technologies into horticultural practices to optimize production, improve efficiency, and promote sustainability. In this work we provide guidance on how to build a user-friendly and low-cost digital horticulture system with off-the-shelf components aimed at operating inside a greenhouse.

POSTER SESSION



Real-Time FPGA-Based Strain Monitoring System

Time: Wednesday 14:45 - 16:00

Keywords: FPGA technology, Strain monitoring, Real-time data acquisition, Structural health monitoring, Signal processing, Autonomous systems, Data visualization, Structural analysis

Evangelia-Agni Alexopoulou (University of West Attica, Department of Electrical and Electronics Engineering, Greece), Ermioni D. Pasiou (National Technical University of Athens, Department of Mechanics, Greece), Ilias Daradimos (University of West Attica, Department of Electrical and Electronics Engineering, Greece), Ilias Stavrakas (University of West Attica, Department of Electrical and Electronics Engineering, Greece) and Efstathios D. Kyriakis-Bitzaros (University of West Attica, Department of Electrical and Electronics Engineering, Greece)

Abstract

An FPGA-based strain monitoring system for real-time data acquisition and visualization in structural health monitoring is presented in this paper. The system supports serial communication for MATLAB-based analysis and independent onboard visualization by integrating the MAX10 FPGA, KYOWA strain gauges, and a custom signal conditioning unit. Experiments with different loading scenarios showed excellent accuracy and dependability. The suggested system demonstrates the potential of FPGA technology for real-time structural analysis while providing a scalable and affordable solution.

POSTER SESSION

Integrated IoT and AI-Driven Smart Refrigerator System

Time: Wednesday 14:45 - 16:00

Keywords: Smart refrigerator, machine learning, embedded system, linear regression, LSTM, IoT

Dimitrios Toliopoulos (International Hellenic University), Efthimios Demkas (International Hellenic University), Argyrios T. Hatzopoulos (Department of Information and Electronic Systems Engineering - International Hellenic University), Kyriakos Tsiakmakis (International Hellenic University), Achilles Boursianis (Aristotle University of Thessaloniki), Spyridon Nikolaidis (Aristotle University of Thessaloniki), Sotirios Goudos (Aristotle University of Thessaloniki) and Maria Papadopoulou (International Hellenic University)

Abstract

In addition to the considerable economic costs, inefficient electricity usage significantly contributes to environmental pollution. To tackle this issue, we developed an IoT system utilizing various electronic devices, including an ESP8266 microcontroller, a temperature-humidity sensor, an electromechanical switch, a power metering for appliance control, and a Raspberry Pi 4. This system records and stores data on temperature, humidity, door openings, and power consumption. By leveraging the open-source Home Assistant platform, we successfully synchronized these components to achieve our desired outcomes. Using machine learning techniques, such as Long Short-Term Memory (LSTM), we can predict power consumption based on temperature and humidity. We also employed the Linear Regression method to correlate temperature differences with the duration of refrigerator door openings. Finally, we applied the Anomaly Detection and Isolation Forest model to identify significant variations in temperature and humidity when the door is not in use.

POSTER SESSION

Low-Power and Rail-to-Rail StrongARM DL-Latch Comparator: Design, Analysis and Performance Evaluation

Time: Wednesday 14:45 - 16:00

Keywords: SOI-BCD technology, MOSFET, Low-power, Comparator, StrongARM, ADC, DAC

Nandakishor Yadav (Fraunhofer Institute for Photonic Microsystems IPMS Dresden), Konstantinos Efstathios Falidas (Fraunhofer Institute for Photonic Microsystems IPMS Dresden), David Lehninger (Fraunhofer Institute for Photonic Microsystems IPMS Dresden), Konrad Seidel (Fraunhofer Institute for Photonic Microsystems IPMS Dresden) and Thomas Kämpfe (Fraunhofer Institute for Photonic Microsystems IPMS Dresden).

Abstract

In this paper, a low-power and rail-to-rail StrongARM comparator is proposed. A novel preamplifier stage which supports rail-to-rail common-mode input voltage (CMIV) is added to the conventional StrongARM. Furthermore, the proposed preamplifier also saves static power by using the existing clock gating and power gating from conventional StrongARM comparator. It saves 63.3% more power than state-of-the-art design. The resolution of the comparator is below 10µV and the CMIV varies from 0V to VDD. The design is scalable and ready to be used in data converters.

POSTER SESSION

Specification of generic Memristor-based Crossbar Architectures for In-Memory Computing

Time: Wednesday 14:45 - 16:00

Keywords: Specification of generic Memristor-based Crossbar Architectures for In-Memory Computing.

Benjamin Seiler (Friedrich-Alexander-University Erlangen-Nürnberg) and Dietmar Fey (Friedrich-Alexander-University Erlangen-Nürnberg)

Abstract

Processing data where it resides, as envisioned by in-memory computing concepts, is expected to be the next step after multi-core and heterogeneous architectures consisting of CPU and accelerators to counteract the energy wall. The use of memristors offers low read energy and non-volatility of the data when accessing the memory. This helps energy- and computing performance hungry embedded functions for artificial intelligence and machine learning. In addition, memristive devices enable the integration of storage and processing functions in close proximity to significantly reduce the energy required to transport data. Prototypes of this concept with memristors have already been built and tested. To simplify the design and simulation of memristive IMC architectures, mixed-signal or generally mixed-abstraction simulations would be ideal, which simultaneously combine digital architecture elements with analogue components, e.g. memristive matrix-vector accelerators. This requires new simulation environments that enable fast simulation times and a flexible design process. To move forward in this direction, we present our SystemC-based solution for the design and simulation of memristive crossbar architectures and demonstrate and evaluate its usefulness for selected neuromorphic architectures.

POSTER SESSION

Reflecting Intelligent Swarm Cloud for Near Field Wireless Communications

Time: Wednesday 14:45 - 16:00

Keywords: Unmanned Aerial Vehicles, Reflecting Intelligent Surfaces, Multiple Input Multiple Output, Base Station

Theodoros Kaifas (Democritus University of Thrace), Dimitrios Babas (Aristotle University of Thessaloniki), Achilles Boursianis (Aristotle University of Thessaloniki) and John Sahalos (Aristotle University of Thessaloniki)

Abstract

In this paper, the scenario of an Unmanned Aerial Vehicle Swarm armed with one reflecting intelligent surface per UAV is presented. The swarm is to be integrated, as a flying–movable distributed, sizable passive / reflecting inexpensive relay, into the underlaying 5G/6G wireless communication system. The communication scenario focuses on near-field communications assuming a MIMO base station and many single antenna mobile users that experience unreliable communication links due to shadowing. The reflecting swarm – cloud, is demonstrated that has the potential not only to restore link reliability but also to jointly minimize the transmit power and increase the sum rate of the system. This is achieved by exploiting the equivalent swarm UAV distributed–general array antenna and maximizing its directive gain to the desired mobile user, minimizing at the same time the directive gain to the interferers.

POSTER SESSION

Edge of chaos kernel in CellNN model of FitzHugh Nagumo system

Time: Wednesday 14:45 - 16:00

Keywords: cellular nonlinear network model, local activity, edge of chaos kernel, pattern generation, pattern operations

Angela Slavova (Institute of Mechanics, Bulgarian Academy of Sciences) and Ventsislav Ignatov (Institute of Mechanics, Bulgarian Academy of Sciences)

Abstract

In this paper we study the cellular nonlinear network model (CellNN) of the FitzHugh Nagumo system. The mathematical model which is simplification of Hodgkin-Huxley model of neural excitation transmission consists of a FitzHugh Nagumo system of differential equations with two diffusion terms. We study the dynamics of this model by applying local activity theory. Moreover, the edge of chaos kernel (EOCK) is defined for it in order to prove that our model exhibits the edge of chaos phenomenon of being stable yet potentially unstable. Applications in pattern generation and pattern operations are presented.

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