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## Lecture SCT2 - Process Integration

## 1. Web-based virtual Lecture: April 15 2021 Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik Technische Universität Dresden

Summer Semester 2021

To start the lecture click on [



"SCT2SS21-01.1" 51:39

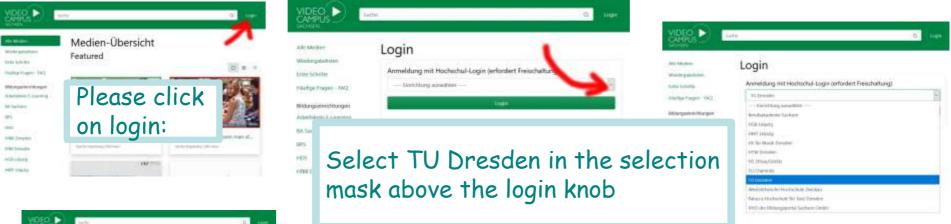


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## Virtual Lecture - How to watch the streams

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Now you continue with your personal login procedure. Use the same username and password as you do for OPAL or ZIH!



Finally you are logged on at VCS. Now you are able to access the streams. Please stay logged on as long as you work with the pdf



Next time, you click on a stream symbol, you see something like this. Enjoy the stream!



## > About the partial reuse of Slides and streams



## OPAL Registration, where to find the slides

Intro of the lecturer

Lab associated with the lecture -DMA 2021

Books - Exam

Wrap up of SCT1 - left over from SCT1



## • OPAL! Please sign up.

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		Semiconductor Technology 2 - Process Integration -					

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• OPAL! You find the pdf slides and other stuff here:

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Remarks & organizational stuff:

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## About the instructor



CV: Johann W. Bartha

Johann.Bartha@tu-dresden.de TU Dresden, IHM/mierdel-Bau Nöthnitzer Str. 64 01062 Dresden +49 351 463 35292 http://www.ihm.tu-dresden.de/

Prof. Dr. Johann W. Bartha received a Diploma and PhD. degree in solid state physics at the University of Hannover, Germany. He was two years Post Doc at the IBM T. J. Watson Research Center Yorktown Heights, N. Y. were he investigated Metal Polyimide interfaces for applications in multi layer ceramic packaging. 1985 he joined the IBM German Manufacturing Technology Center (GMTC) at Sindelfingen Germany as staff member and became responsible for plasma based technologies in semiconductor processing as a senior staff member. 1994 he accepted a professorship at the University of Applied Sciences at Münster, Germany where he established a laboratory for micro manufacturing. 1999 he accepted a C4 professorship as head of the chair for Semiconductor Technology at the Dresden University (TUD). Since March 2003 he is director of the Institute of Semiconductor- and Microsystems technologies at TUD and established a strong collaboration between Dresden University and local semiconductor Industry. The research focus at his department is BEOL processing including barriers (ALD and PVD), ECD and CMP. Since 4/2019 he is retired but continues as senior professor at IHM.

Prof. Bartha is member of the DPG (German physical society), the ECS (Electrochemical society) and foundation member of the Silicon Saxony association. He is co-organizer of several international conferences in the field of microelectronics (IITC - International Interconnect Conference, European AEC/APC, ICPT 2007 - Int. Conf. on Planarization Technology, IWFIPT 2007 - Int. Workshop on Future Information Processing Techn., MRS Spring Symposium on CMP 2004 and 2010) and co-founder of the Dresden Summer School Microelectronics. He was non voting member in the board of the CNT until 2009 (a joint R&D organization of AMD, Qimonda and Fraunhofer) and is head of the NaMLab gGmbH scientific board (materials research company owned by TUD).



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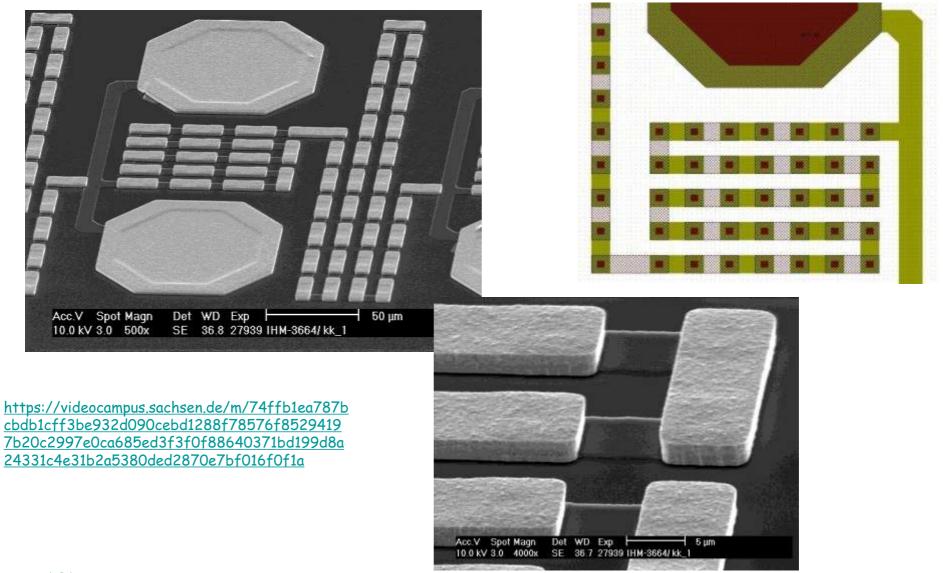


## The access to the lab is restricted! General admission to the lab is only for those students, where the lab is part of the regular study plan and

for those students who did not perform the lab before!



## SCT2 Laboratory Fabrication of a contact chain





- Chemical Vapor Deposition (CVD) / Atomic Layer Deposition (ALD)
- **RIE structuring** contact vias
- **Sputtering metal** for barrier/seed layer
- Lithography structures/ resist mask for galvanic copper deposition
- **Pattern plating** copper structures 2nd conducting layer
- Wet chemical etch seed layer and barrier
- **Electrical measurement** of contacts and conducting layer parameters







## > Students are merged in groups of 4

> Each group will have two appointments in the summer semester with a duration of about 3 time hours each

> At such an appointment one specific task out the 7 is performed together with an assistant professor

> You need to be prepared for the appointment and afterwards a protocol is requested



This Year it will be 2 out of the 7!

- Chemical Vapor Deposition (CVD) / Atomic Layer Deposition (ALD)
- **RIE structuring** contact vias
- **Sputtering metal** for barrier/seed layer
- Lithography structures/ resist mask for galvanic copper deposition
- **Pattern plating** copper structures 2nd conducting layer
- Wet chemical etch seed layer and barrier
- Electrical measurement of contacts and conducting layer parameters

https://bildungsportal.sachsen.de/opal/auth/Repository Entry/5690753028/CourseNode/101358303504339



General admission to the lab is only for those students, where the lab is part of the regular study plan!

This means specifically for the current SS21, allowed are:

- > The NES students with starting semester WS20/21
- > The OME students with starting semester WS20/21
- > The MEL students of module ET-121201 in the 6'th semester
- And students of earlier starting semesters of the groups above, who, for good reasons were not able to attend the lab before.

This applies also to students who, for what reason ever, repeat a module. A former attendance of the lab will be counted for the repetition as well!



## Remarks & organizational stuff:

## Lab organization by appointment: Time Windows

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## Remarks & organizational stuff:

## Lab organization by appointment: Registration

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Intro of the lecturer

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## https://cfaed.tudresden.de/dmawelcome



Production: Jan Luther - http://www.app-bis-web.de

#### Welcome to the cfaed Summer School: Dresden Microelectronics Academy

Save-the-date: 20-24 September 2021 - please check here regularly for updates on the format and program of DMA'21!

This one-week summer school showcases Dresden as Europe's largest microelectronics hub and TU Dresden as the ideal place to study and work!

#### Who can apply

 advanced students (Master/Diplom students) / PhD students / postdocs of engineering with affinity to micro-/nanoelectronics, e.g., design, technology and test



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S.M. Sze,	VLSI Technology	Mc Graw-Hill Inc, 1983/1988
S.M. Sze	Semiconductor Devices Physics and Technology	John Wiley & Sons 1985/2002
Stephen A. Campbell	The Science and Engineering of Microelectronic Fabrication	Oxford University Press 1996
J.D. Plummer, M. Deal, P.B. Griffin	Silicon VLSI Technology	Prentice Hall, 2000
S. Wolf	Silicon Processing for the VLSI Era, Vol. 1-4 Insbesondere Vol. 2, Process Integration	Lattice Press 2000-2004
Sima Dimitrijev	Understanding Semiconductor	Oxford University Press 2000
S. Wolf	Microchip Manufacturing	Lattice Press 2004



https://www.spiedigitallibrary.org/ebooks/PM/Introduction-to-Semiconductor-Manufacturing-Technology-Second-Edition/eISBN-9780819490933/10.1117/3.924283?SSO=1 Chapter 2, 3, 13 to 15!

## Sima Dimitrijev Understanding Semiconductor Devices Oxford University Press 2000

This book contains a CD-ROM with mathlab animations which I will use for demonstration purpose

## S. Wolf Microchip Manufacturing Lattice Press 2004

# Exam will be written (120 min.) probably mid to end of July



OPAL Registration, where to find the slides

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Introduction		6.1.3.	Reaction Kinetics Môn crystalline vs. Polycrystalline Pattern Displacement
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from an infinite Source from a finite Source Two step Diffusion Further Effects Practical Realization Implantation Projected Range Implantation - Masks Channeling Further Effects Healing and Activation Implantation Systems		8.3.1. 8.3.2. 8.3.3. 8.3.4. 8.3.5.	Sputter-Etching Plasma Induced Chemical Etching Reactive Ion Etching Process Parameters Plasmatools
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4.1.2.	Positive Resist	8.1.4.	Plasma Generation
4.2.	Multi-Layer Resists	8.2	Sputter Deposition
4.3.	Image Reversal	8.2.1.	Sputter Deposition of Alloys
4.4.	Pattern Enhancement	8.2.2.	Reactive Sputtering
		8.2.3.	Magnetron Sputtering
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5.2.3.	Channeling		
5.2.4.	Further Effects		
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4.1.2.	Positive Resist	8.1.4.	Plasma Generation
4.2.	Multi-Layer Resists	8.2	Sputter Deposition
4.3.	Image Reversal	8.2.1.	Sputter Deposition of Alloys
4.4.	Pattern Enhancement	8.2.2.	Reactive Sputtering
		8.2.3.	Magnetron Sputtering
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5.1.2.	from a finite Source	8.3.2.	Plasma Induced Chemical Etching
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5.1.5.	Practical Realization	8.3.5.	Plasmatools
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5.2.3.	Channeling		
5.2.4.	Further Effects		
5.2.5.	Healing and Activation		
5.2.6.	Implantation Systems		

https://www.youtub e.com/watch?v=Uvlu uAIiA50&t=283s

https://www.halbleiter.org/index.php/?sprache=en



https://bildungsportal.sachsen.de/opal/auth/BusinessGroup/26548961288/menu/MENU FOLDER

Please watch this clip (~10 min.) and look for the question: Which of the presented technologies in the video were not covered in lecture SCT1?



https://www.youtub e.com/watch?v=Uvlu uAIiA50&t=283s

Lecture Semiconductor Technology I, Prof. Dr. J. W. Bartha

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Silicon as Substrate Material The Silicon Crystal **Crystal Defects** Conductivity and Doping Si as the most important material of Microelectronics Fabrication of pure Silicon Si Wafer Fabrication

#### The Oxidation of Silicon

Growth model after Deal and Grove Dependency on Process parameters Oxidation technique Stress and Oxidation

#### Lithography

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#### Doping

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- 5.1.2. ... from a finite Source
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### Terms and Classification of the manufacturing sequence

"SCT2\_1.2" 46:09





Terms and Classification of the manufacturing sequence

"SCT2\_1.2" 46:09

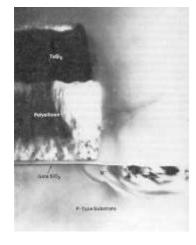
### Basic distinction of processing in:





Terms and Classification of the manufacturing sequence

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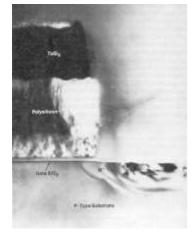
Basic distinction of processing in:

Front end (of line) FEOL





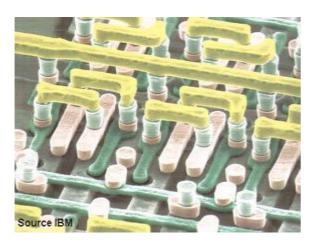
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### Basic distinction of processing in:

Front end (of line) FEOL

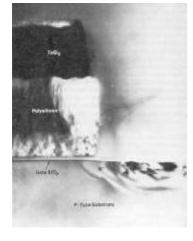
back end of line or interconnect or metallization BEOL







"SCT2\_1.2" 46:09



## Basic distinction of processing in:

Front end (of line) FEOL

back end of line or interconnect or metallization BEOL

and back end or packaging







Wire Bonding (Kaijo Corporation)

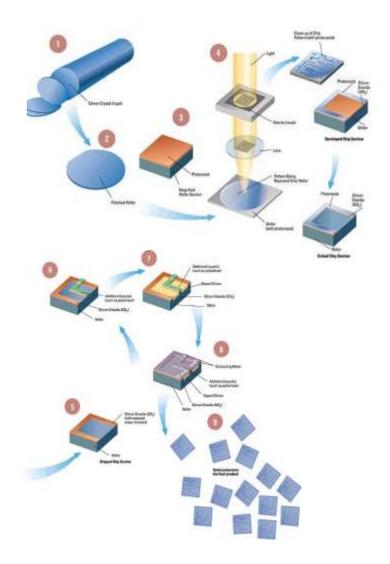


## Semiconductor Processing

Technology inventory: Oxidation Lithography Etching (wet & dry, polish) Doping => Implantation (Diffusion) Deposition **Chemical Vapor Deposition** (CVD +/- Plasma) - ALD Evaporation / Sputter Deposition (PVD)

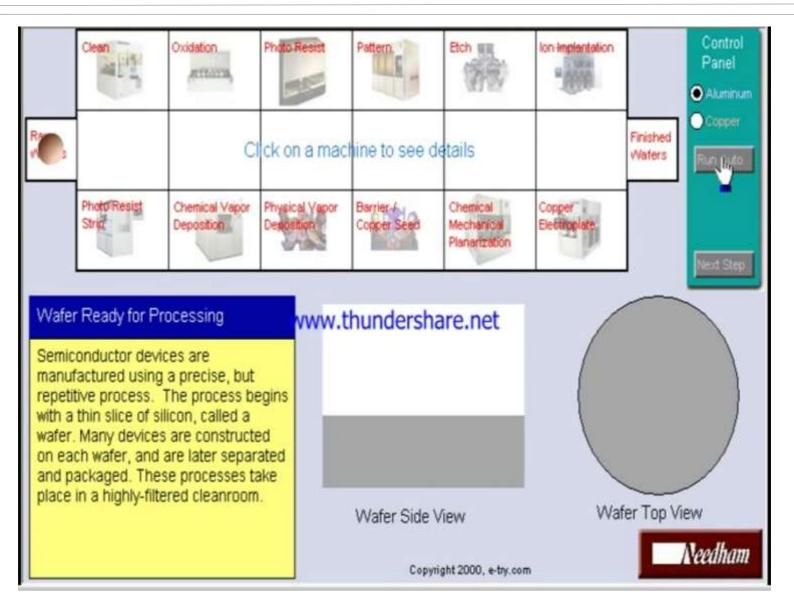
Electrochem. Depo. (ECD)

http://www.semiconductor.net/info/CA6432169.html



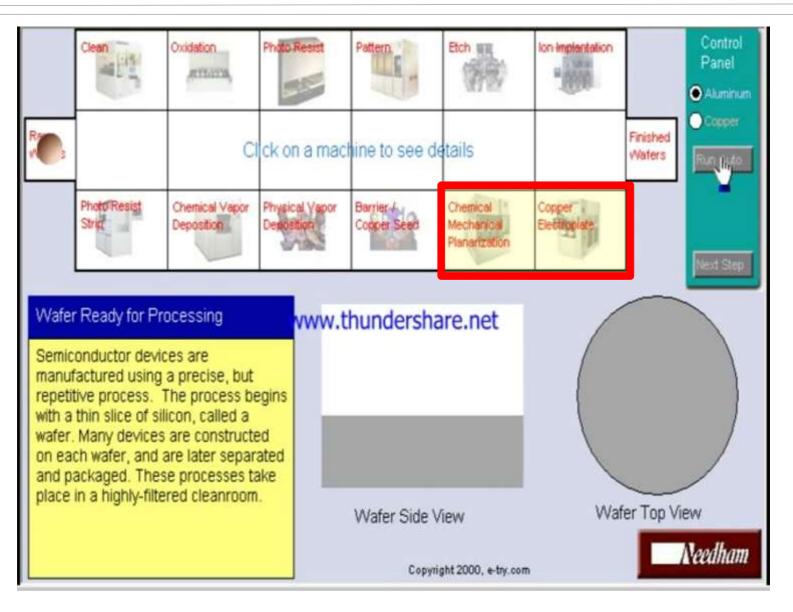


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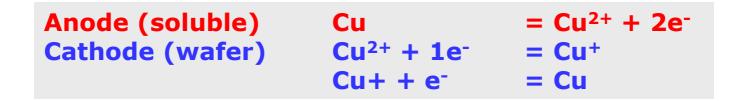
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	Oxidation technique			
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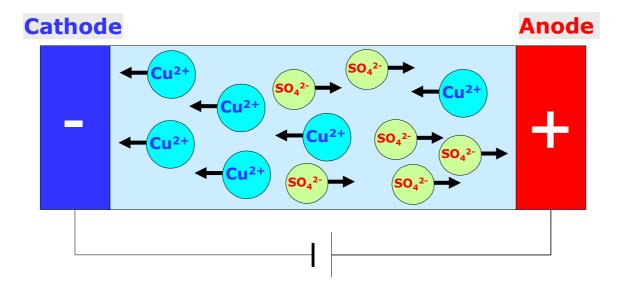


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## Cu Electroplating







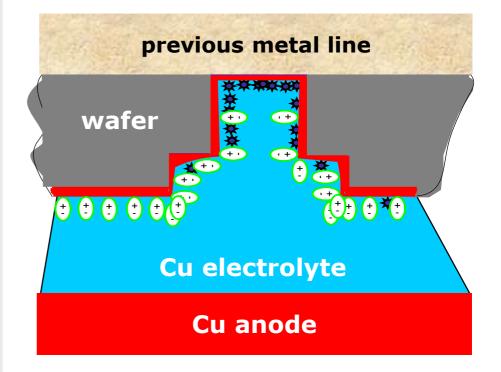
## Cu Electroplating - Additives

#### +- Suppressor / Leveler

- ✓ absorbed preferentially on the peaks of the substrate and inhibit the deposition on this particular location
   ✓ act as wetting agent
- $\checkmark$  long chain polymers

#### ★ Accelerator

- ✓ absorbed preferred at the bottom of the feature
- ✓ supports deposition in this area
- ✓ sulfonic acid





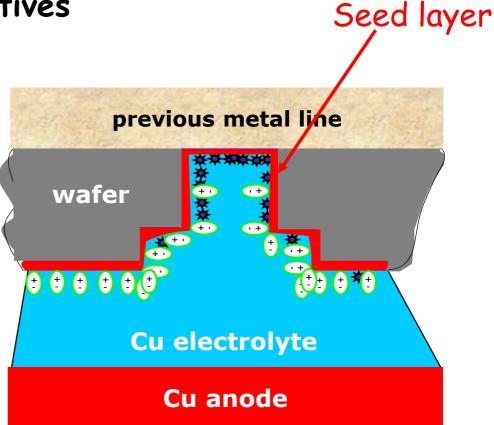
## Cu Electroplating - Additives

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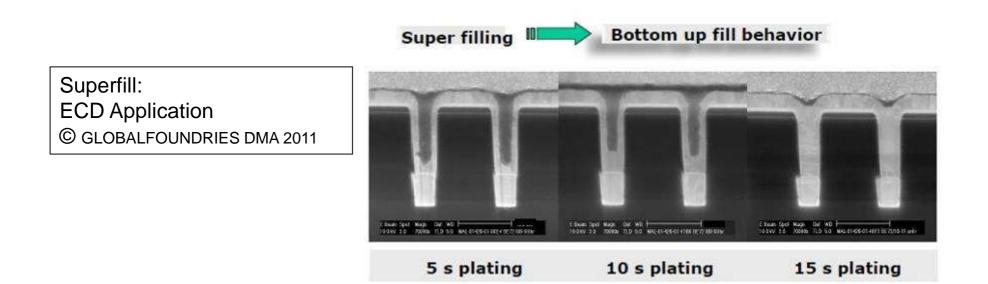
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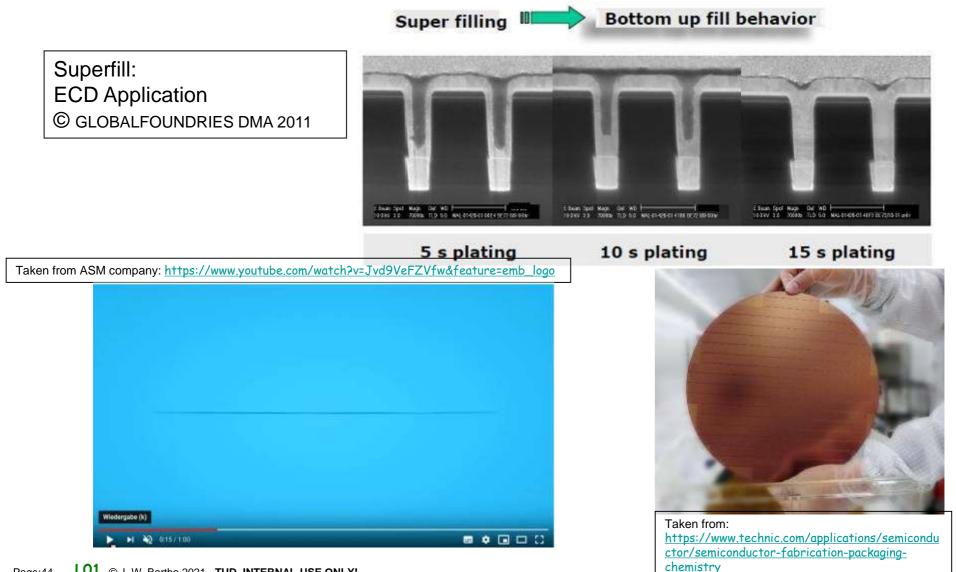
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	Lecture Semiconductor Technology I, Prof. Dr. J. W. <u>Bartha</u>	<u> </u>	<b>6.</b> 6.1.	<mark>Epitaxy</mark> Gas Phase <u>Epitaxy</u>
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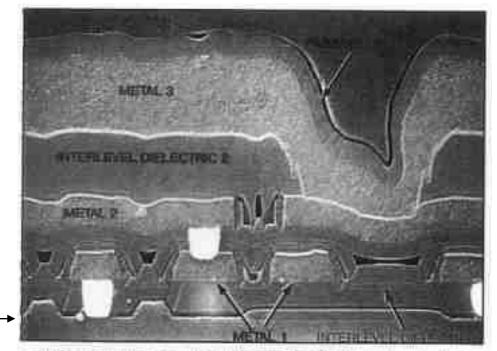


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				eft over: CMP
		-		



In the evolution of IC products the corrugation of surface topologies grew constantly. On the other hand the CD became constantly smaller. At a certain point in time the technically possible DOF was larger than the corrugation of the surface. =>

It became necessary to create a technology for planarization!

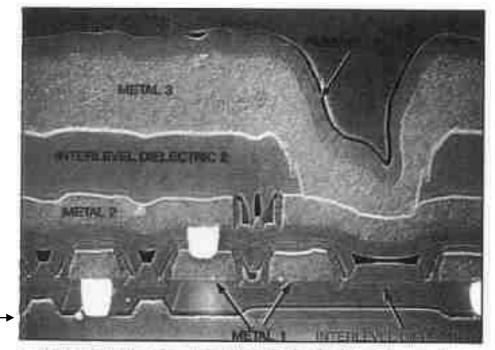


 Digital Equiment Corp.'s Alpha chip has both tungsten and conventional vias.



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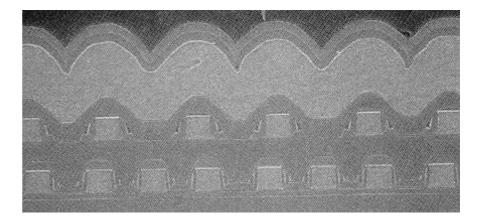
 Digital Equiment Corp.'s Alpha chip has both tungsten and conventional vias.

## CMP :=

#### Chemical mechanical Polishing Chemical mechanical Planarization



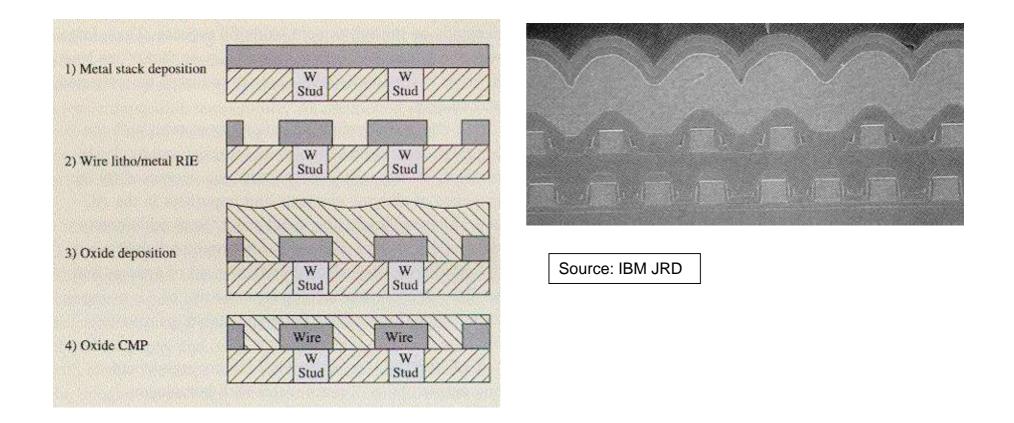
Example: Oxide planarization after CVD of insulator layer



Source: IBM JRD

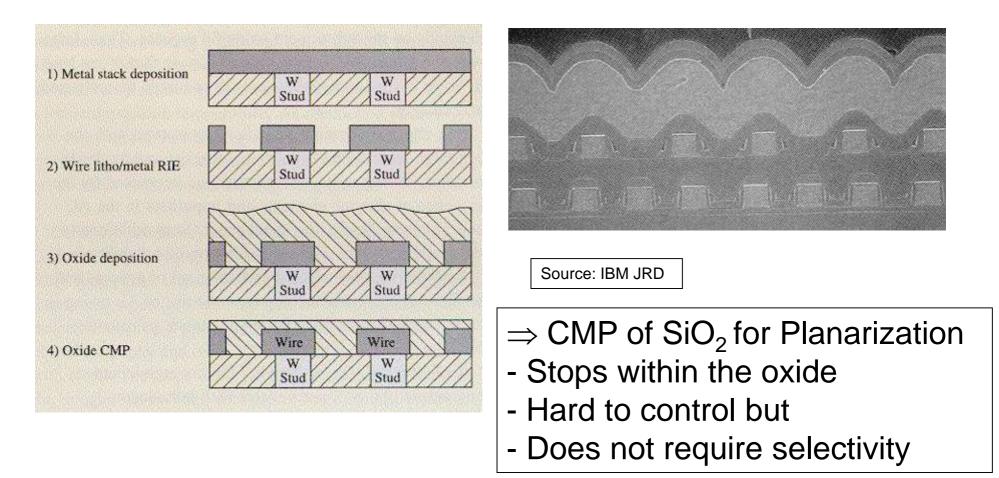


#### Example: Oxide planarization after CVD of insulator layer



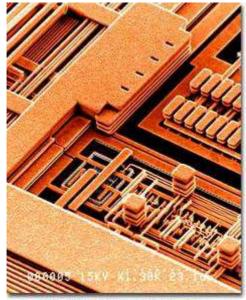


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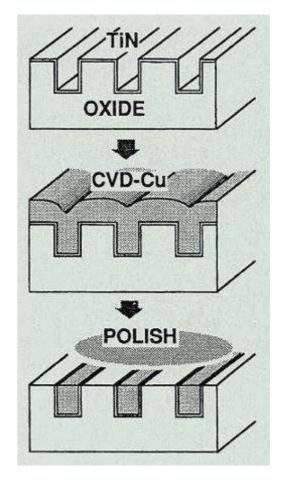


#### The necessity of CMP on Cu results from the unavailability of Cu – RIE!



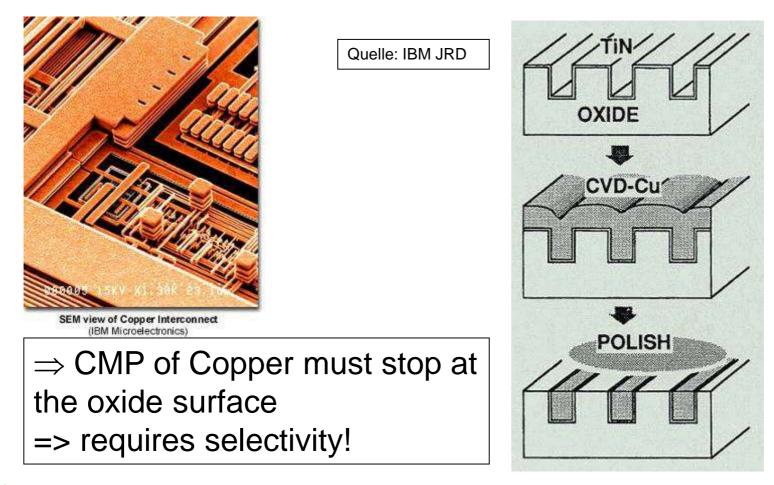
SEM view of Copper Interconnect (IBM Microelectronics)

Quelle: IBM JRD





#### The necessity of CMP on Cu results from the unavailability of Cu – RIE!





Platen rotation Velocity Down force (applied pressure) Slurry supply rate	10–100 rpm 10–100 cm/s 10–50 kPa 50–500 ml/min	down force	slurry dispense
Polish rate Selectivity Uniformity across wafer Wafer-to-wafer repeatability	100–1000 nm/min 1:1 to 100:1 10% 10%	spindle chuck wafer	0
Table 16-1 CMP tool parameters and pr	rocess responses.	slurry pad platen	

Figure 16-2 Schematic structure of rotary CMP equipment. Wafer is held face down in the spindle chuck.

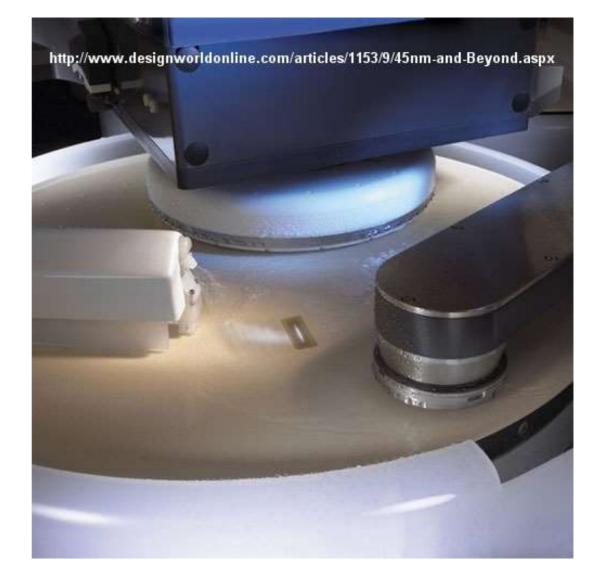


Polish rate 100–1000 nm/min Selectivity 1:1 to 100:1 Uniformity across wafer 10% Wafer-to-wafer repeatability 10% Table 16-1 CMP tool parameters and process responses.		spindle chuck wafer slurry pad platen		
Slurry is an aquaus suspension that contains besides abrasive particles			C	

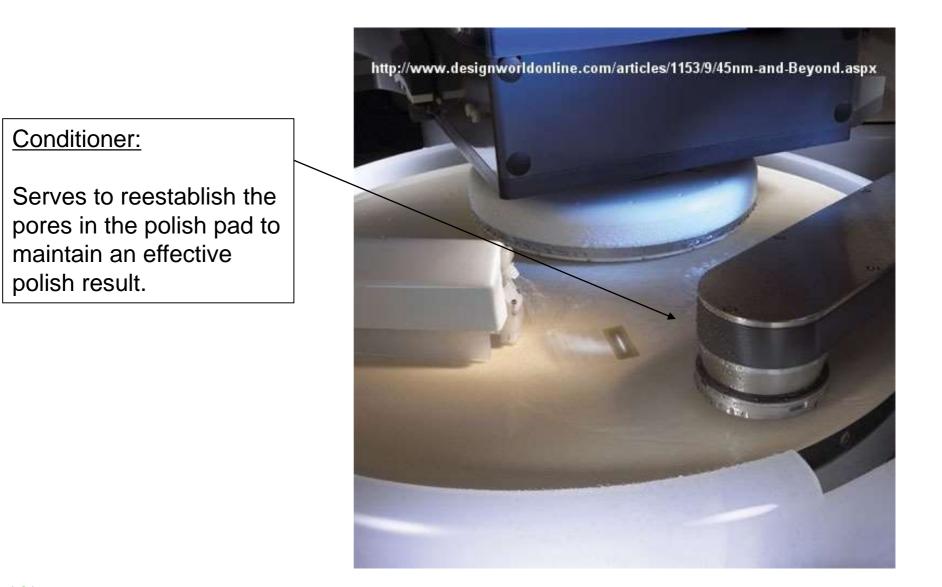


Schematic structure of rotary CMP equipment. Wafer is held face down in the spindle chuck.











#### **Conditioner:**

Serves to reestablish the pores in the polish pad to maintain an effective polish result.

<u>https://s3-</u> <u>alliance.com/products/rd-cmp-</u> <u>poli-500-2/</u>





Fundamental equation of CMP by Preston:

$$R = \Delta H / \Delta t = K_{\rm p} P (\Delta s / \Delta t)$$

- $\Delta H$  = change in the height of the surface
  - P = pad pressure
- $K_{\rm p}$  = Preston coefficient
- $(\Delta s / \Delta t)$  = linear velocity of the pad relative to the wafer.



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The removal rate is proportional to (local!) DownForce (Pressure) and Velocity (relative velocity between pad and wafer)



# Fundamental equation of CMP by Preston:

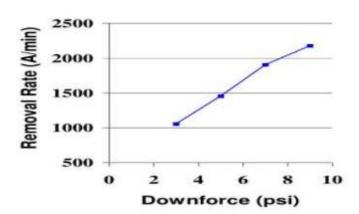
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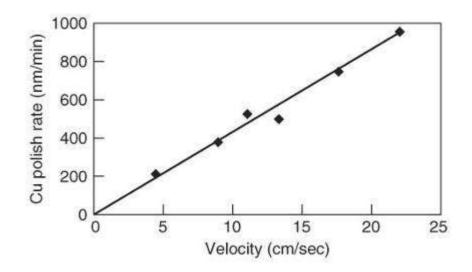
P = pad pressure

- $K_{\rm p} = \text{Preston coefficient}$
- $(\Delta s / \Delta t)$  = linear velocity of the pad relative to the wafer.

The removal rate is proportional to (local!) DownForce (Pressure) and Velocity (relative velocity between pad and wafer)



https://www.slideserve.com/nola-harrison/tutorial-on-chemical-mechanical-polishing-cmp





Copper polish rate as a function of velocity (15 kPa pressure). Reproduced from Steigerwald *et al.* (1997) by permission of John Wiley & Sons, Ltd.



The planarization effect is a result of the local difference in pressure between UP (hills in the topography) and DOWN (Valeys in the topography) areas.

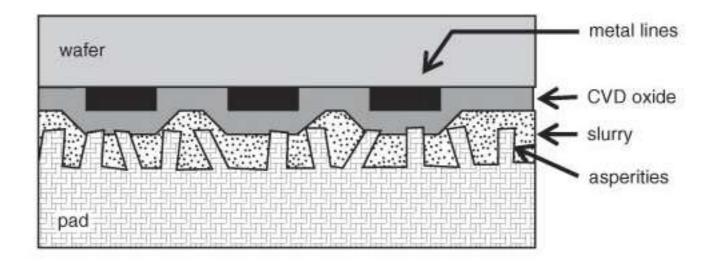
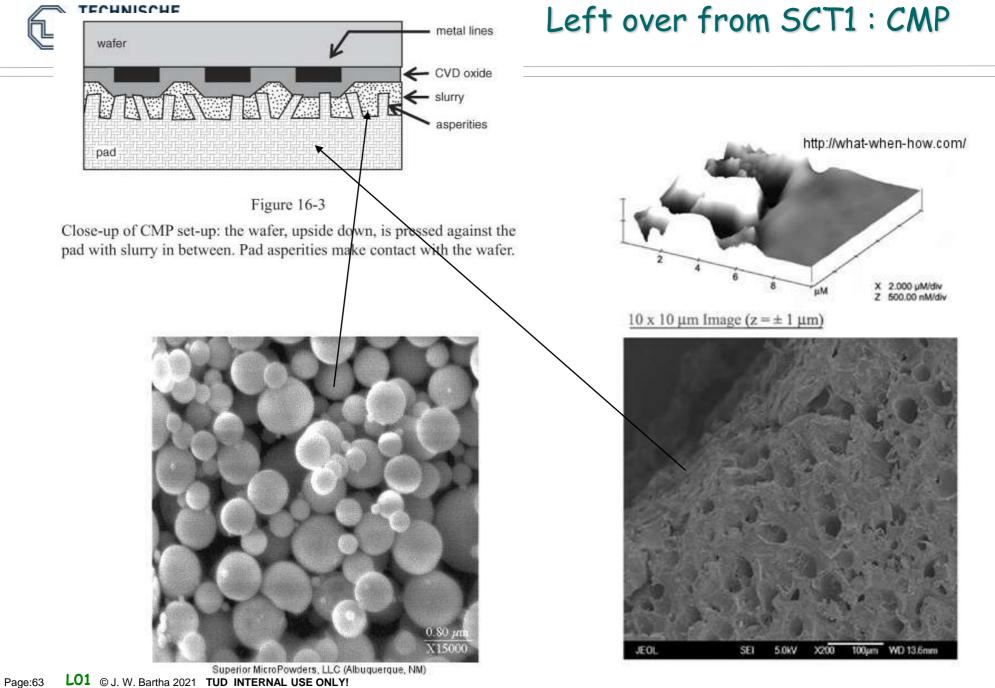
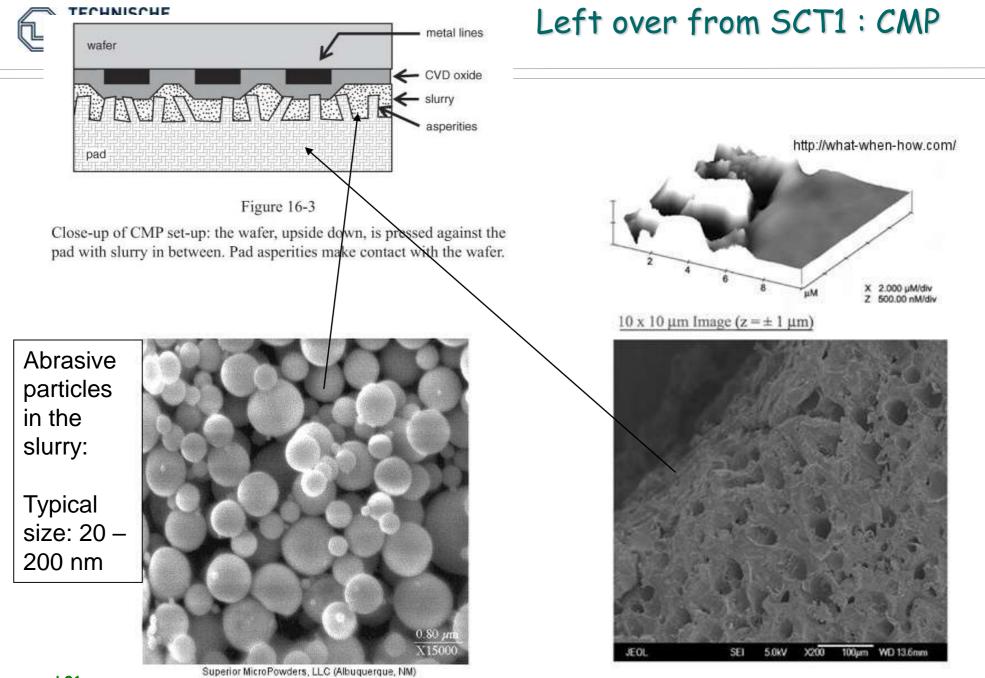


Figure 16-3

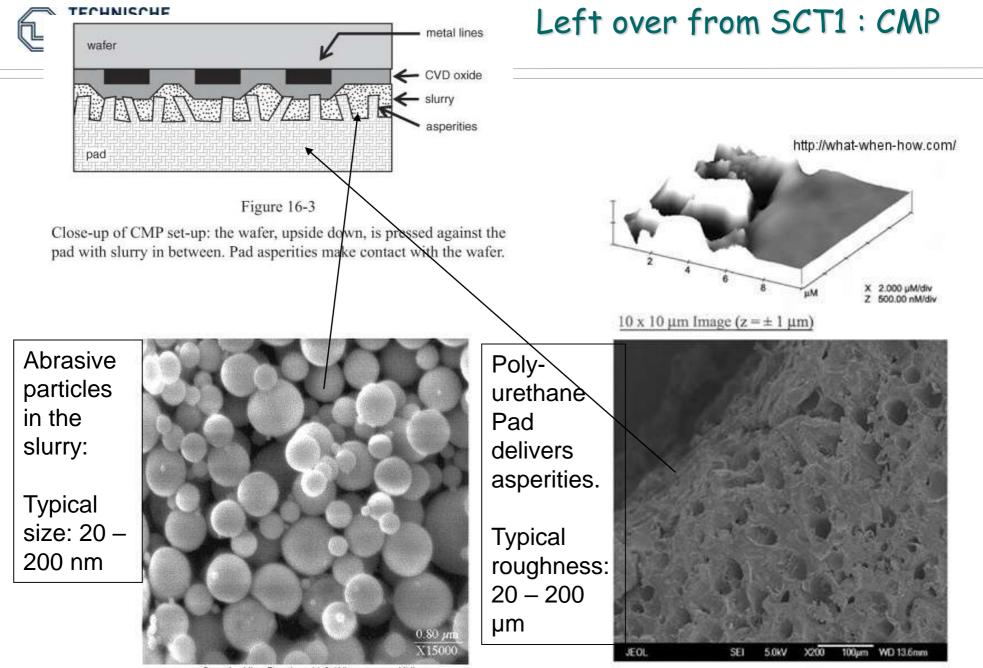
Close-up of CMP set-up: the wafer, upside down, is pressed against the pad with slurry in between. Pad asperities make contact with the wafer.



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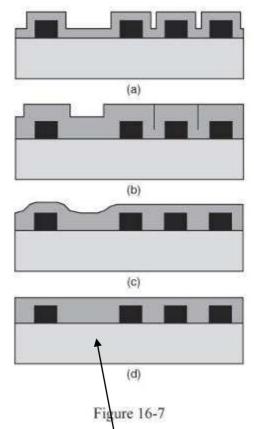


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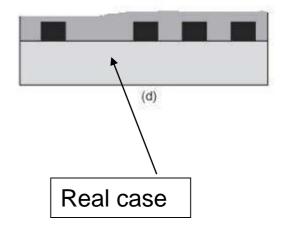
Superior MicroPowders, LLC (Albuquerque, NM) LO1 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!



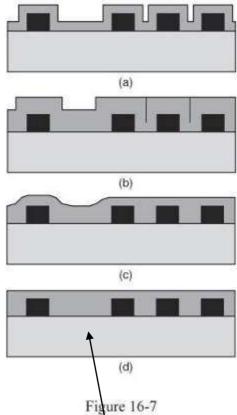


Planarization: (a) thin conformal deposition, no planarization; (b) thick conformal deposition, gap filling but no planarization, (c) local planarization by spin-on film; (d) global planarization by CMP of thick conformal deposition.

Ideal planarization





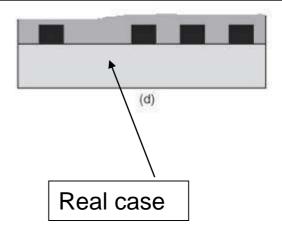


Planarization: (a) thin conformal deposition, no planarization; (b) thick conformal deposition, gap filling but no planarization, (c) local planarization by spin-on film; (d) global planarization by CMP of thick conformal deposition.

Ideal planarization

The local removal rate depends on the local pattern density!

A low pattern density causes a high removal rate! (The global downforce concentrates at only a few contact spots – high local pressure!)





## For those, who want to learn more about CMP

## I recommend the following tutorial of a company supplying CMP consumables: Cabot Microelectronics

#### Please click on the section

#### Outline

Section 1: Intro to Chip Manufacturing & Design

Section 2: CMP Tools and Process

Section 3: Fundamentals of CMP Slurries

Section 4: Fundamentals of CMP Polishing Pads

Section 5: CMP Challenges

Section 6: Summary & Closing Remarks

## Perfecting the Surfaces of Tornarian Cabot Microelectronic Microelectronic Cabot Cab

Fundamentals of CMP & Slurry

Section 1: Introduction to Chip Manufacturing & Design

CMC Technical Marketing

9:50 Cabot Microelectronic

Fundamentals of CMP & Slurry

Section 4: Fundamentals of CMP Polishing Pads

CMC Technical Marketing

Fundamentals of CMP & Slurry

Section 2: CMP Tools and Process

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**Fundamentals** 

Fundamentals of CMP & Slurry

Section 3: Fundamentals of CMP Slurries

CMC Technical Marketing



Sections 5 & 6: CMP Challenges

of CMP

& Slurry

Summary & Closing Remarks

CMC Technical Marketing







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	Prof. Dr. J. W. Bartha		6.	Epitaxy
			6.1.	Gas Phase Epitaxy
	Content		6.1.1.	Uniformity
			6.1.2.	Reaction Kinetics
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1000	mouncain		6.1.4.	Pattern Displacement
2.	Silicon as Substrate Material		6.1.5.	Doping
2.1	The Silicon Crystal		6.1.6.	Epi-Reactor + Process
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4743	02/2 30		8.2.3.	Magnetron Sputtering
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5.2.6.	Implantation Systems		· ·	
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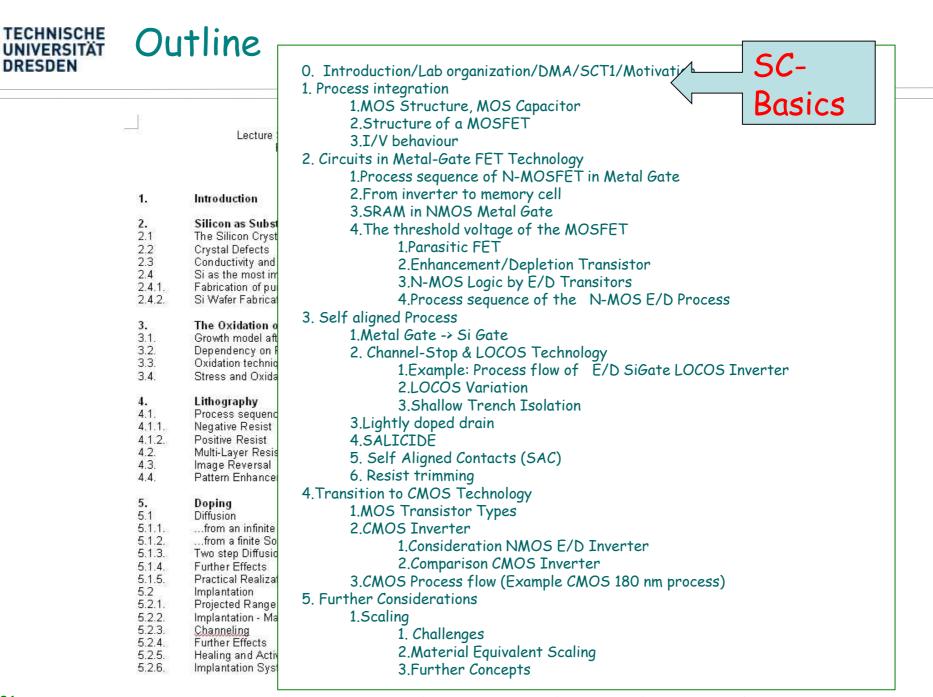


Ou	itline	0. Introduction/Lab organization/DMA/SCT1/Motivation
	Lecture :	<ol> <li>Process integration         <ol> <li>1.MOS Structure, MOS Capacitor</li> <li>2.Structure of a MOSFET</li> <li>3.I/V behaviour</li> </ol> </li> <li>Circuits in Metal-Gate FET Technology         <ol> <li>1.Process sequence of N-MOSFET in Metal Gate</li> </ol> </li> </ol>
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4. 4.1. 4.1.1. 4.1.2. 4.2. 4.3. 4.4.	Lithography Process sequenc Negative Resist Positive Resist Multi-Layer Resis Image Reversal Pattern Enhance	3.Shallow Trench Isolation 3.Lightly doped drain 4.SALICIDE 5. Self Aligned Contacts (SAC) 6. Resist trimming
5. 5.1 5.1.2. 5.1.3. 5.1.4. 5.1.5. 5.2 5.2.1. 5.2.2. 5.2.3. 5.2.4. 5.2.5. 5.2.6.	<b>Doping</b> Diffusion from an infinite So Two step Diffusio Further Effects Practical Realizat Implantation Projected Range Implantation - Ma <u>Channeling</u> Further Effects Healing and Activ Implantation Syst	<ul> <li>4.Transition to CMOS Technology <ol> <li>MOS Transistor Types</li> <li>CMOS Inverter <ol> <li>Consideration NMOS E/D Inverter</li> <li>Comparison CMOS Inverter</li> <li>CMOS Process flow (Example CMOS 180 nm process)</li> </ol> </li> <li>5. Further Considerations <ol> <li>Challenges</li> <li>Material Equivalent Scaling</li> <li>Further Concepts</li> </ol> </li> </ol></li></ul>



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<b>3.</b> 3.1.	The Oxidation o Growth model aft	1.Metal Gate -> Si Gate
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http://www.computerhistory.org/siliconengine/timeline/



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