TECHNISCHE UNIVERSITÄT DRESDEN

The hyperlinks to the video streams in this virtual lecture are marked by the Video Campus Sachsen Logo. To watch them you need to be logged on at the host: VCS. Please click on: https://videocampus.sachsen.de/login select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 – Process Integration

1. Web-based virtual Lecture: April 15 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

To start the lecture click on 

"SCT2SS21-01.1" 51:39

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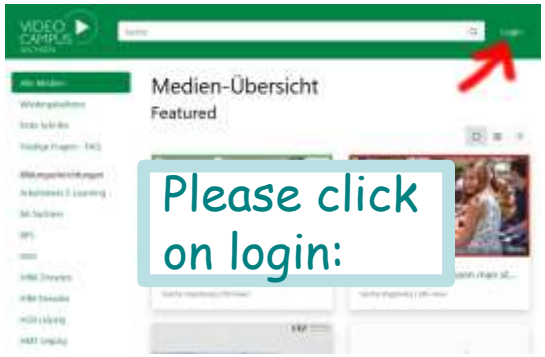
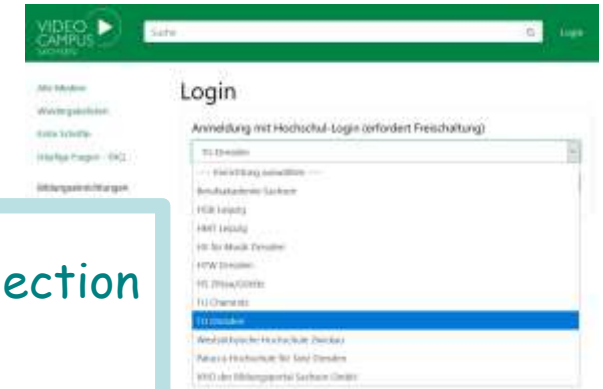
Virtual Lecture – How to watch the streams

When you klick on one of the VCS symbols, this will bring you to the VCS site. If you are already logged on at VCS you will be able to start a video stream. Otherwise you will just see the VCS Start Page. In that case you need to login in the following way:



Please click on login:

Select TU Dresden in the selection mask above the login knob



Now you continue with your personal login procedure.
Use the same username and password as you do for OPAL or ZIH!

Finally you are logged on at VCS. Now you are able to access the streams. Please stay logged on as long as you work with the pdf

Next time, you click on a stream symbol, you see something like this. Enjoy the stream!

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Remarks & organizational stuff

> About the partial reuse of Slides and streams

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Remarks & organizational stuff:

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Intro of the lecturer

Lab associated with the lecture – DMA 2021

Books - Exam

Wrap up of SCT1 – left over from SCT1

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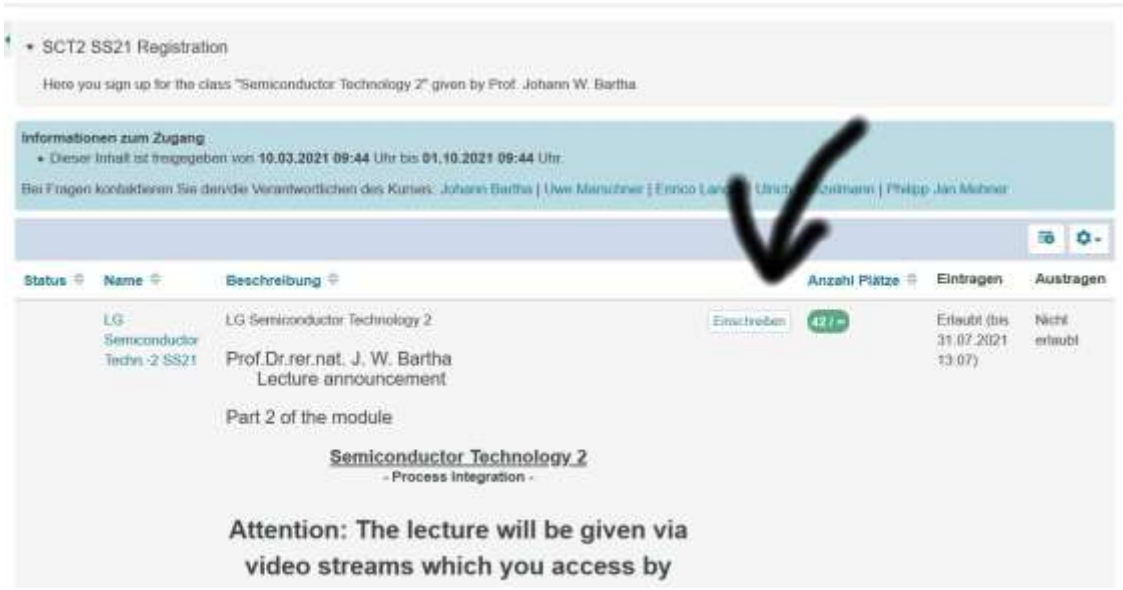
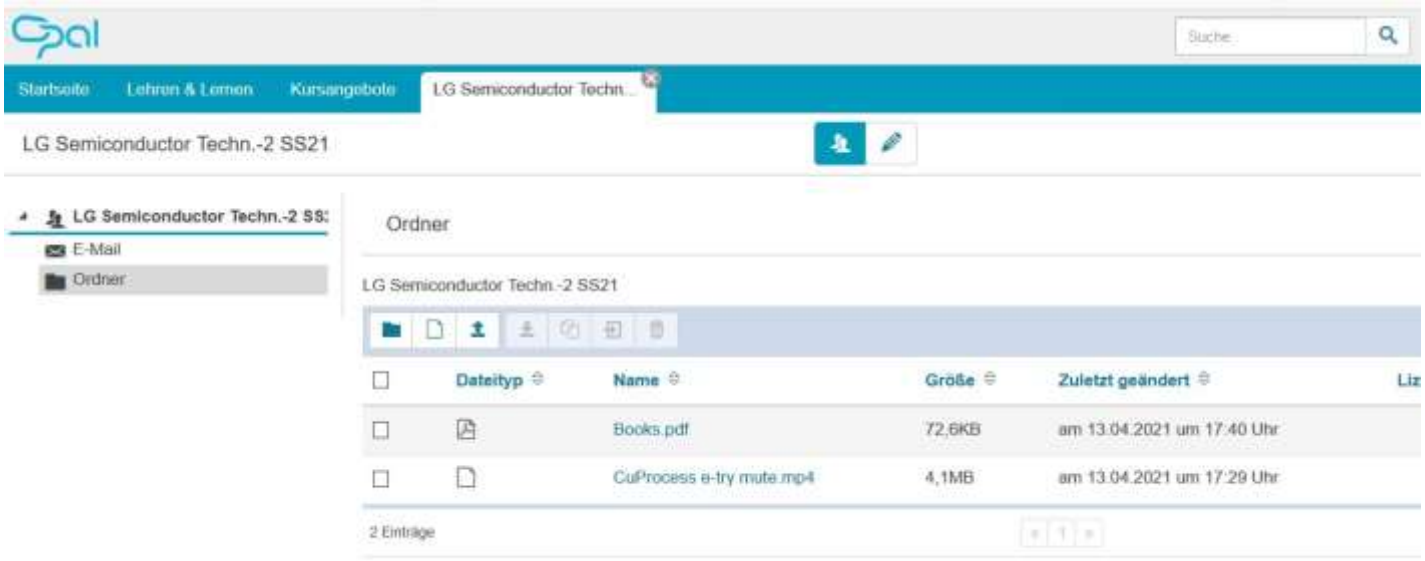
- OPAL! Please sign up.



https://bildungsportal.sachsen.de/opal/auth/RepositoryEntry/5690753028/CourseNode/8847426428590 6?17

- OPAL! You find the pdf slides and other stuff here:



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About the instructor

CV: Johann W. Bartha

Johann.Bartha@tu-dresden.de
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01062 Dresden
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http://www.ihm.tu-dresden.de/

Prof. Dr. Johann W. Bartha received a Diploma and PhD. degree in solid state physics at the University of Hannover, Germany. He was two years Post Doc at the IBM T. J. Watson Research Center Yorktown Heights, N. Y. were he investigated Metal Polyimide interfaces for applications in multi layer ceramic packaging. 1985 he joined the IBM German Manufacturing Technology Center (GMTC) at Sindelfingen Germany as staff member and became responsible for plasma based technologies in semiconductor processing as a senior staff member. 1994 he accepted a professorship at the University of Applied Sciences at Münster, Germany where he established a laboratory for micro manufacturing. 1999 he accepted a C4 professorship as head of the chair for Semiconductor Technology at the Dresden University (TUD). Since March 2003 he is director of the Institute of Semiconductor- and Microsystems technologies at TUD and established a strong collaboration between Dresden University and local semiconductor Industry. The research focus at his department is BEOL processing including barriers (ALD and PVD), ECD and CMP. Since 4/2019 he is retired but continues as senior professor at IHM.
Prof. Bartha is member of the DPG (German physical society), the ECS (Electrochemical society) and foundation member of the Silicon Saxony association. He is co-organizer of several international conferences in the field of microelectronics (IITC – International Interconnect Conference, European AEC/APC, ICPT 2007 – Int. Conf. on Planarization Technology, IWFIPT 2007 – Int. Workshop on Future Information Processing Techn., MRS Spring Symposium on CMP 2004 and 2010) and co-founder of the Dresden Summer School Microelectronics. He was non voting member in the board of the CNT until 2009 (a joint R&D organization of AMD, Qimonda and Fraunhofer) and is head of the NaMLab gGmbH scientific board (materials research company owned by TUD).

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The access to the lab is restricted!

General admission to the lab is only for those students, where the lab is part of the regular study plan and for those students who did not perform the lab before!

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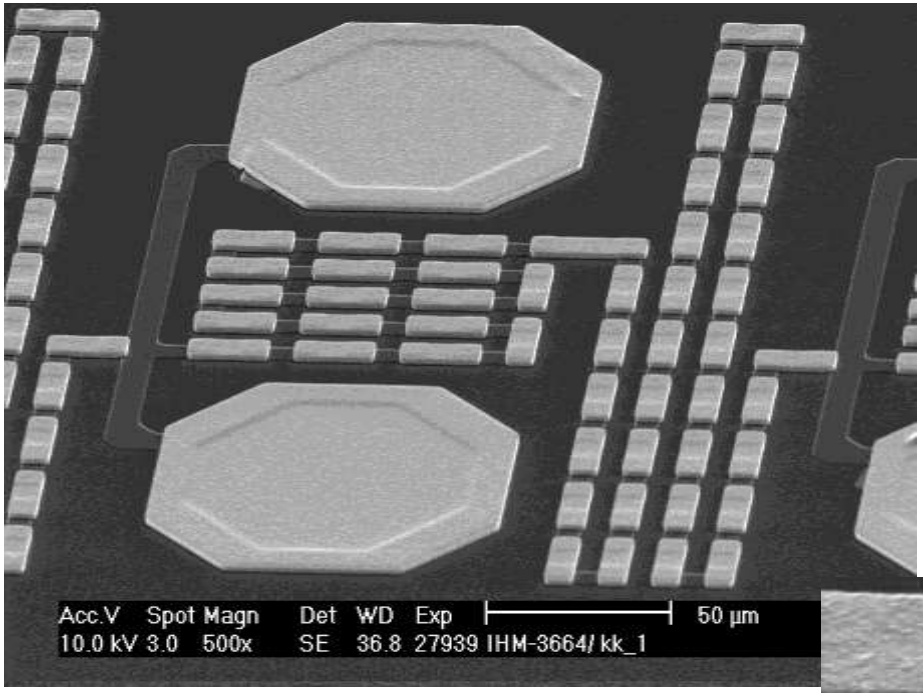
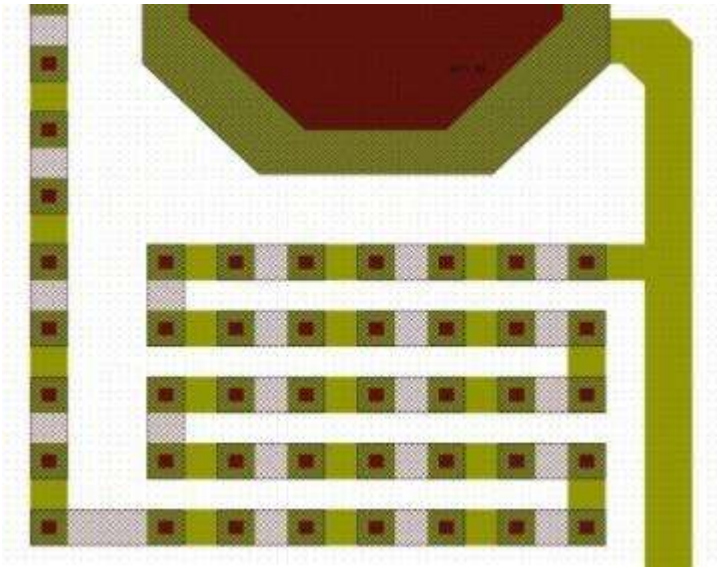
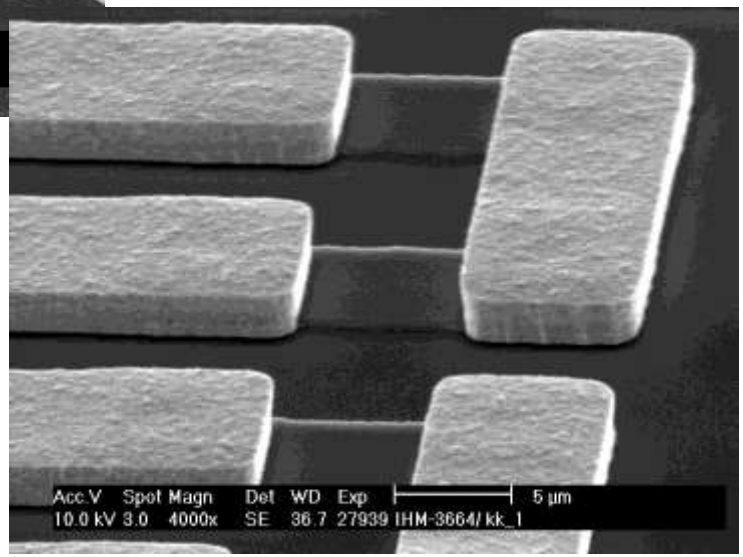
SCT2 Laboratory
Fabrication of a contact chain







https://videocampus.sachsen.de/m/74ffb1ea787bcbdb1cff3be932d090cebd1288f78576f85294197b20c2997e0ca685ed3f3f0f88640371bd199d8a24331c4e31b2a5380ded2870e7bf016f0f1a

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Inventory of 7 Experiments/Tasks

- **Chemical Vapor Deposition (CVD)** / Atomic Layer Deposition (ALD)
- **RIE structuring** contact vias
- **Sputtering metal** for barrier/seed layer
- **Lithography** structures/ resist mask for galvanic copper deposition
- **Pattern plating** copper structures 2nd conducting layer
- **Wet chemical etch** seed layer and barrier
- **Electrical measurement** of contacts and conducting layer parameters

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> Students are merged in groups of 4

> Each group will have two appointments in the summer semester with a duration of about 3 time hours each

> At such an appointment one specific task out the 7 is performed together with an assistant professor

> You need to be prepared for the appointment and afterwards a protocol is requested

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Inventory of 7 Experiments/Tasks
In regular Years every group of 4 students takes 3 out of the 7

This Year it will be 2 out of the 7!

- **Chemical Vapor Deposition (CVD)** / Atomic Layer Deposition (ALD)
- **RIE structuring** contact vias
- **Sputtering metal** for barrier/seed layer
- **Lithography** structures/ resist mask for galvanic copper deposition
- **Pattern plating** copper structures 2nd conducting layer
- **Wet chemical etch** seed layer and barrier
- **Electrical measurement** of contacts and conducting layer parameters

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Due to the large outlay concerning staff and expense, the participation in the lab is restricted!

General admission to the lab is only for those students, where the lab is part of the regular study plan!

This means specifically for the current SS21, allowed are:

- The NES students with starting semester WS20/21
- The OME students with starting semester WS20/21
- The MEL students of module ET-121201 in the 6'th semester
- And students of earlier starting semesters of the groups above, who, for good reasons were not able to attend the lab before.

This applies also to students who, for what reason ever, repeat a module. A former attendance of the lab will be counted for the repetition as well!

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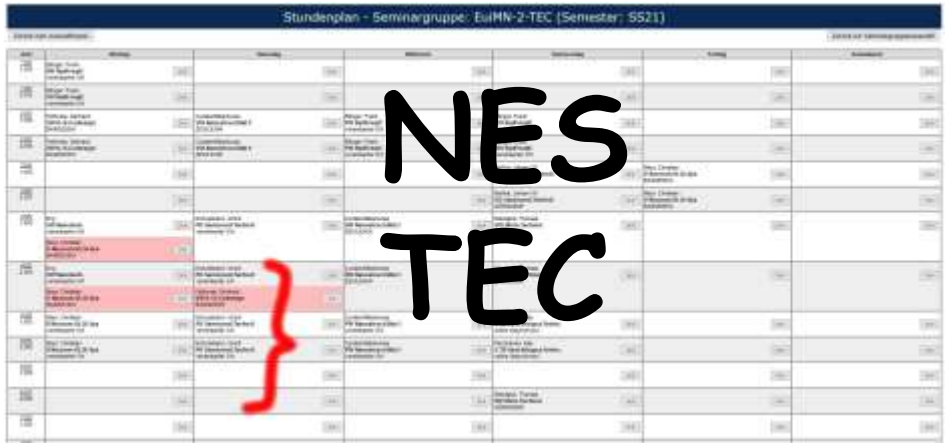
Remarks & organizational stuff:

Lab organization by appointment: Time Windows



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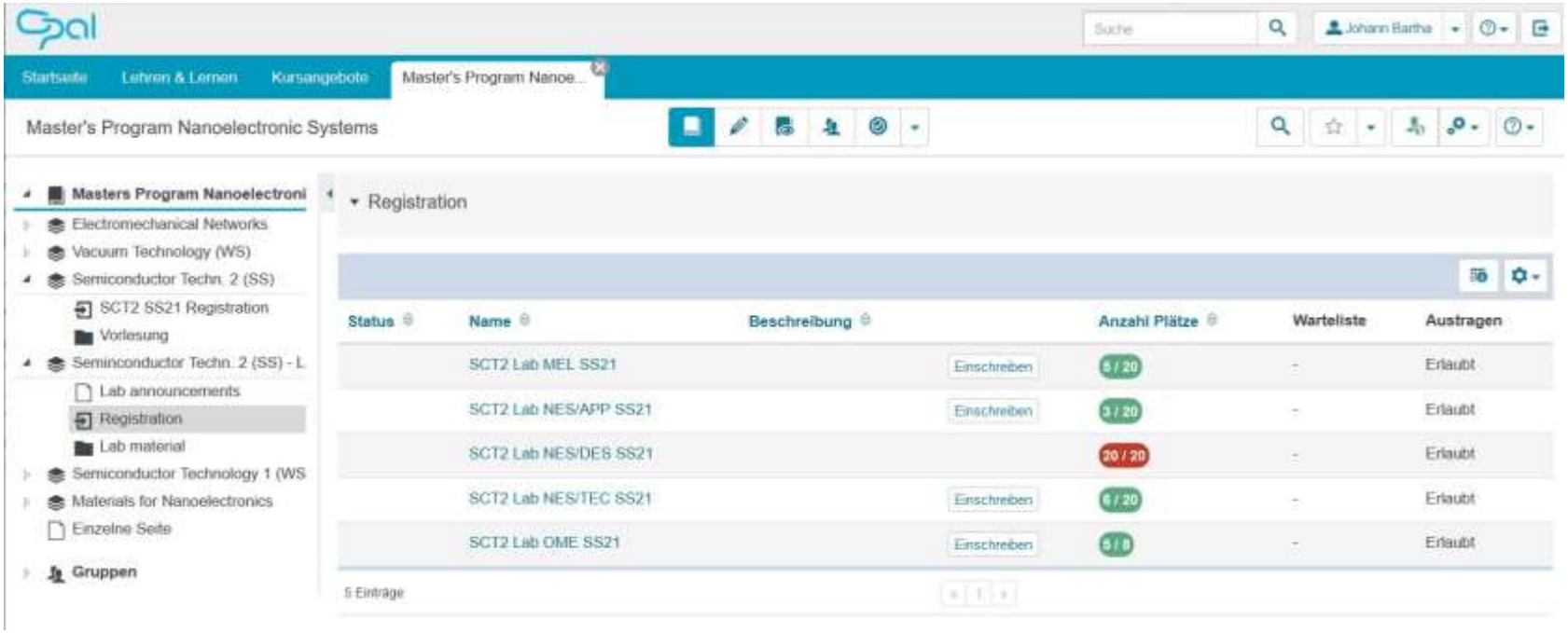
Remarks & organizational stuff:

Lab organization by appointment: Registration

https://bildungsportal.sachsen.de/opal/auth/RepositoryEntry/5690753028/CourseNode/101358303504194



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Wrap up of SCT1 – left over from SCT1

https://cfaed.tu-dresden.de/dma-welcome

Dresden Microelectronics Academy

Welcome | Program | About Us | Sponsors | Links | Contact | DMA Impressions

Production: Jan Luther - http://www.app-bis-web.de

Welcome to the cfaed Summer School: Dresden Microelectronics Academy

Save-the-date: 20-24 September 2021 - please check here regularly for updates on the format and program of DMA'21!

This **one-week** summer school showcases Dresden as Europe's largest microelectronics hub and TU Dresden as the ideal place to study and work!

Who can apply

- advanced students (Master/Diplom students) / PhD students / postdocs of engineering with affinity to micro-/nanoelectronics, e.g., design, technology and test

Remarks & organizational stuff:

OPAL Registration,
where to find the slides

Intro of the lecturer

Lab associated with the lecture – DMA 2021

Books - Exam

Wrap up of SCT1 – left over from SCT1

Topics to begin: Exam and books:

Books:

S.M. Sze,	VLSI Technology	Mc Graw-Hill Inc, 1983/1988
S.M. Sze	Semiconductor Devices Physics and Technology	John Wiley & Sons 1985/2002
Stephen A. Campbell	The Science and Engineering of Microelectronic Fabrication	Oxford University Press 1996
J.D. Plummer, M. Deal, P.B. Griffin	Silicon VLSI Technology	Prentice Hall, 2000
S. Wolf	Silicon Processing for the VLSI Era, Vol. 1-4 Insbesondere Vol. 2, Process Integration	Lattice Press 2000-2004
Sima Dimitrijev	Understanding Semiconductor	Oxford University Press 2000
S. Wolf	Microchip Manufacturing	Lattice Press 2004

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Topics to begin: Exam and books:

https://www.spiedigitallibrary.org/ebooks/PM/Introduction-to-Semiconductor-Manufacturing-Technology-Second-Edition/eISBN-9780819490933/10.1117/3.924283?SSO=1 **Chapter 2, 3, 13 to 15!**

Sima Dimitrijev
Understanding Semiconductor Devices
Oxford University Press 2000
This book contains a CD-ROM with mathlab animations which I will use for demonstration purpose

S. Wolf Microchip Manufacturing
Lattice Press 2004

Exam will be written (120 min.) probably mid to end of July

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Wrap up of SCT1 – left over from SCT1

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Wrap up of SCT1

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Lecture Semiconductor Technology I,
Prof. Dr. J. W. Bartha

Content

1. Introduction

2. Silicon as Substrate Material
2.1 The Silicon Crystal
2.2 Crystal Defects
2.3 Conductivity and Doping
2.4 Si as the most important material of Microelectronics
2.4.1. Fabrication of pure Silicon
2.4.2. Si Wafer Fabrication

3. The Oxidation of Silicon
3.1. Growth model after Deal and Grove
3.2. Dependency on Process parameters
3.3. Oxidation technique
3.4. Stress and Oxidation

4. Lithography
4.1. Process sequence
4.1.1. Negative Resist
4.1.2. Positive Resist
4.2. Multi-Layer Resists
4.3. Image Reversal
4.4. Pattern Enhancement

5. Doping
5.1 Diffusion
5.1.1. ...from an infinite Source
5.1.2. ...from a finite Source
5.1.3. Two step Diffusion
5.1.4. Further Effects
5.1.5. Practical Realization
5.2 Implantation
5.2.1. Projected Range
5.2.2. Implantation - Masks
5.2.3. Channeling
5.2.4. Further Effects
5.2.5. Healing and Activation
5.2.6. Implantation Systems

6. Epitaxy
6.1. Gas Phase Epitaxy
6.1.1. Uniformity
6.1.2. Reaction Kinetics
6.1.3. Mön crystalline vs. Polycrystalline
6.1.4. Pattern Displacement
6.1.5. Doping
6.1.6. Epi-Reactor + Process
6.1.7. Selective Epitaxy
6.2. Molecular Beam Epitaxy

7. Chemical Vapor Deposition CVD
7.1. Poly-Silizium
7.2. Siliconoxide SiO_2
7.3. Silicon nitride Si_3N_4
7.4. PECVD
7.5. Tungsten W

8. Plasma based Deposition and Etch
8.1 Plasma technology
8.1.1. Basic Processes in a Plasma
8.1.2. Energy Absorption by the Electric Field
8.1.3. Plasma Properties
8.1.4. Plasma Generation
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8.2.1. Sputter Deposition of Alloys
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8.2.3. Magnetron Sputtering
8.2.4. Bias-Sputtering
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8.3.1. Sputter-Etching
8.3.2. Plasma Induced Chemical Etching
8.3.3. Reactive Ion Etching
8.3.4. Process Parameters
8.3.5. Plasmatools

https://www.youtube.com/watch?v=UvluuAIiA50&t=283s

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Wrap up of SCT1

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Wrap up of SCT1

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Please watch this clip (~10 min.) and look for the question: Which of the presented technologies in the video were not covered in lecture SCT1?

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Terms and Classification of the manufacturing sequence

"SCT2_1.2" 46:09

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Terms and Classification of the manufacturing sequence

"SCT2_1.2" 46:09

Basic distinction of processing in:

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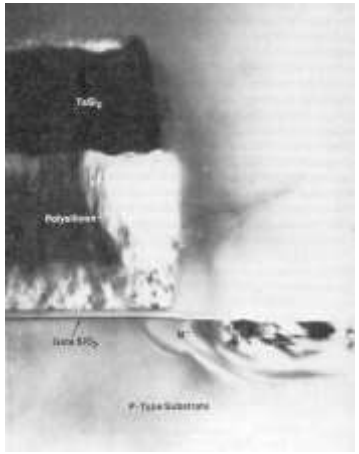
Terms and Classification of the manufacturing sequence

"SCT2_1.2" 46:09



Basic distinction of processing in:

Front end (of line) FEOL

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Terms and Classification of the manufacturing sequence

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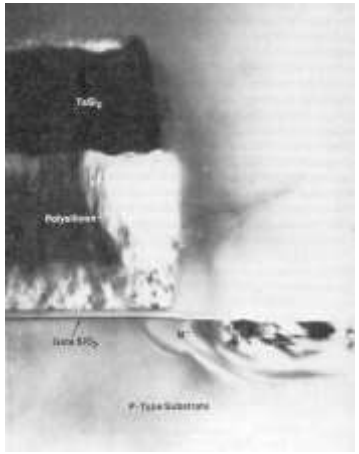
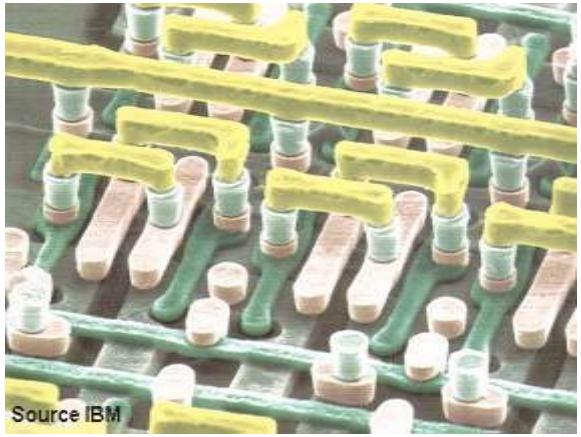


Basic distinction of processing in:

Front end (of line) FEOL

back end of line or interconnect or metallization BEOL



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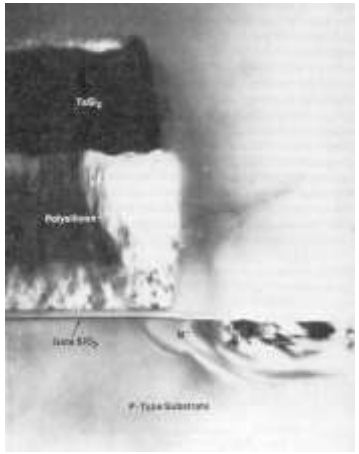
Terms and Classification of the manufacturing sequence

"SCT2_1.2" 46:09

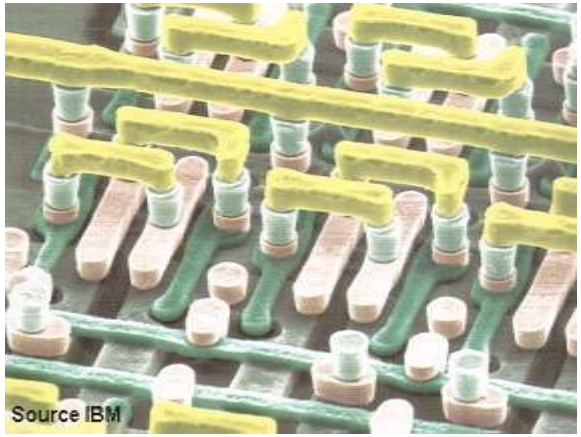


Basic distinction of processing in:

Front end (of line) FEOL

back end of line or interconnect or metallization BEOL

and back end or packaging



Wire Bonding
(Kaijo Corporation)

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Semiconductor Processing

Technology inventory:

Oxidation

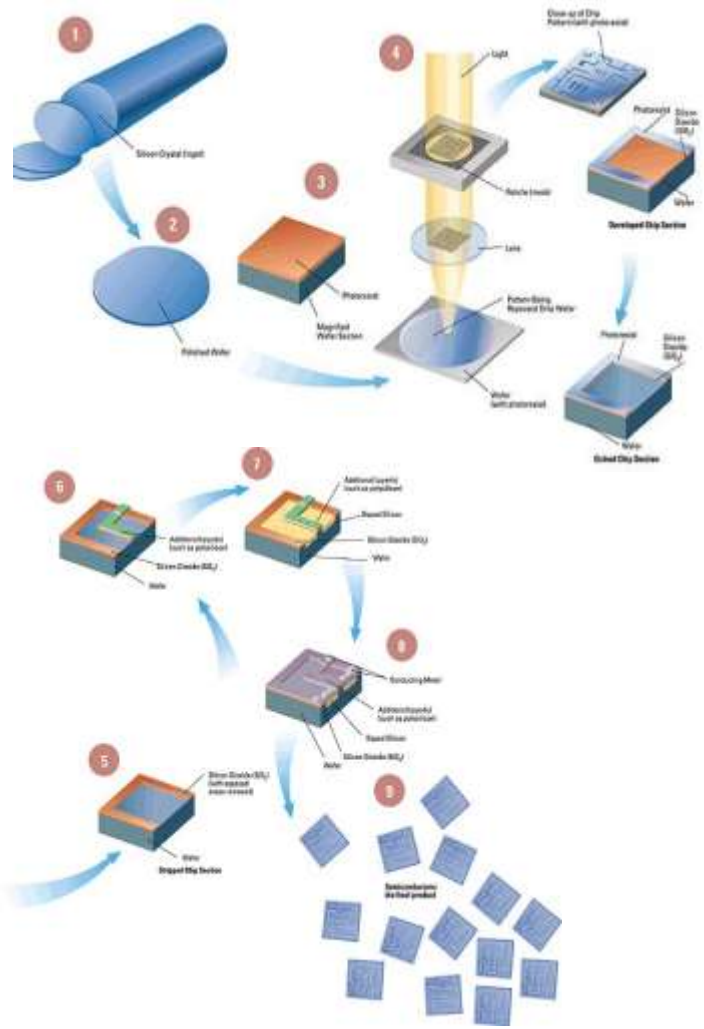
Lithography

Etching (wet & dry, polish)

Doping => Implantation (Diffusion)

Deposition

- Chemical Vapor Deposition (CVD +/- Plasma) - ALD
- Evaporation /
- Sputter Deposition (PVD)
- Electrochem. Depo. (ECD)



http://www.semiconductor.net/info/CA6432169.html

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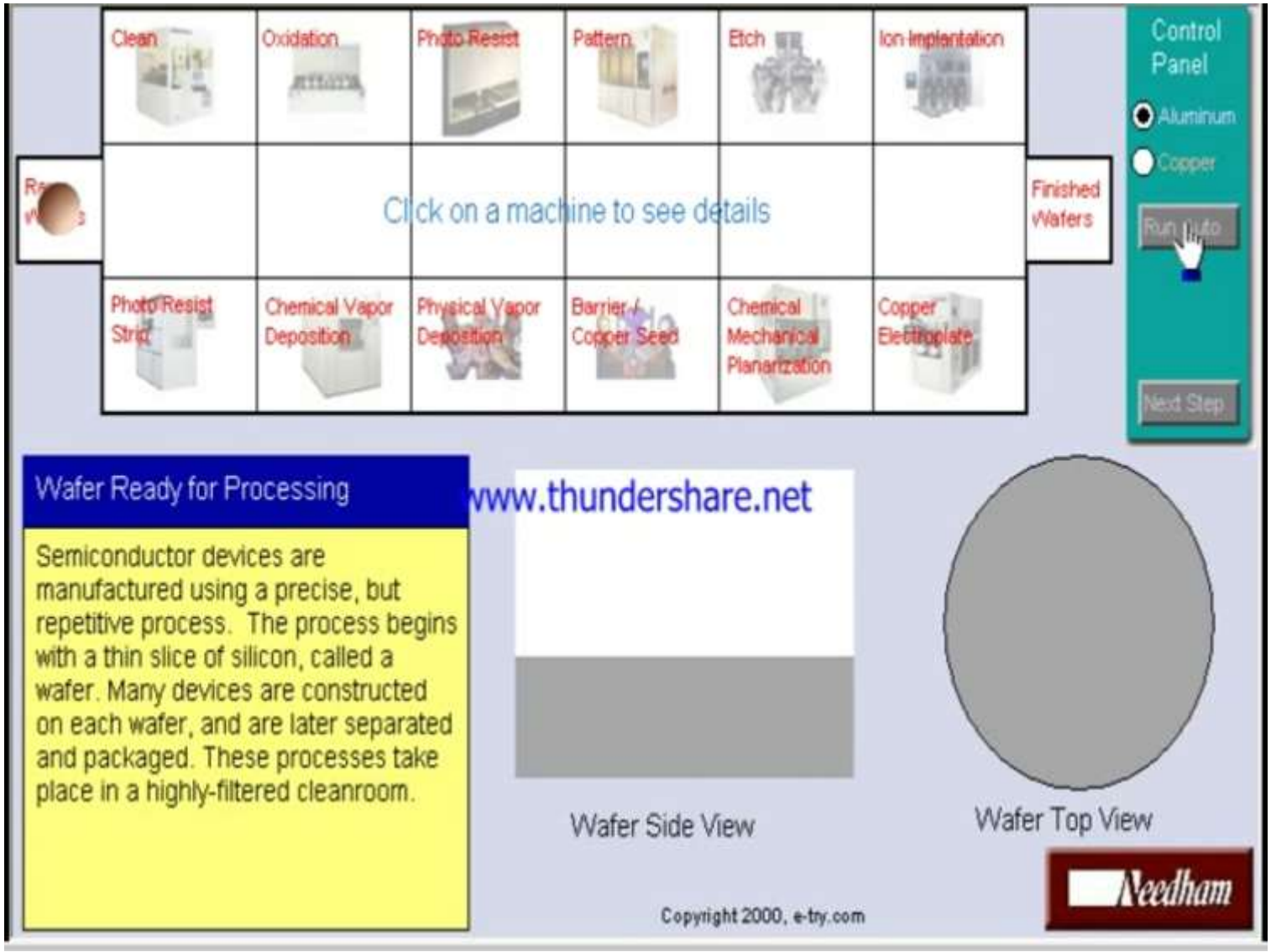

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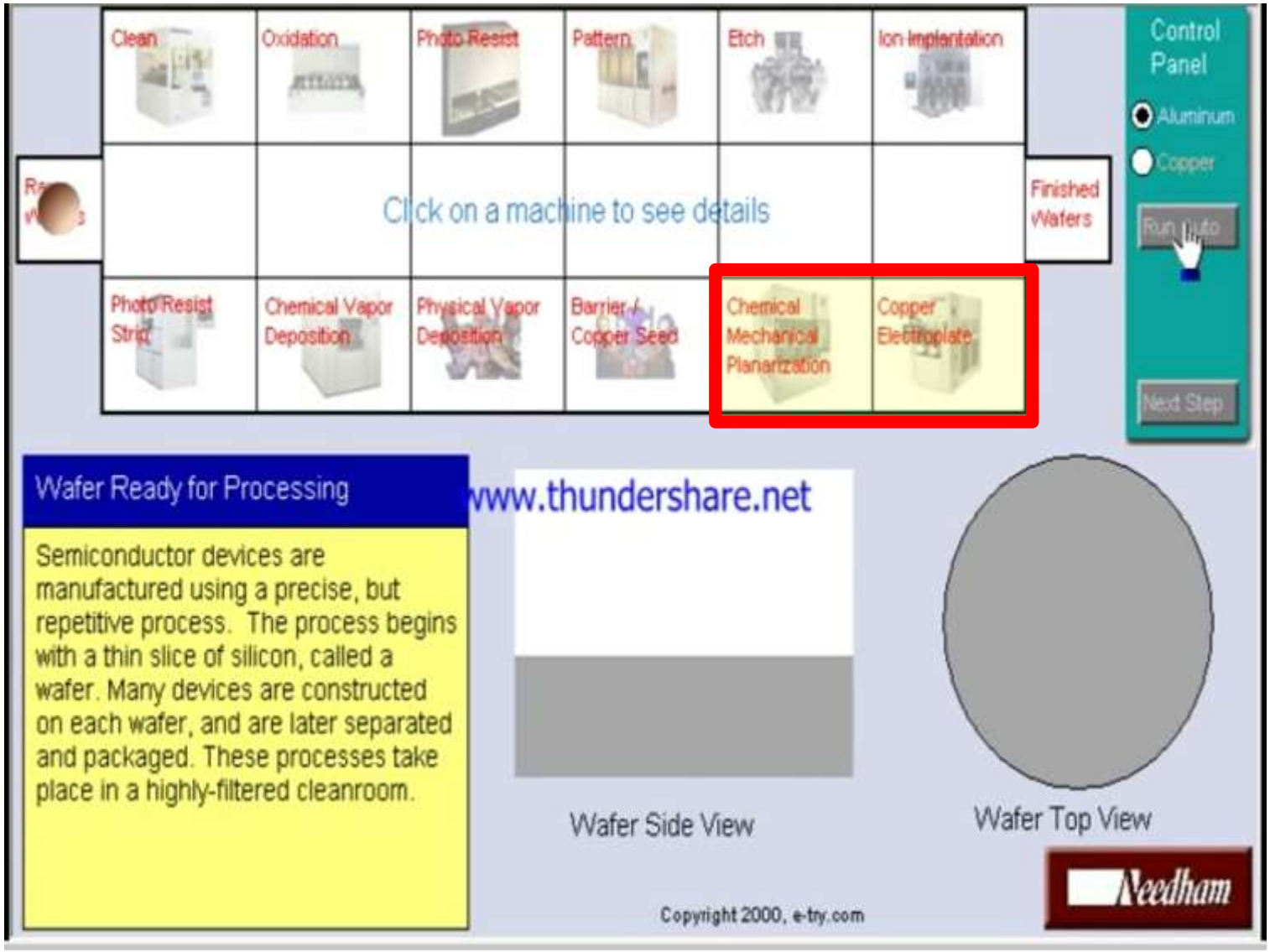

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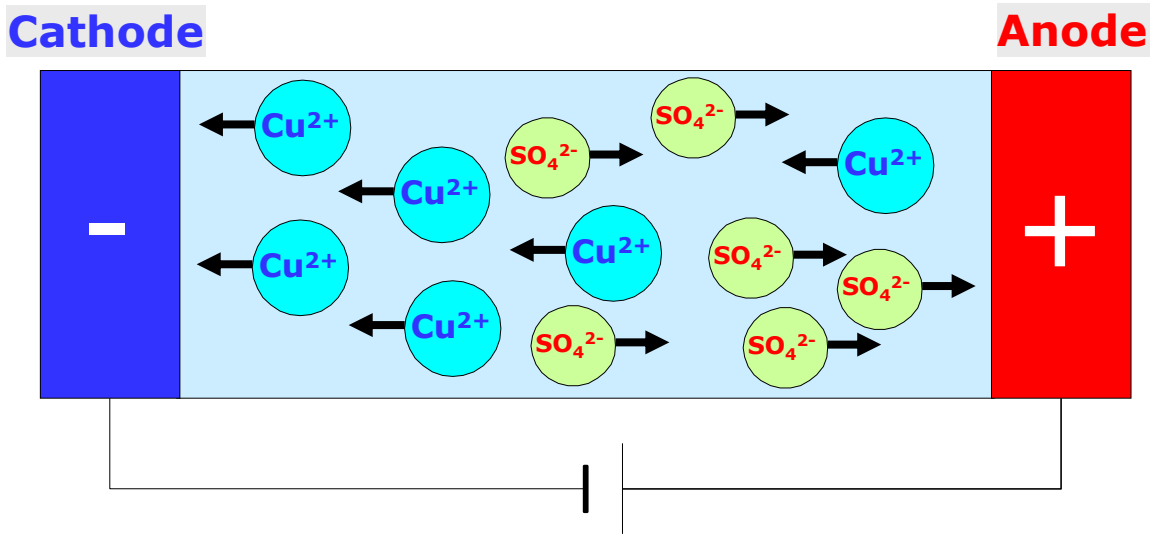
Cu Electroplating

Anode (soluble)	**Cu**	**= $Cu^{2+} + 2e^-$**
Cathode (wafer)	**$Cu^{2+} + 1e^-$**	**= Cu^+**
	$Cu+ + e^-$	**= Cu**



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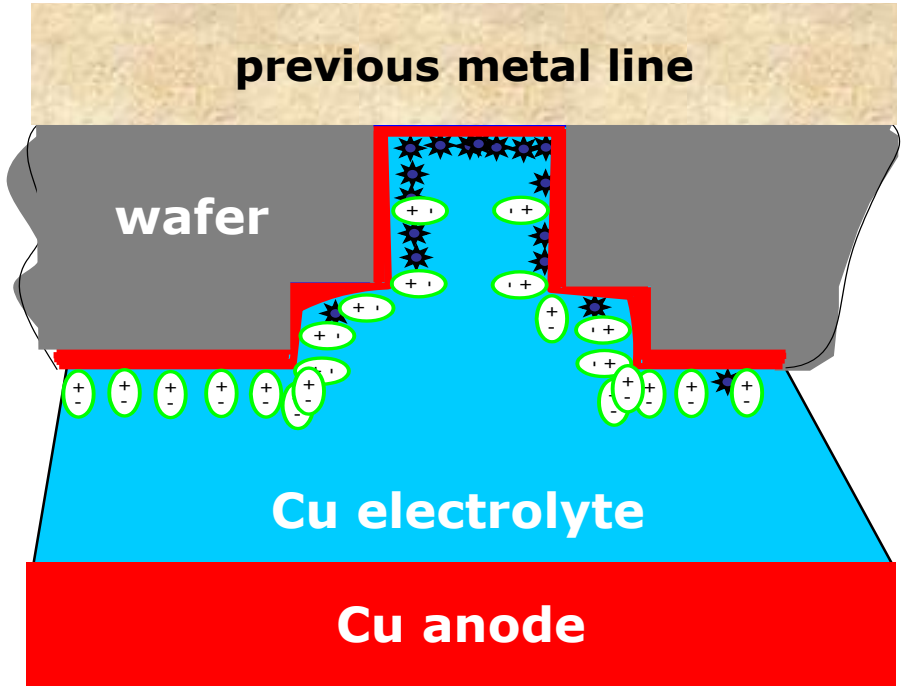
Cu Electroplating - Additives

+ - Suppressor / Leveler

- ✓ absorbed preferentially on the peaks of the substrate and inhibit the deposition on this particular location
- ✓ act as wetting agent
- ✓ long chain polymers

Accelerator

- ✓ absorbed preferred at the bottom of the feature
- ✓ supports deposition in this area
- ✓ sulfonic acid



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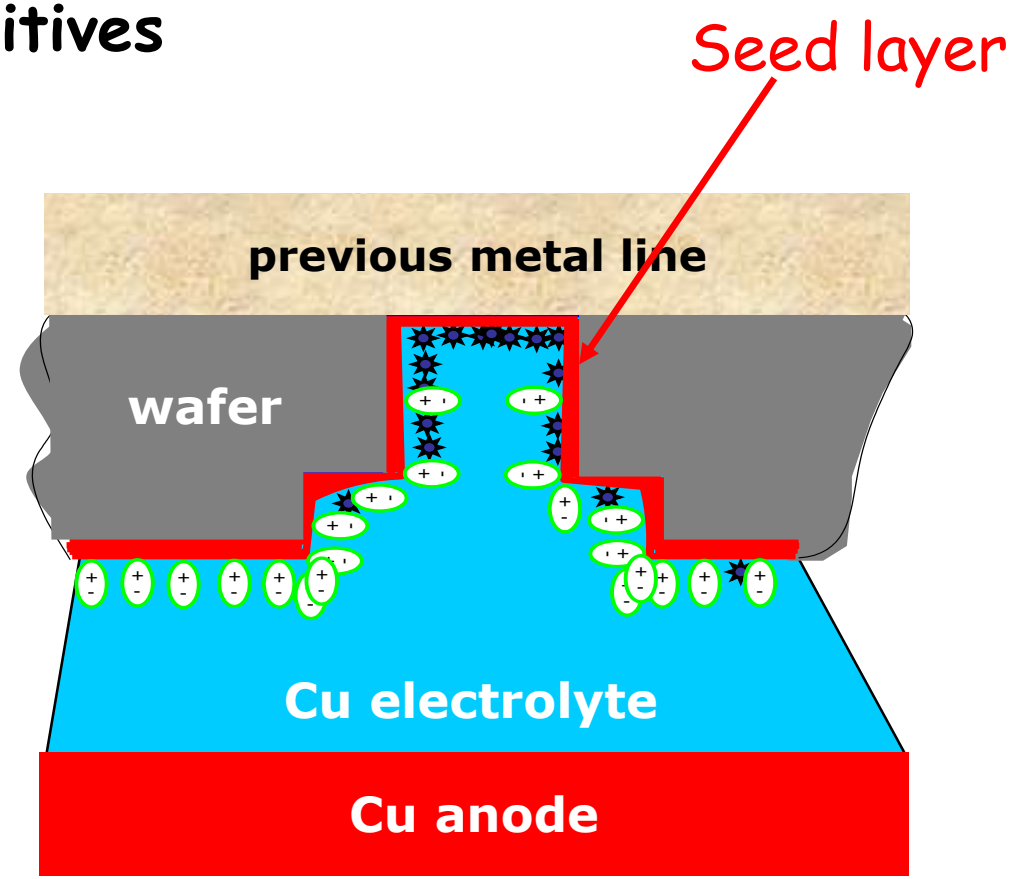

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Superfill:
ECD Application
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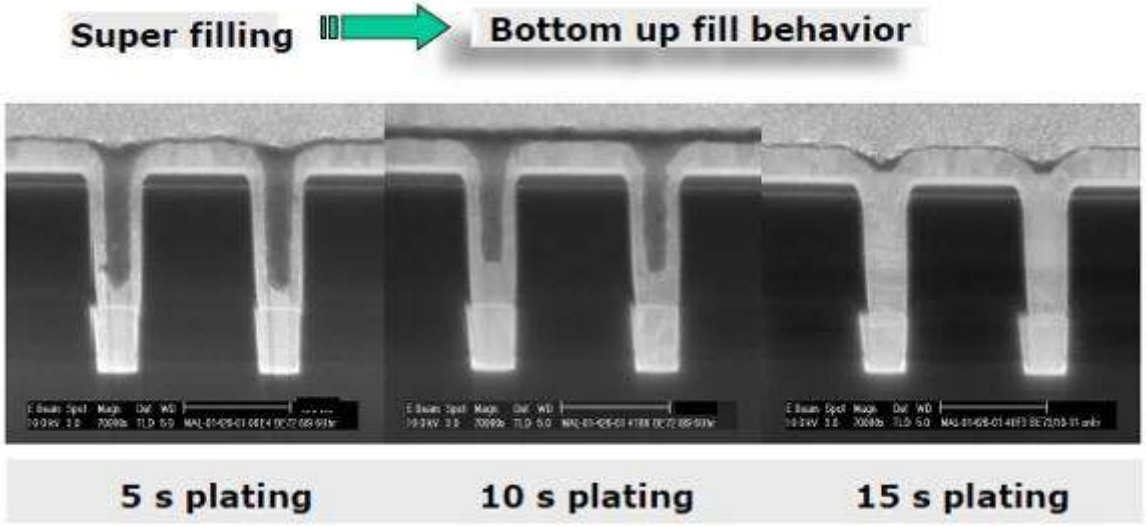

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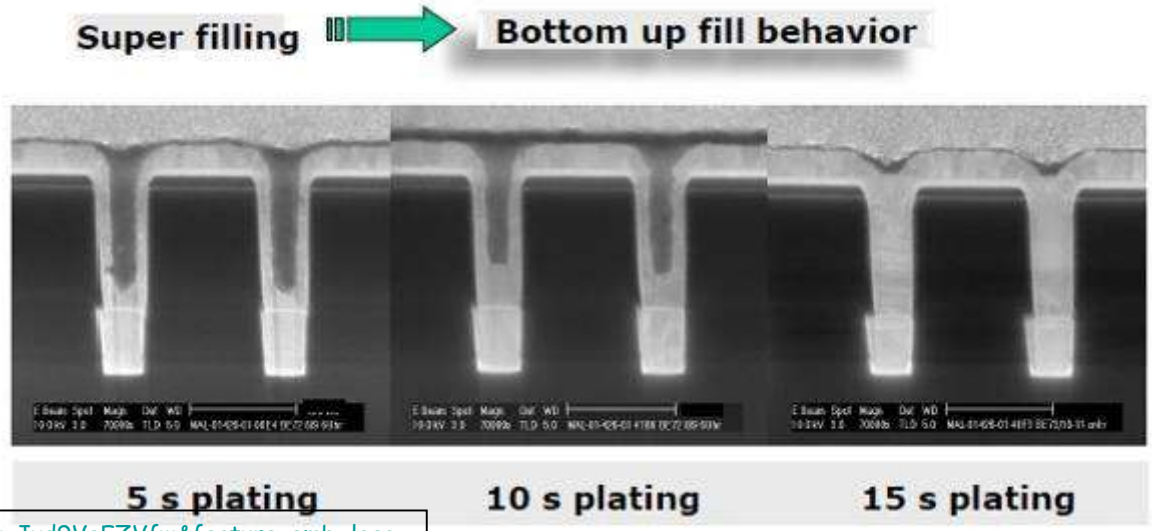

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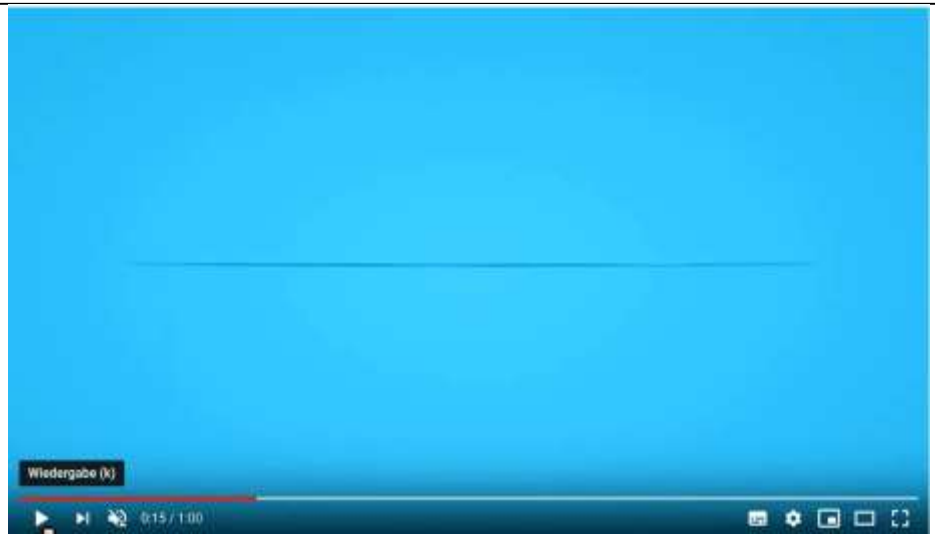

Taken from:
https://www.technic.com/applications/semiconductor/semiconductor-fabrication-packaging-chemistry

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Left over: ECD

Left over: CMP

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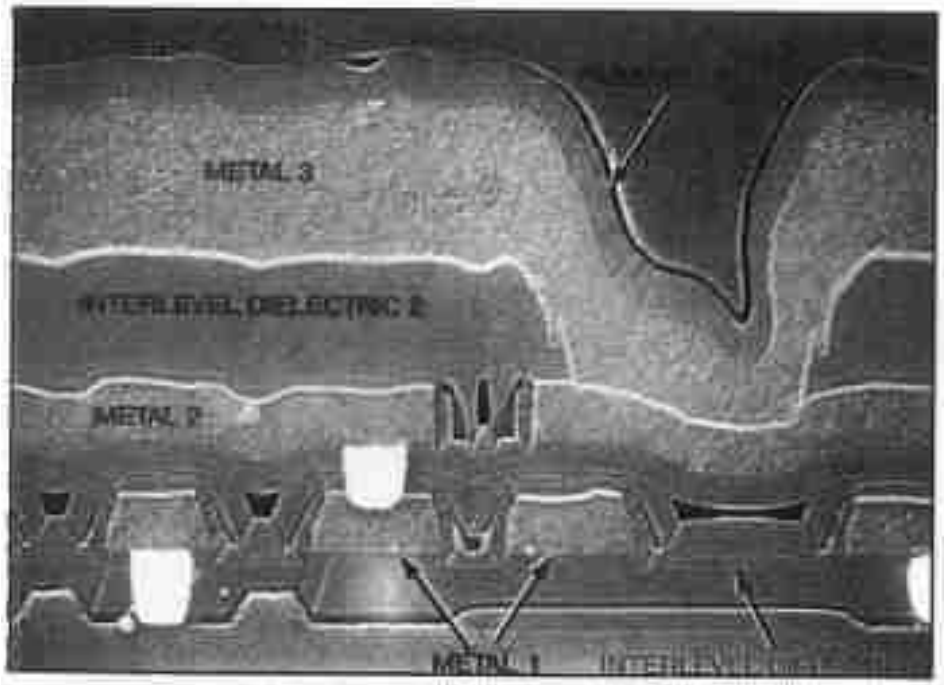
Left over from SCT1 : CMP

In the evolution of IC products the corrugation of surface topologies grew constantly.
On the other hand the CD became constantly smaller. At a certain point in time the technically possible DOF was larger than the corrugation of the surface. =>
It became necessary to create a technology for planarization!



4. Digital Equiment Corp.'s Alpha chip has both tungsten and conventional vias.

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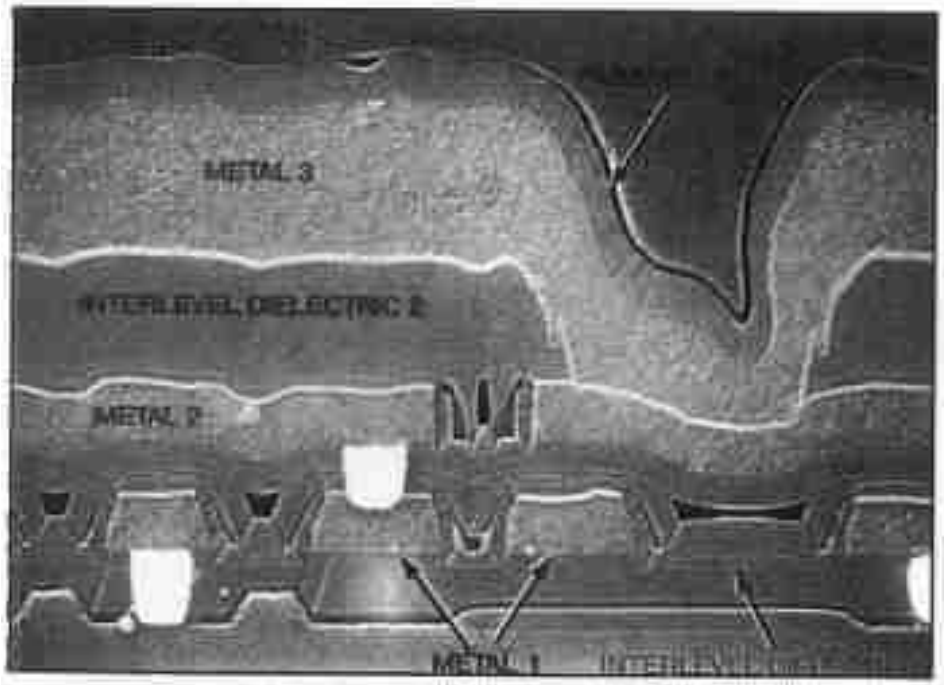

4. Digital Equiment Corp.'s Alpha chip has both tungsten and conventional vias.

CMP := Chemical mechanical Polishing
or Chemical mechanical Planarization

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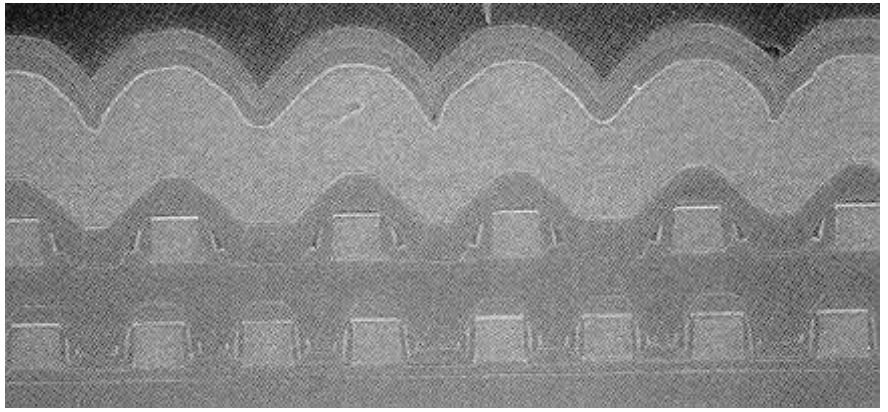
Left over from SCT1 : CMP

Example: Oxide planarization after CVD of insulator layer



Source: IBM JRD

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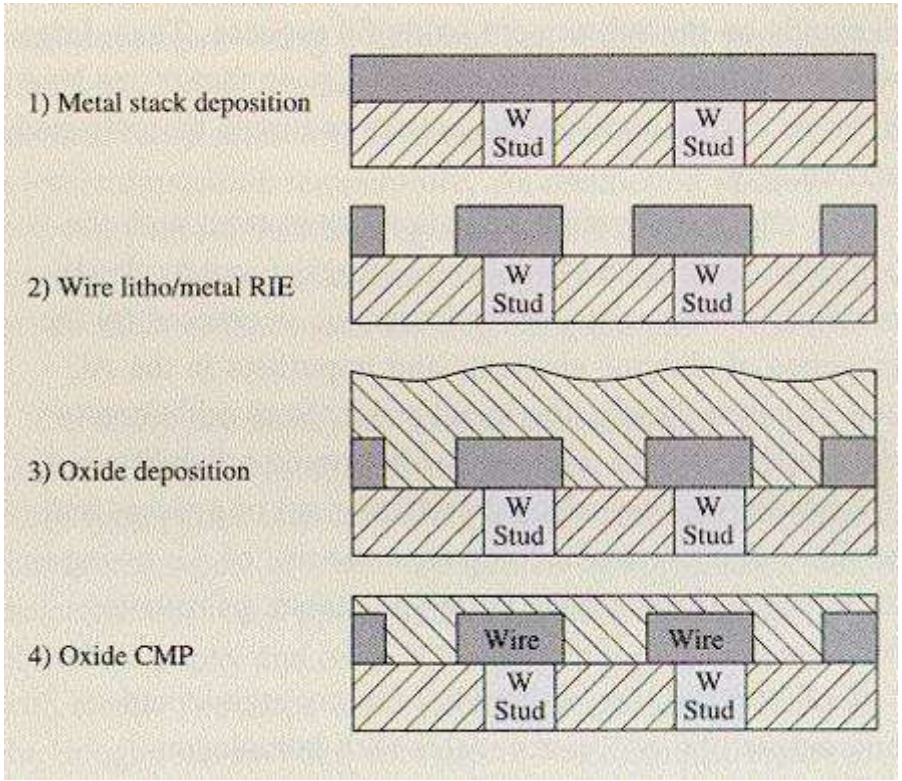

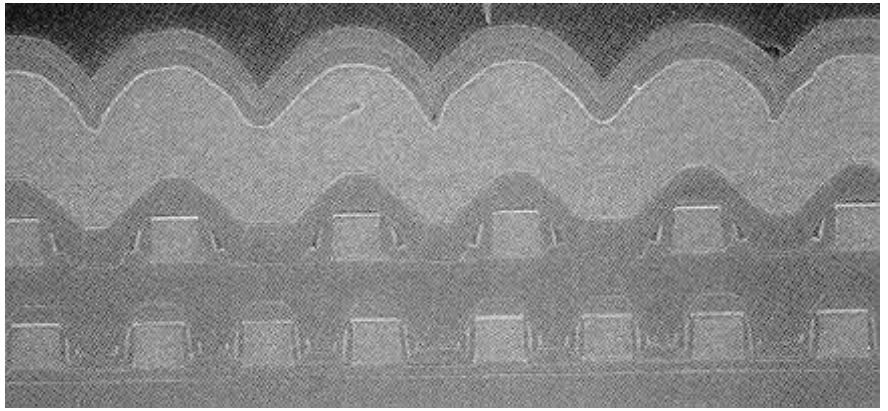

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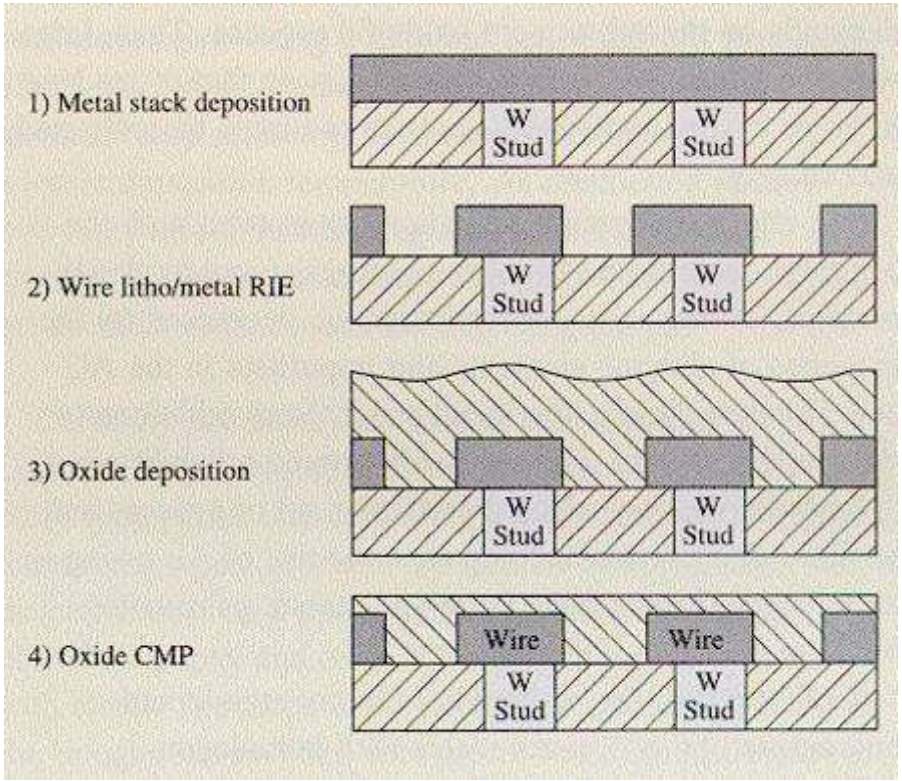

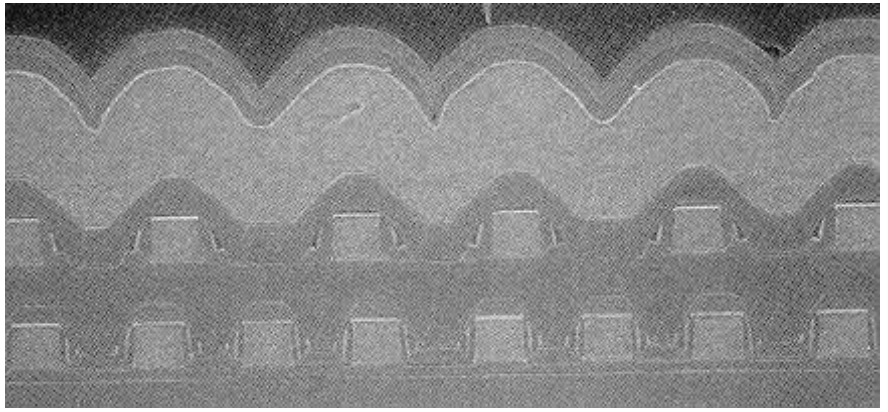

Source: IBM JRD

⇒ CMP of SiO_2 for Planarization
- Stops within the oxide
- Hard to control but
- Does not require selectivity

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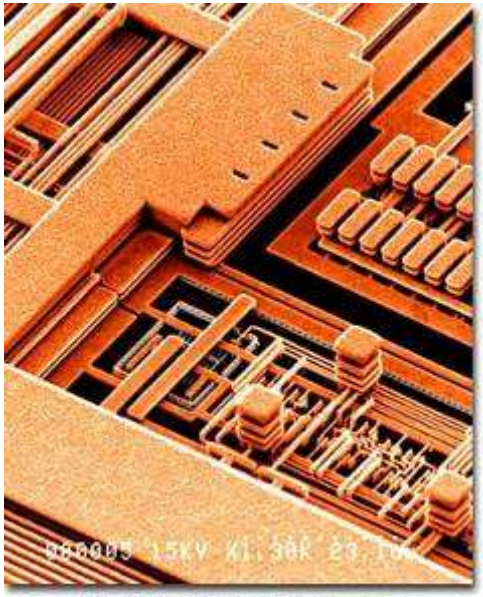
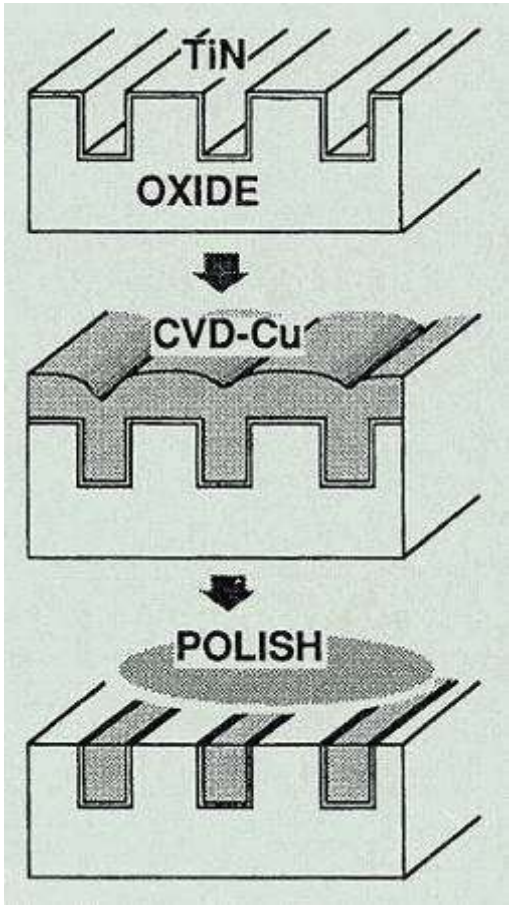
Left over from SCT1 : CMP

The necessity of CMP on Cu results from the unavailability of Cu – RIE!



SEM view of Copper Interconnect
(IBM Microelectronics)

Quelle: IBM JRD



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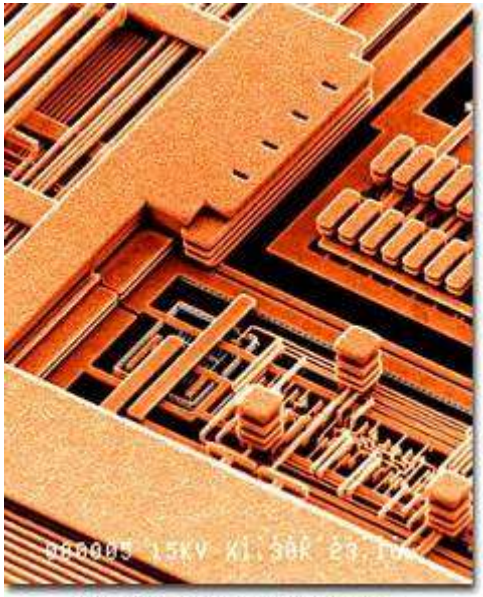

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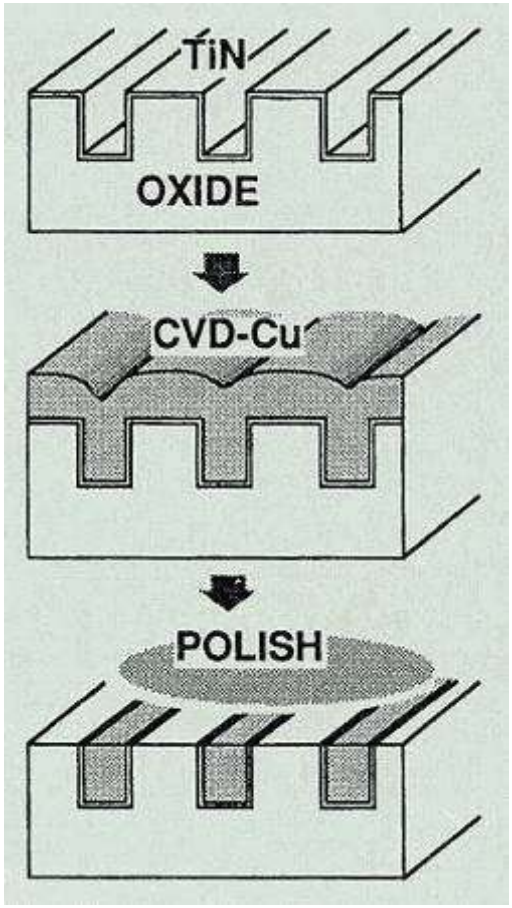

⇒ CMP of Copper must stop at the oxide surface
=> requires selectivity!

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Left over from SCT1 : CMP

Platen rotation	10–100 rpm
Velocity	10–100 cm/s
Down force (applied pressure)	10–50 kPa
Slurry supply rate	50–500 ml/min
Polish rate	100–1000 nm/min
Selectivity	1:1 to 100:1
Uniformity across wafer	10%
Wafer-to-wafer repeatability	10%

Table 16-1

CMP tool parameters and process responses.

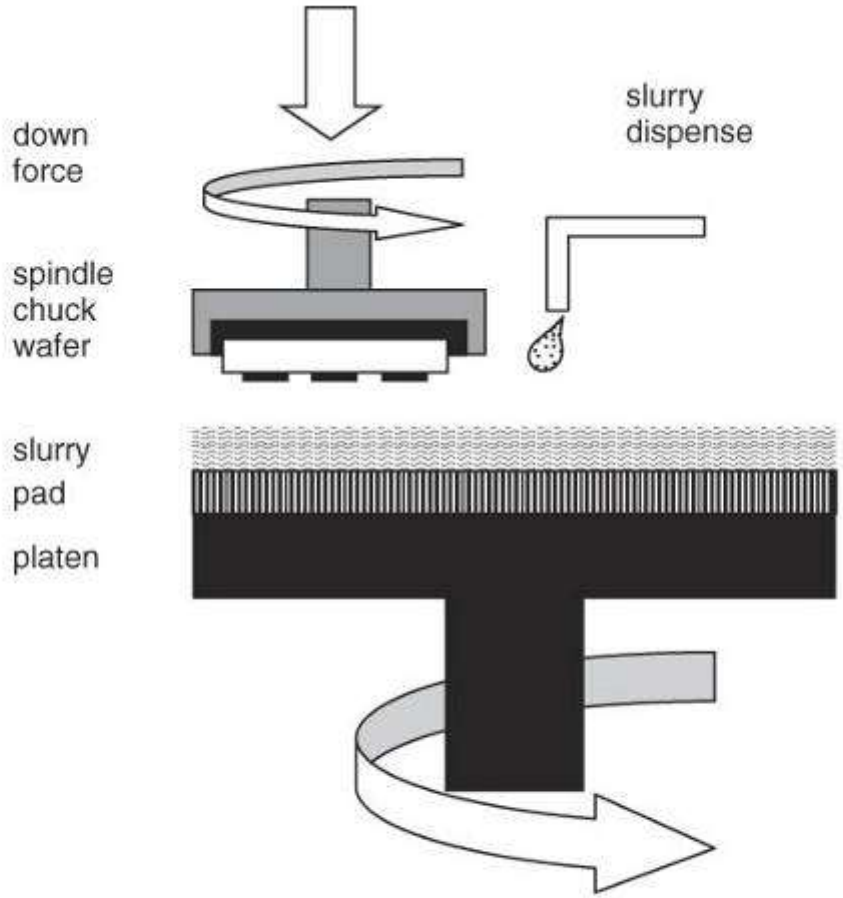

Figure 16-2

Schematic structure of rotary CMP equipment. Wafer is held face down in the spindle chuck.

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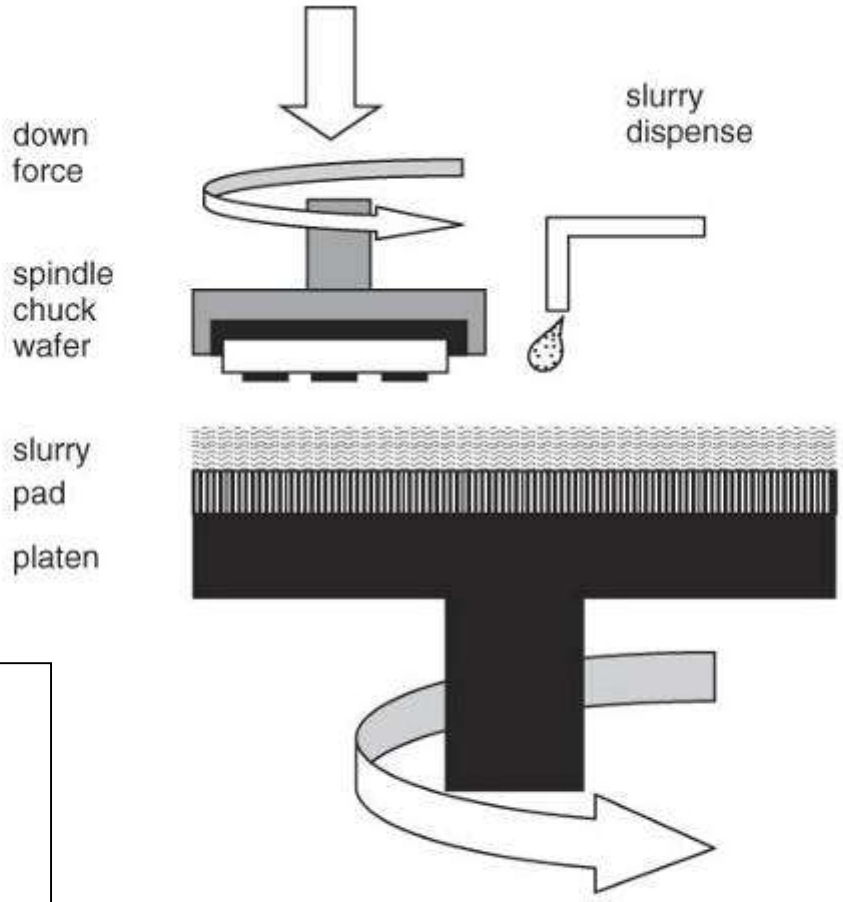
Table 16-1

CMP tool parameters and process responses.



Slurry
is an aquaus suspension that contains besides abrasive particles some chemically active additives.

Figure 16-2

Schematic structure of rotary CMP equipment. Wafer is held face down in the spindle chuck.

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Left over from SCT1 : CMP

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Left over from SCT1 : CMP

Conditioner:

Serves to reestablish the pores in the polish pad to maintain an effective polish result.

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Left over from SCT1 : CMP

Conditioner:

Serves to reestablish the pores in the polish pad to maintain an effective polish result.

https://s3-alliance.com/products/rd-cmp-poli-500-2/

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Fundamental equation of CMP by Preston:

$$R = \Delta H / \Delta t = K_p P (\Delta s / \Delta t)$$

ΔH = change in the height of the surface
P = pad pressure
K_p = Preston coefficient
$(\Delta s / \Delta t)$ = linear velocity of the pad relative to the wafer.

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The removal rate is proportional to (local!) DownForce (Pressure) and Velocity (relative velocity between pad and wafer)

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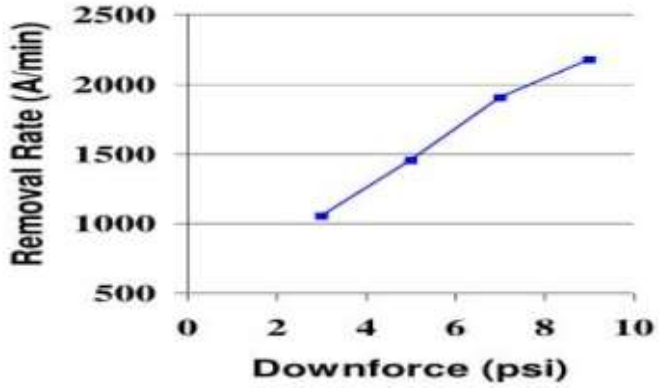

https://www.slideserve.com/nola-harrison/tutorial-on-chemical-mechanical-polishing-cmp

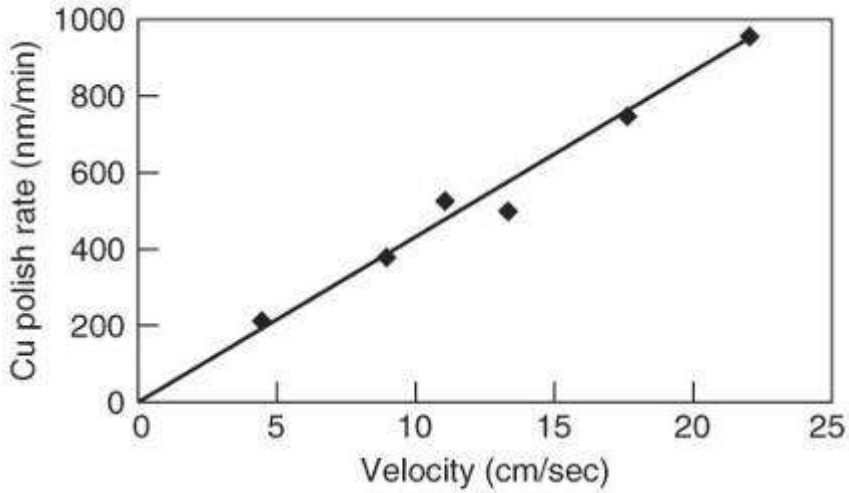

Figure 16-5

Copper polish rate as a function of velocity (15 kPa pressure). Reproduced from Steigerwald *et al.* (1997) by permission of John Wiley & Sons, Ltd.

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The planarization effect is a result of the local difference in pressure between UP (hills in the topography) and DOWN (Valeys in the topography) areas.

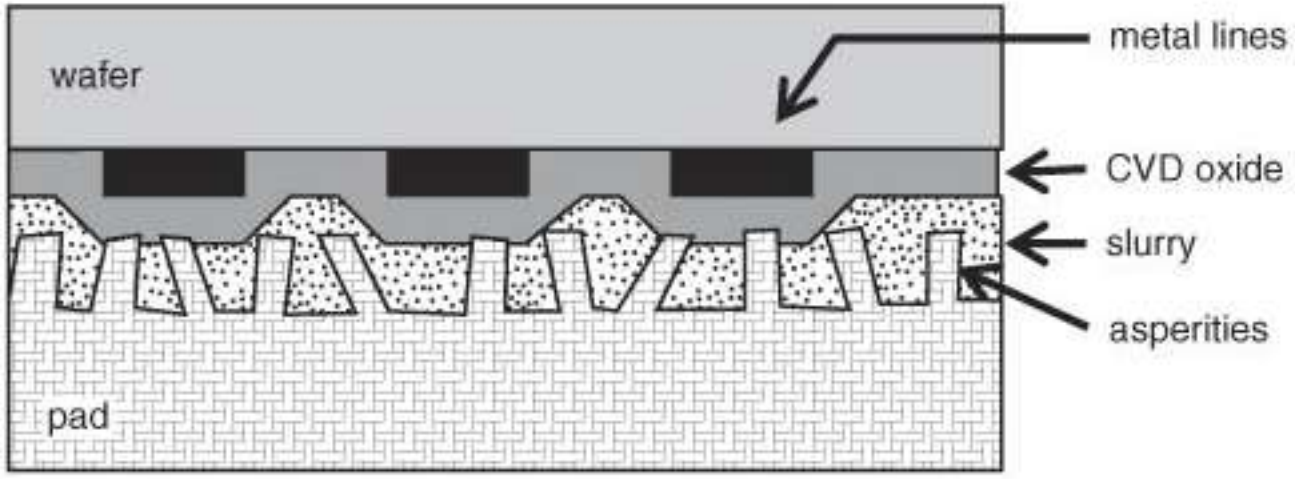

Figure 16-3

Close-up of CMP set-up: the wafer, upside down, is pressed against the pad with slurry in between. Pad asperities make contact with the wafer.

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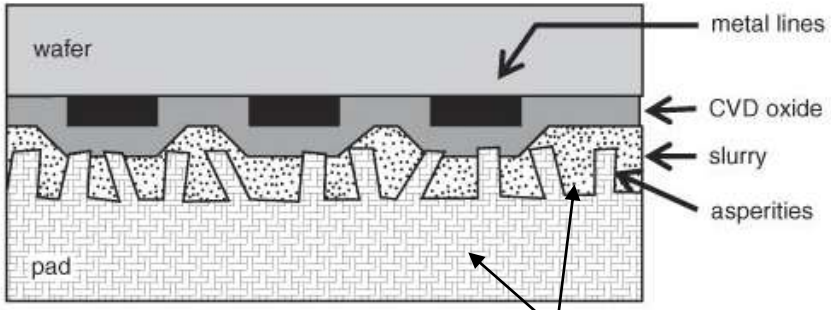

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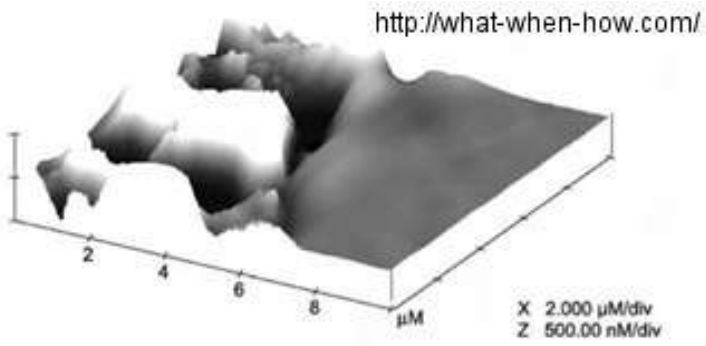
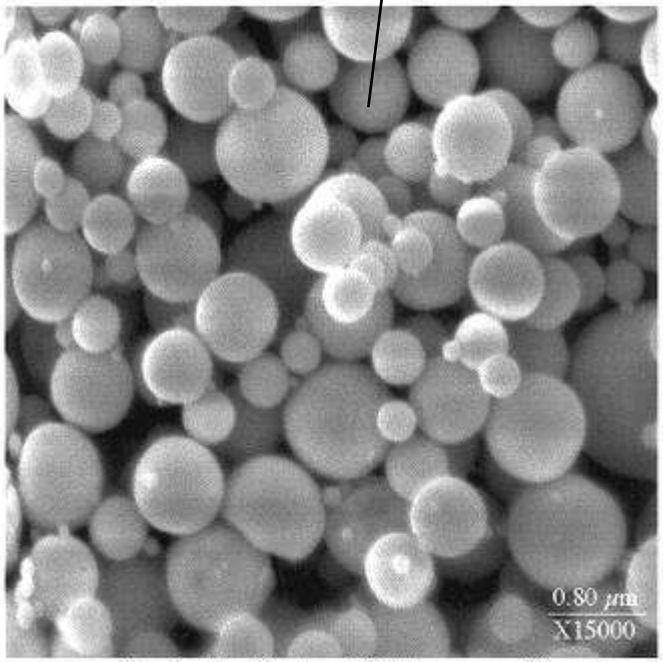
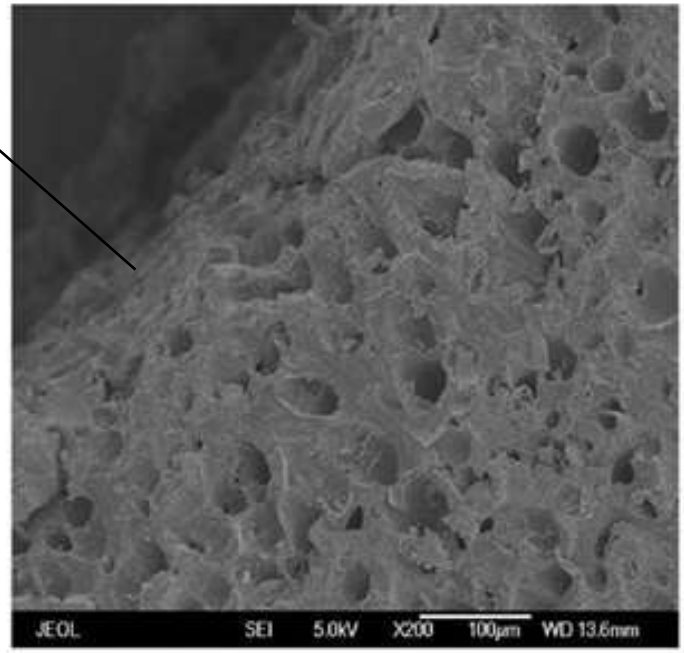


10 x 10 µm Image (z = ± 1 µm)



Superior MicroPowders, LLC (Albuquerque, NM)



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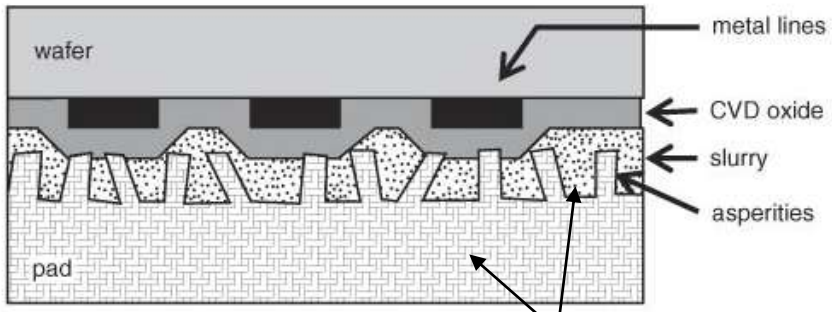

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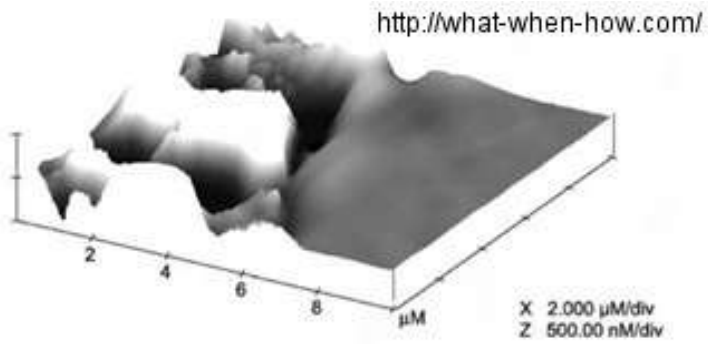
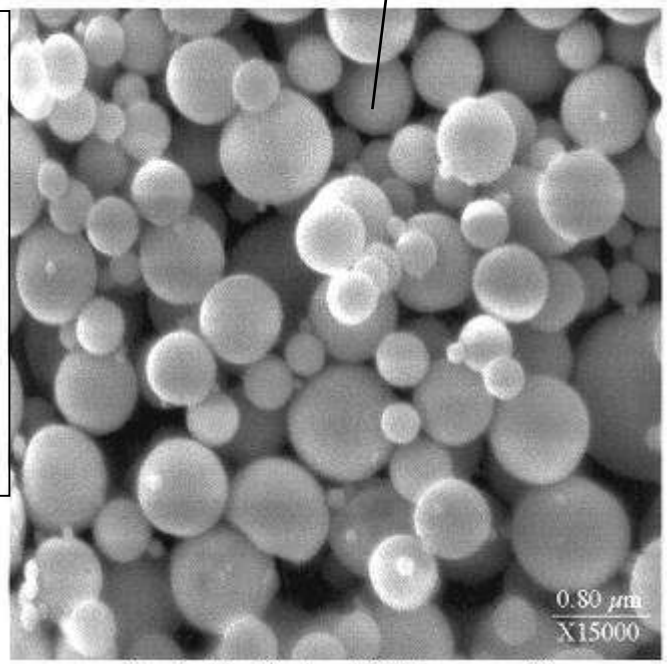


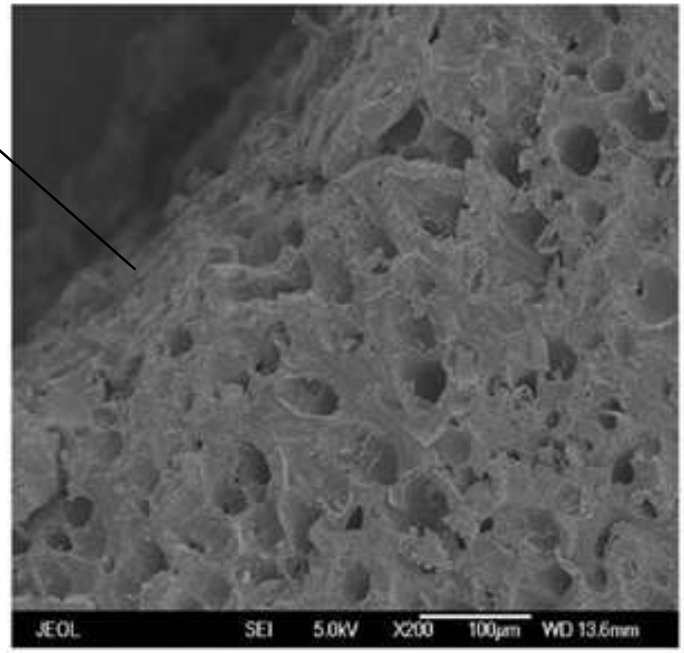
10 x 10 µm Image (z = ± 1 µm)

Abrasive particles in the slurry:

Typical size: 20 – 200 nm



Superior MicroPowders, LLC (Albuquerque, NM)



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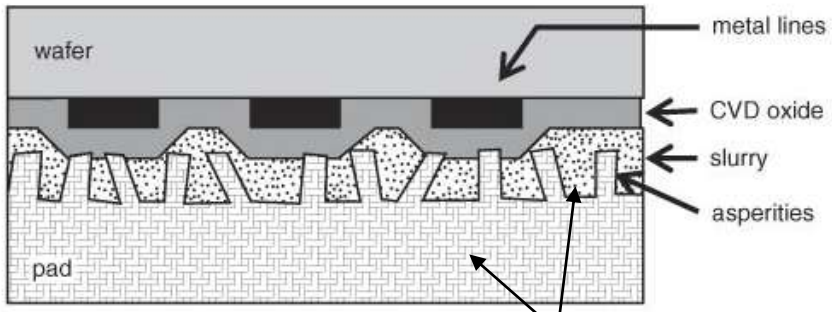

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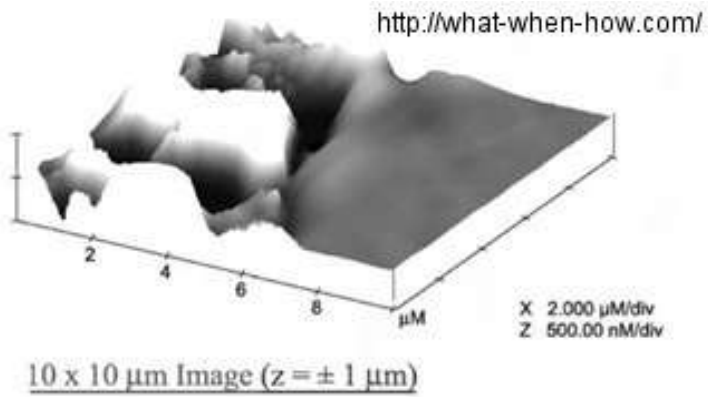

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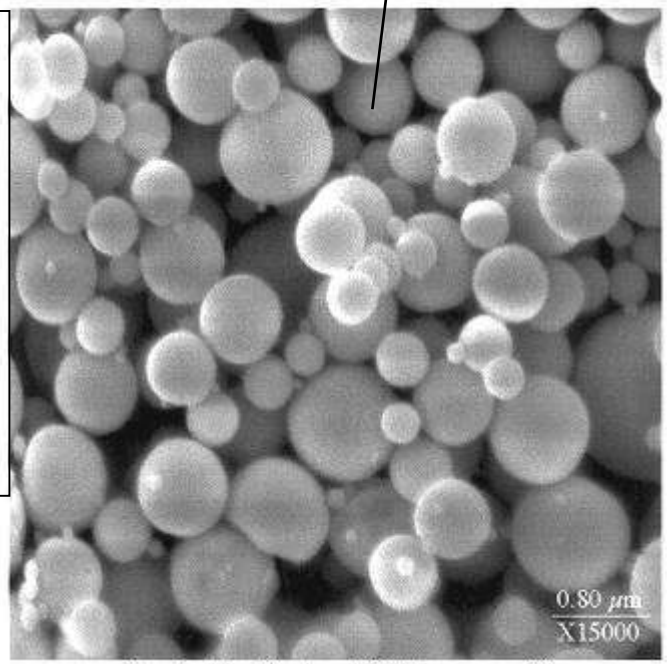
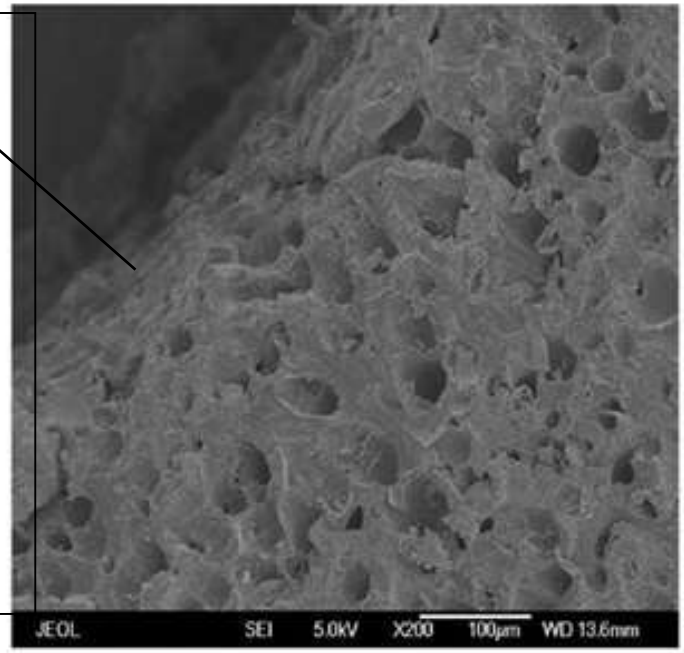


Superior MicroPowders, LLC (Albuquerque, NM)

Poly-urethane Pad delivers asperities.

Typical roughness: 20 – 200 µm



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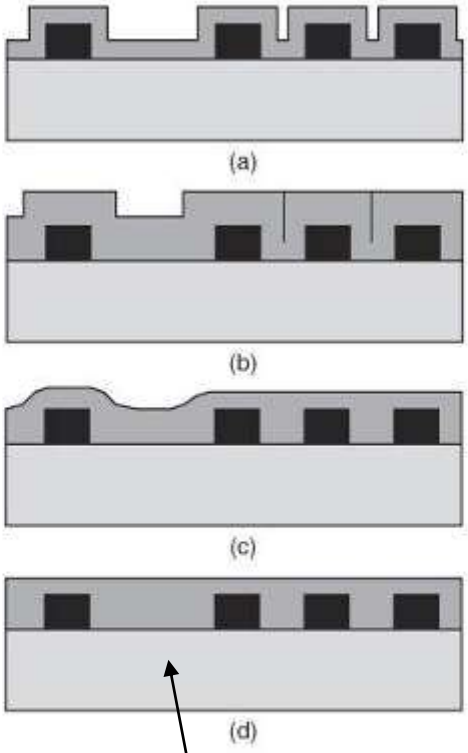
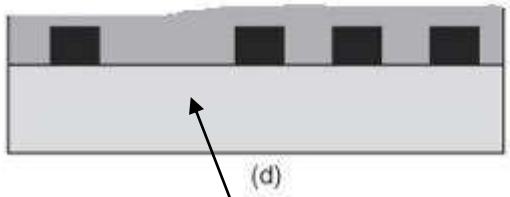


Figure 16-7

Planarization: (a) thin conformal deposition, no planarization; (b) thick conformal deposition, gap filling but no planarization, (c) local planarization by spin-on film; (d) global planarization by CMP of thick conformal deposition.

Ideal planarization



Real case

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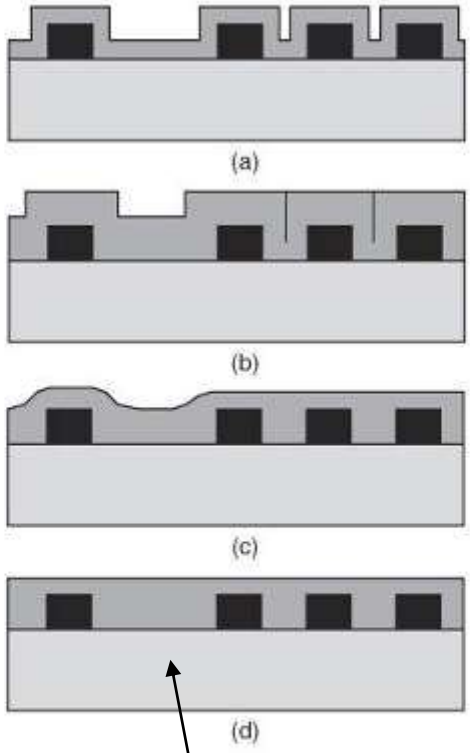


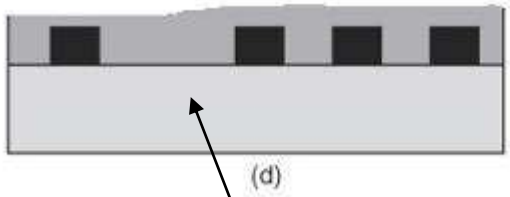
Figure 16-7

Planarization: (a) thin conformal deposition, no planarization; (b) thick conformal deposition, gap filling but no planarization, (c) local planarization by spin-on film; (d) global planarization by CMP of thick conformal deposition.

Ideal planarization

The local removal rate depends on the local pattern density!

A low pattern density causes a high removal rate!
(The global downforce concentrates at only a few contact spots – high local pressure!)



Real case

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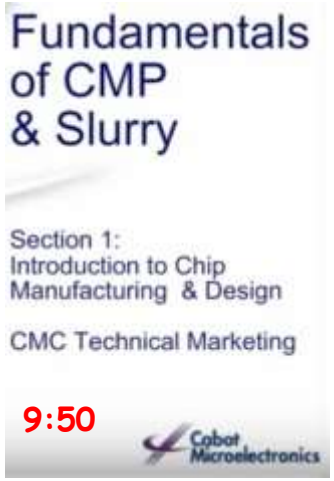
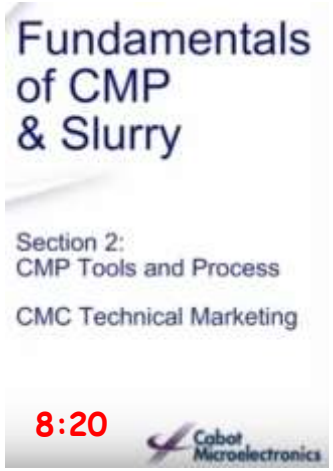
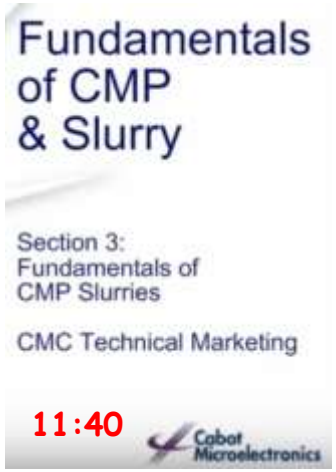
For those, who want to learn more about CMP

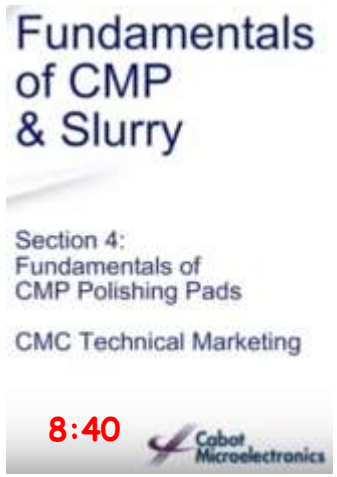
I recommend the following tutorial of a company supplying CMP consumables: Cabot Microelectronics

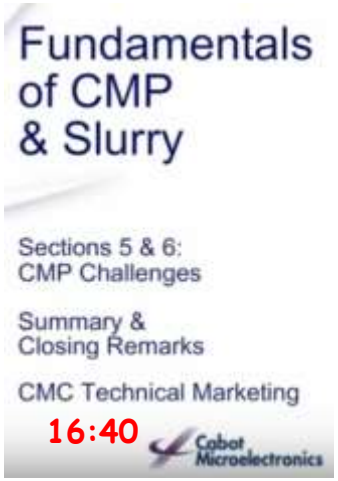
Please click on the section











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Outline

Lecture Semiconductor Technology I,
Prof. Dr. J. W. Bartha

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2. Silicon as Substrate Material
2.1 The Silicon Crystal
2.2 Crystal Defects
2.3 Conductivity and Doping
2.4 Si as the most important material of Microelectronics
2.4.1. Fabrication of pure Silicon
2.4.2. Si Wafer Fabrication

3. The Oxidation of Silicon
3.1. Growth model after Deal and Grove
3.2. Dependency on Process parameters
3.3. Oxidation technique
3.4. Stress and Oxidation

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6.1.2. Reaction Kinetics
6.1.3. Môn crystalline vs. Polycrystalline
6.1.4. Pattern Displacement
6.1.5. Doping
6.1.6. Epi-Reactor + Process
6.1.7. Selective Epitaxy
6.2. Molecular Beam Epitaxy

7. Chemical Vapor Deposition CVD
7.1. Poly-Silizium
7.2. Siliconoxide SiO_2
7.3. Silicon nitride Si_3N_4
7.4. PECVD
7.5. Tungsten W

8. Plasma based Deposition and Etch
8.1 Plasma technology
8.1.1. Basic Processes in a Plasma
8.1.2. Energy Absorption by the Electric Field
8.1.3. Plasma Properties
8.1.4. Plasma Generation
8.2 Sputter Deposition
8.2.1. Sputter Deposition of Alloys
8.2.2. Reactive Sputtering
8.2.3. Magnetron Sputtering
8.2.4. Bias-Sputtering
8.3 Plasma induced Etching
8.3.1. Sputter-Etching
8.3.2. Plasma Induced Chemical Etching
8.3.3. Reactive Ion Etching
8.3.4. Process Parameters
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ECD + CMP

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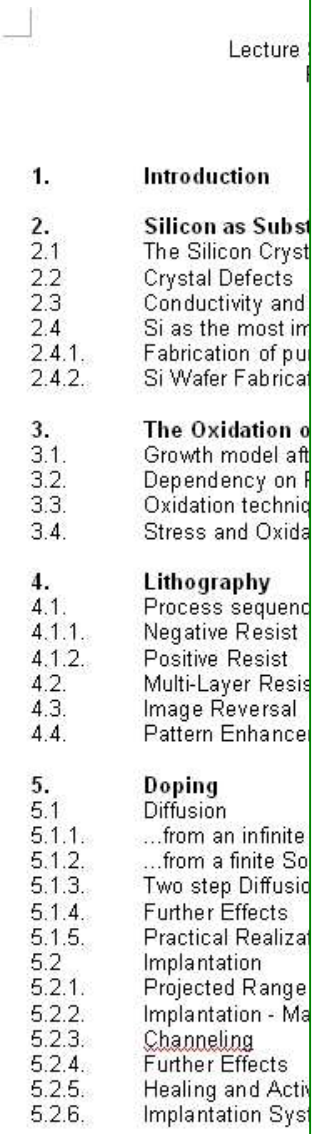

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    2.Structure of a MOSFET
    3.I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
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    2. Channel-Stop & LOCOS Technology
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        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
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        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
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        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

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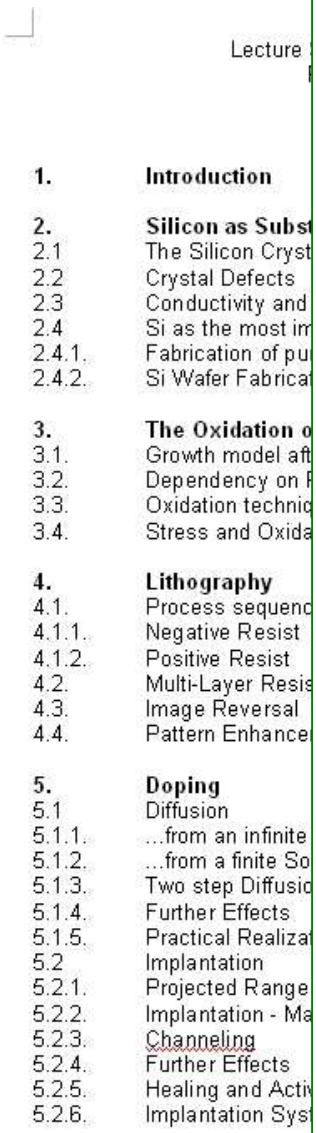

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http://www.computerhistory.org/siliconengine/timeline/

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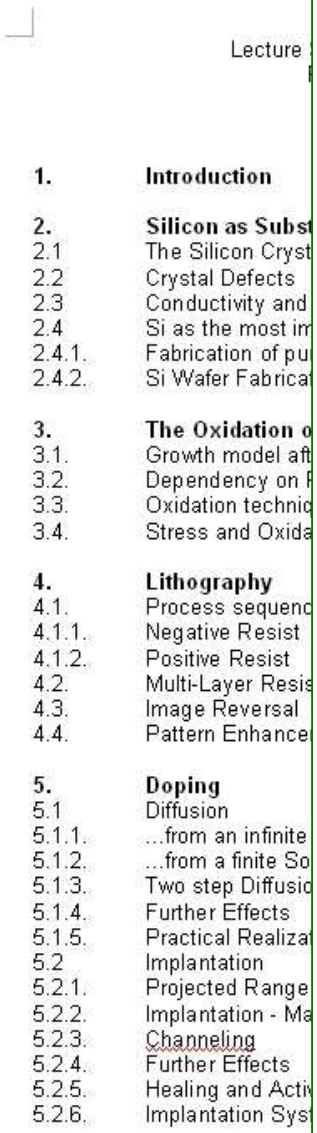

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        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

SC-Basics

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http://www.computerhistory.org/siliconengine/timeline/

»Wissen schafft Brücken.«

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