TECHNISCHE UNIVERSITÄT DRESDEN

The hyperlinks to the video streams in this virtual lecture are marked by the Video Campus Sachsen Logo. To watch them you need to be logged on at the host: VCS. Please click on: https://videocampus.sachsen.de/login select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 - Process Integration

3. Web-based virtual Lecture: April 29 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here

This document including the contained video streams is only available to students of the lecture „Semiconductor Technology 2“ at TU-Dresden.
It must not be copied and published outside of TUD!
It is intended for
TUD internal use only!

Outline

TECHNISCHE UNIVERSITÄT DRESDEN

Lecture Semiconductor Technology I,
Prof. Dr. J. W. Bartha

Content

1. Introduction

2. Silicon as Substrate Material
2.1 The Silicon Crystal
2.2 Crystal Defects
2.3 Conductivity and Doping
2.4 Si as the most important material of Microelectronics
2.4.1. Fabrication of pure Silicon
2.4.2. Si Wafer Fabrication

3. The Oxidation of Silicon
3.1. Growth model after Deal and Grove
3.2. Dependency on Process parameters
3.3. Oxidation technique
3.4. Stress and Oxidation

4. Lithography
4.1. Process sequence
4.1.1. Negative Resist
4.1.2. Positive Resist
4.2. Multi-Layer Resists
4.3. Image Reversal
4.4. Pattern Enhancement

5. Doping
5.1 Diffusion
5.1.1. ...from an infinite Source
5.1.2. ...from a finite Source
5.1.3. Two step Diffusion
5.1.4. Further Effects
5.1.5. Practical Realization
5.2 Implantation
5.2.1. Projected Range
5.2.2. Implantation - Masks
5.2.3. Channeling
5.2.4. Further Effects
5.2.5. Healing and Activation
5.2.6. Implantation Systems

6. Epitaxy
6.1. Gas Phase Epitaxy
6.1.1. Uniformity
6.1.2. Reaction Kinetics
6.1.3. Môn crystalline vs. Polycrystalline
6.1.4. Pattern Displacement
6.1.5. Doping
6.1.6. Epi-Reactor + Process
6.1.7. Selective Epitaxy
6.2. Molecular Beam Epitaxy

7. Chemical Vapor Deposition CVD
7.1. Poly-Silizium
7.2. Siliconoxide SiO_2
7.3. Silicon nitride Si_3N_4
7.4. PECVD
7.5. Tungsten W
7.6 ALD

8. Plasma based Deposition and Etch
8.1 Plasma technology
8.1.1. Basic Processes in a Plasma
8.1.2. Energy Absorption by the Electric Field
8.1.3. Plasma Properties
8.1.4. Plasma Generation
8.2 Sputter Deposition
8.2.1. Sputter Deposition of Alloys
8.2.2. Reactive Sputtering
8.2.3. Magnetron Sputtering
8.2.4. Bias-Sputtering
8.3 Plasma induced Etching
8.3.1. Sputter-Etching
8.3.2. Plasma Induced Chemical Etching
8.3.3. Reactive Ion Etching
8.3.4. Process Parameters
8.3.5. Plasmatools

ECD + CMP

Outline

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
    1. MOS Structure, MOS Capacitor
    2. Structure of a MOSFET
    3. I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1. Process sequence of N-MOSFET in Metal Gate
    2. From inverter to memory cell
    3. SRAM in NMOS Metal Gate
    4. The threshold voltage of the MOSFET
        1. Parasitic FET
        2. Enhancement/Depletion Transistor
        3. N-MOS Logic by E/D Transitors
        4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1. Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1. Example: Process flow of E/D SiGate LOCOS Inverter
        2. LOCOS Variation
        3. Shallow Trench Isolation
    3. Lightly doped drain
    4. SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4. Transition to CMOS Technology
    1. MOS Transistor Types
    2. CMOS Inverter
        1. Consideration NMOS E/D Inverter
        2. Comparison CMOS Inverter
    3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1. Scaling
        1. Challenges
        2. Material Equivalent Scaling
        3. Further Concepts

Lect

1. Introduction

2. Silicon as S
2.1 The Silicon C
2.2 Crystal Defec
2.3 Conductivity
2.4 Si as the mo
2.4.1. Fabrication o
2.4.2. Si Wafer Fab

3. The Oxidati
3.1. Growth mode
3.2. Dependency
3.3. Oxidation tec
3.4. Stress and O

4. Lithography
4.1. Process seq
4.1.1. Negative Res
4.1.2. Positive Resi
4.2. Multi-Layer R
4.3. Image Rever
4.4. Pattern Enha

5. Doping
5.1 Diffusion
5.1.1. ...from an infi
5.1.2. ...from a finite
5.1.3. Two step Diff
5.1.4. Further Effec
5.1.5. Practical Rea
5.2 Implantation
5.2.1. Projected Ra
5.2.2. Implantation
5.2.3. Channeling
5.2.4. Further Effec
5.2.5. Healing and
5.2.6. Implantation

http://www.computerhistory.org/siliconengine/timeline/

Outline

SC-Basics

Lect

1. Introduction
2. Silicon as S
2.1 The Silicon C
2.2 Crystal Defec
2.3 Conductivity
2.4 Si as the mo
2.4.1. Fabrication o
2.4.2. Si Wafer Fab
3. The Oxidati
3.1. Growth mode
3.2. Dependency
3.3. Oxidation tec
3.4. Stress and O
4. Lithography
4.1. Process sequ
4.1.1. Negative Res
4.1.2. Positive Resi
4.2. Multi-Layer R
4.3. Image Rever
4.4. Pattern Enha
5. Doping
5.1 Diffusion
5.1.1. ...from an infi
5.1.2. ...from a finite
5.1.3. Two step Diff
5.1.4. Further Effec
5.1.5. Practical Rea
5.2 Implantation
5.2.1. Projected Ra
5.2.2. Implantation
5.2.3. Channeling
5.2.4. Further Effec
5.2.5. Healing and
5.2.6. Implantation

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
    1. MOS Structure, MOS Capacitor
    2. Structure of a MOSFET
    3. I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1. Process sequence of N-MOSFET in Metal Gate
    2. From inverter to memory cell
    3. SRAM in NMOS Metal Gate
    4. The threshold voltage of the MOSFET
        1. Parasitic FET
        2. Enhancement/Depletion Transistor
        3. N-MOS Logic by E/D Transitors
        4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1. Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1. Example: Process flow of E/D SiGate LOCOS Inverter
        2. LOCOS Variation
        3. Shallow Trench Isolation
    3. Lightly doped drain
    4. SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4. Transition to CMOS Technology
    1. MOS Transistor Types
    2. CMOS Inverter
        1. Consideration NMOS E/D Inverter
        2. Comparison CMOS Inverter
    3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1. Scaling
        1. Challenges
        2. Material Equivalent Scaling
        3. Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!

TECHNISCHE UNIVERSITÄT DRESDEN

Outline

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
   1. MOS Structure, MOS Capacitor
   2. Structure of a MOSFET
   3. I/V behaviour
2. Circuits in Metal-Gate FET Technology
   1. Process sequence of N-MOSFET in Metal Gate
   2. From inverter to memory cell
   3. SRAM in NMOS Metal Gate
   4. The threshold voltage of the MOSFET
      1. Parasitic FET
      2. Enhancement/Depletion Transistor
      3. N-MOS Logic by E/D Transitors
      4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
   1. Metal Gate -> Si Gate
   2. Channel-Stop & LOCOS Technology
      1. Example: Process flow of E/D SiGate LOCOS Inverter
      2. LOCOS Variation
      3. Shallow Trench Isolation
   3. Lightly doped drain
   4. SALICIDE
   5. Self Aligned Contacts (SAC)
   6. Resist trimming
4. Transition to CMOS Technology
   1. MOS Transistor Types
   2. CMOS Inverter
      1. Consideration NMOS E/D Inverter
      2. Comparison CMOS Inverter
   3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
   1. Scaling
      1. Challenges
      2. Material Equivalent Scaling
      3. Further Concepts

SC-Basics

Lect

1. Introduction

2. Silicon as S
2.1 The Silicon C
2.2 Crystal Defec
2.3 Conductivity
2.4 Si as the mo
2.4.1. Fabrication o
2.4.2. Si Wafer Fab

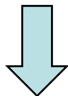
3. The Oxidati
3.1. Growth mode
3.2. Dependency
3.3. Oxidation tec
3.4. Stress and O

4. Lithography
4.1. Process sequ
4.1.1. Negative Res
4.1.2. Positive Resi
4.2. Multi-Layer R
4.3. Image Rever
4.4. Pattern Enha

5. Doping
5.1 Diffusion
5.1.1. ...from an infi
5.1.2. ...from a finite
5.1.3. Two step Diff
5.1.4. Further Effec
5.1.5. Practical Rea
5.2 Implantation
5.2.1. Projected Ra
5.2.2. Implantation
5.2.3. Channeling
5.2.4. Further Effec
5.2.5. Healing and
5.2.6. Implantation

Continue

"SCT_SS20_03.02" 21:13



http://www.computerhistory.org/siliconengine/timeline/

DRAM

DRAM Dynamic Random Access Memory

1T1C

Gate Array

Bit line

BL

BL

P1 or Poly 1

Poly Si

ROX

ROX

SiO_2

gate

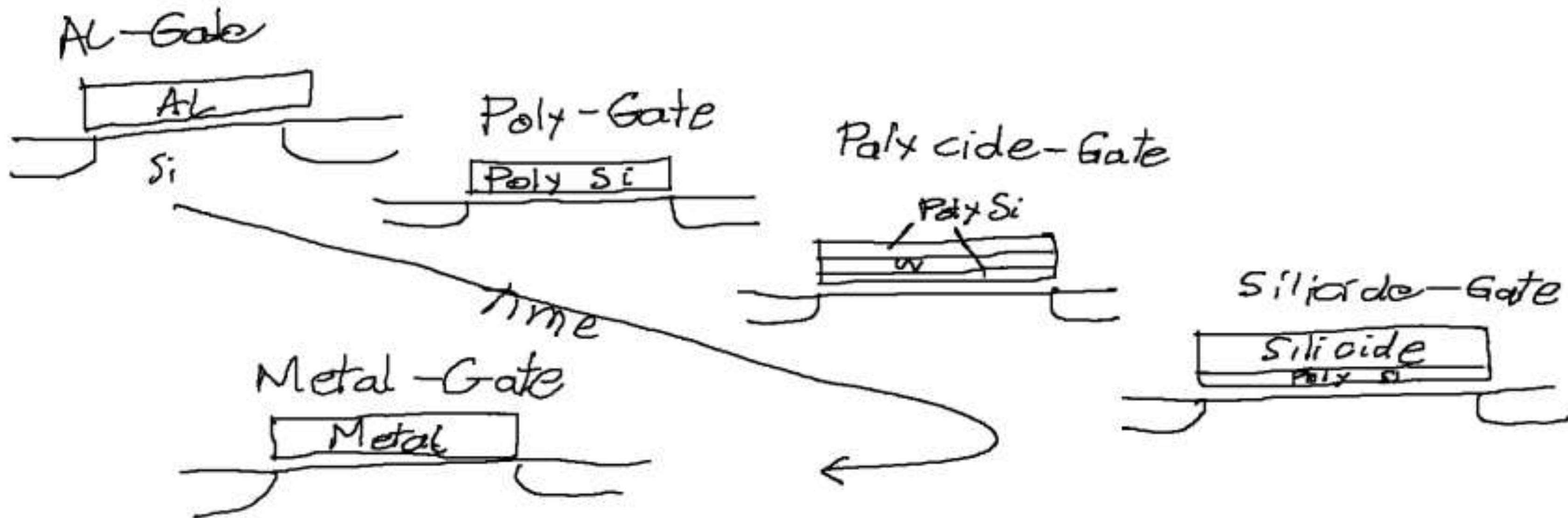
WL Silicon word line

Continue

"SCT_SS20_03.03" 10:50

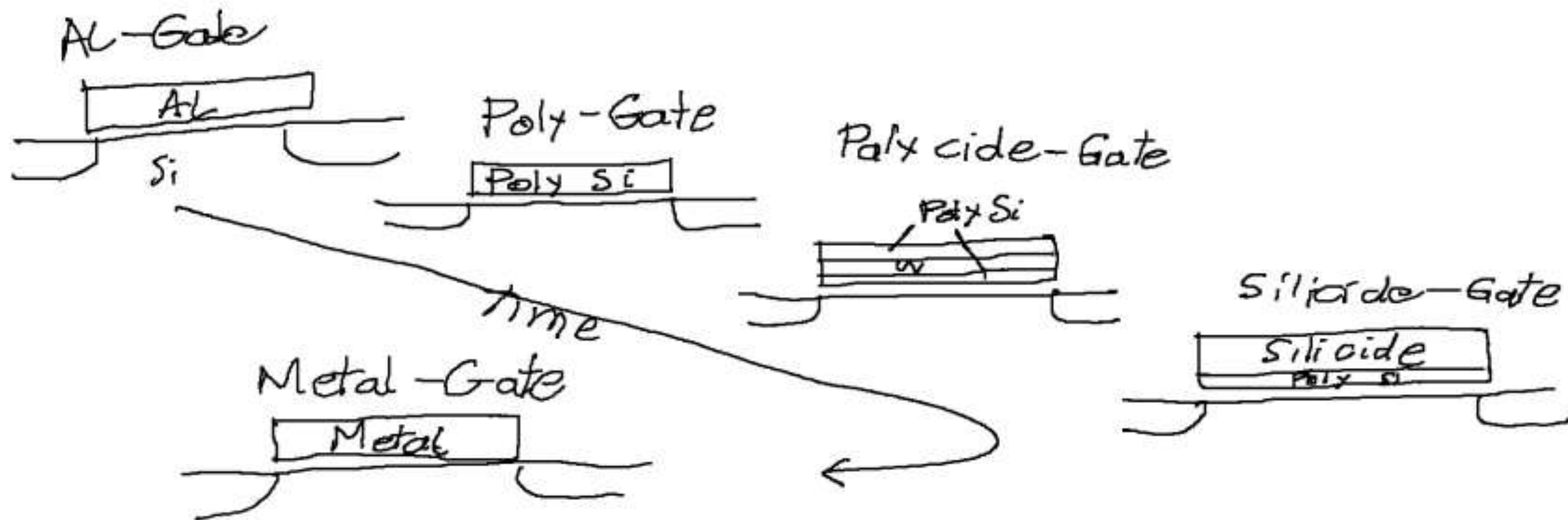
 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!

Gate materials



TECHNISCHE UNIVERSITÄT DRESDEN

Gate materials



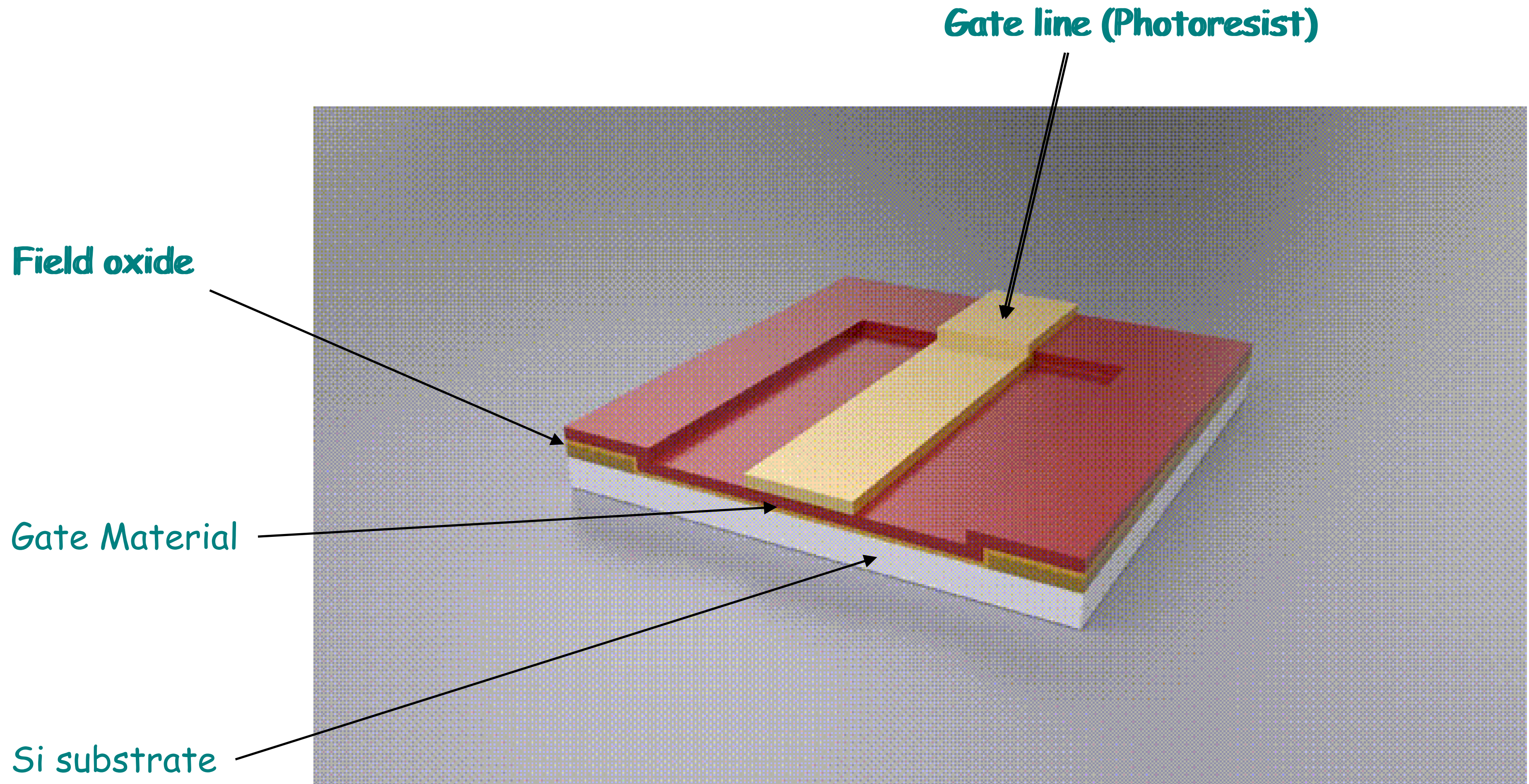
Continue

"SCT_SS20_03.04" 27:44

 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!

TECHNISCHE UNIVERSITÄT DRESDEN

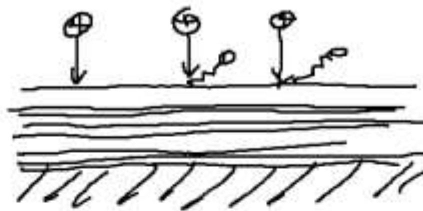
Gate RIE (idealized!)



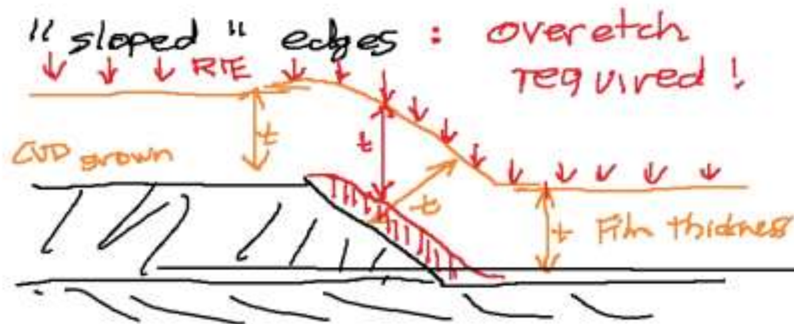
Taken from: https://www.youtube.com/watch?app=desktop&v=bor0qLifjz4
8:23 – 8:57

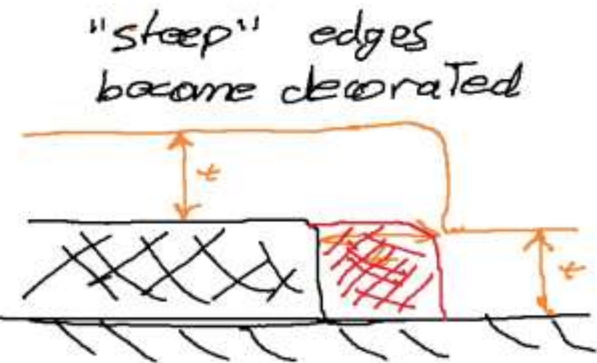
RIE on corrugated substrates

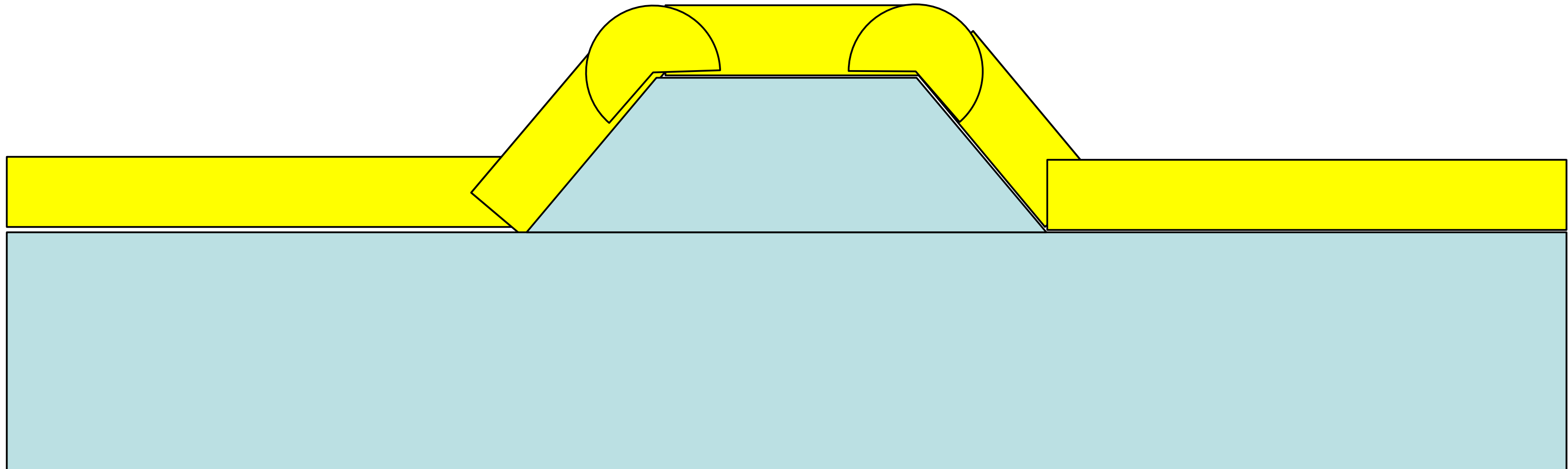
Anisotropic Etching (RIE) on corrugated surfaces



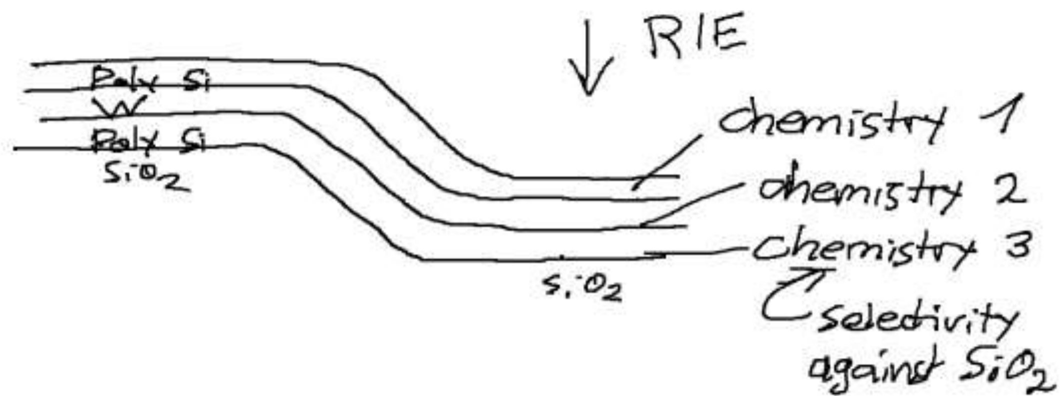
plane substrate
no problem





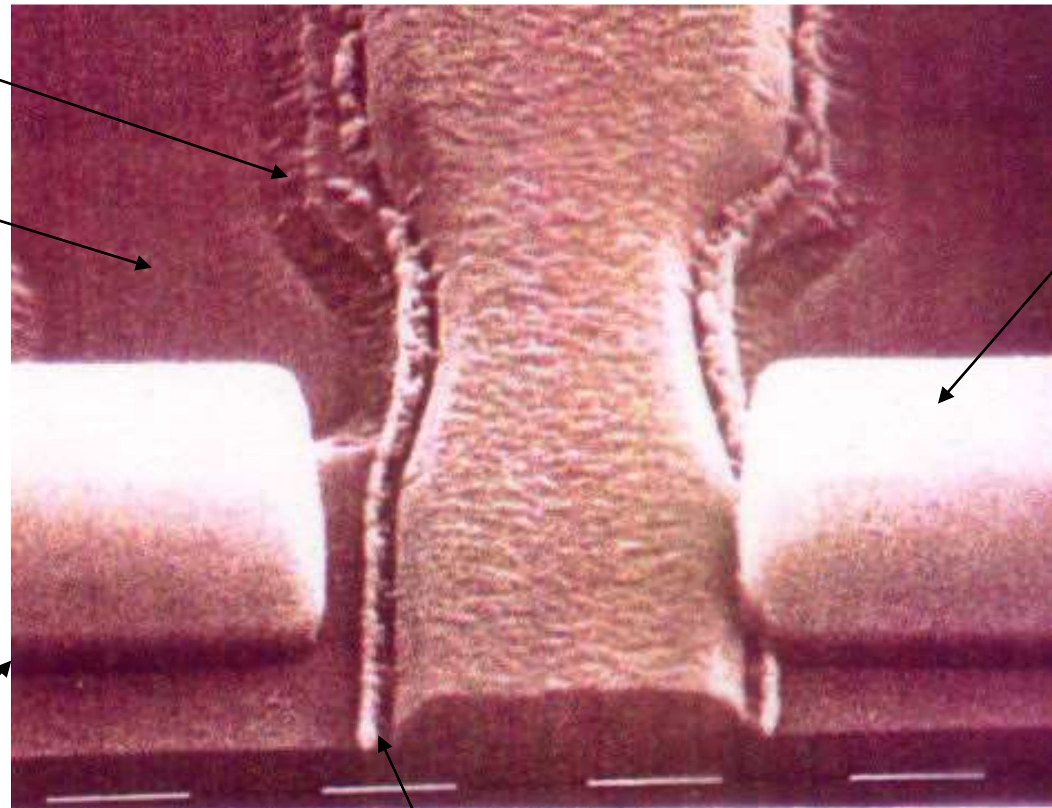


RIE of polycide



0. Process Integration:
Example: Stringer Problem

Undesired residuals after gate RIE



 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!

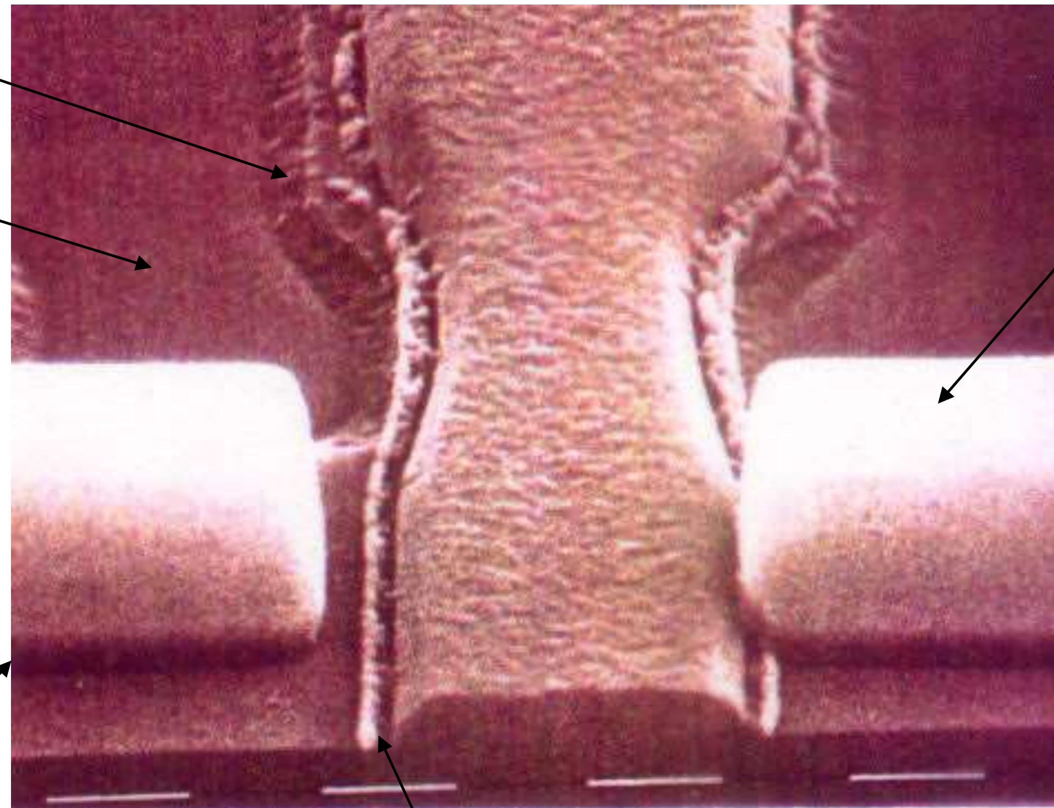
0. Process Integration:
Example: Stringer Problem

Undesired residuals after gate RIE

Field oxide

Si substrate

Gate line (Photoresist)



Gate Material

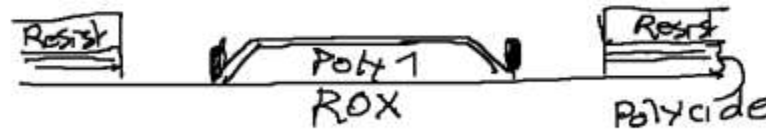
Stringer or filaments

Continue

"SCT_SS21_03.05" 22:28

Finding the origin of the problem

Observation

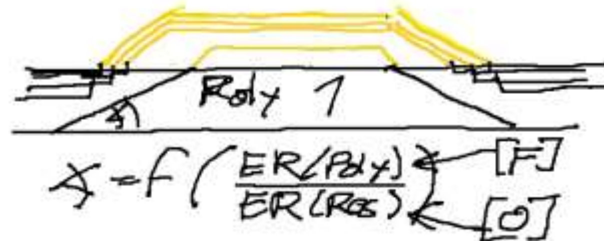


Search for origin:

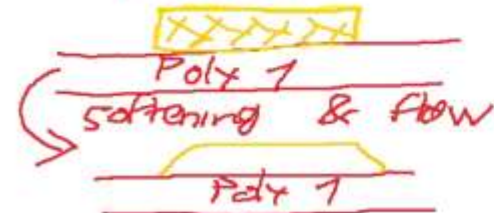
Assumption 1 RIE
Chemistry, Endpoints
Tool parameters

Assumption 2
Polycide CVD
Poly oxidation
Passivation ?

Assumption 3
Poly 1 RIE



Assumption 4 and final origin
Poly 1 Resist
Reflow



 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!

P1 resist reflow:

Vor RIE

Resist nach Reflow

P1 layer

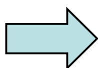
fig 10

Nach RIE

Resist

P1 Layer

fig 11

Continue 

"SCT_SS20_03.06" 04:40

Dresden Microelectronics Academy

A Production Organization
Typical Departments

P R O D U C T I O N

FrontEnd Process Depts. Technology & Production	BackEnd Process Depts. Technology & Production	Support Departments	Process Technology & Integration
⊙ Furnace / RTP	⊙ Assembly	⊙ IT / C I M	⊙ Process Integration Logic
⊙ WET-Processing	⊙ Final Test	⊙ Transport System	⊙ Process Integration Memory
⊙ Lithography	⊙ Burn-In	⊙ Production Control	⊙ Product Engineering
⊙ Etch	⊙ BE-Technology	⊙ Production Coordination	⊙ Defect Density Engineering
⊙ CMP	⊙ ...	⊙ Facilities	⊙ Electrical Para. Engineering
⊙ Ion-Implantation		⊙ HR Human Resources	⊙ Yield Enhancement Eng.
⊙ PVD / Sputter		⊙ ...	⊙ Physical Failure Analysis
⊙ CVD			⊙ ...
⊙ Metrology			
⊙ Wafer Test			

Now focus on Sub-Organization
of a single
FrontEnd Production Department!

© 1999 - 2010 Infineon Technologies AG
Speaker: F. Heinlein
Date: August 16, 2010
Page: 27

TECHNISCHE UNIVERSITÄT DRESDEN   GLOBALFOUNDRIES   infineon

Outline

SC-Basics

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
   1. MOS Structure, MOS Capacitor
   2. Structure of a MOSFET
   3. I/V behaviour
2. Circuits in Metal-Gate FET Technology
   1. Process sequence of N-MOSFET in Metal Gate
   2. From inverter to memory cell
   3. SRAM in NMOS Metal Gate
   4. The threshold voltage of the MOSFET
      1. Parasitic FET
      2. Enhancement/Depletion Transistor
      3. N-MOS Logic by E/D Transitors
      4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
   1. Metal Gate -> Si Gate
   2. Channel-Stop & LOCOS Technology
      1. Example: Process flow of E/D SiGate LOCOS Inverter
      2. LOCOS Variation
      3. Shallow Trench Isolation
   3. Lightly doped drain
   4. SALICIDE
   5. Self Aligned Contacts (SAC)
   6. Resist trimming
4. Transition to CMOS Technology
   1. MOS Transistor Types
   2. CMOS Inverter
      1. Consideration NMOS E/D Inverter
      2. Comparison CMOS Inverter
   3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
   1. Scaling
      1. Challenges
      2. Material Equivalent Scaling
      3. Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

 © J. W. Bartha 2021 TUD INTERNAL USE ONLY!

»Wissen schafft Brücken.«