TECHNISCHE UNIVERSITÄT DRESDEN

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select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 – Process Integration

4. Web-based virtual Lecture: May 06 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here 

"SCT_SS21_04.1" 14:20

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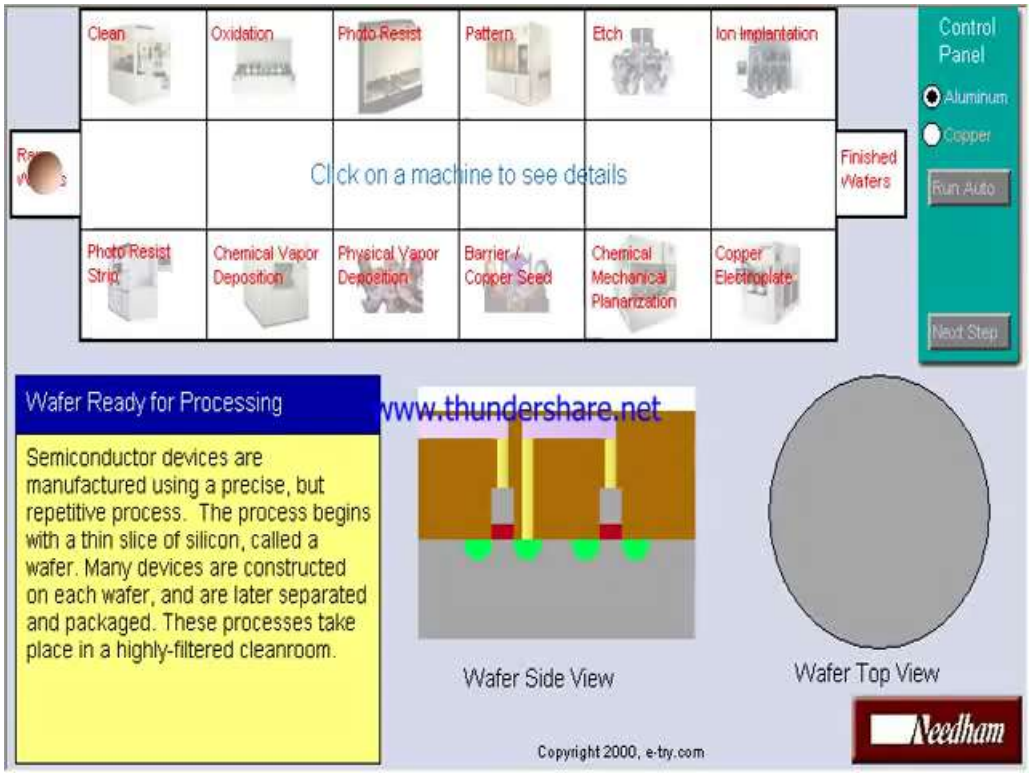
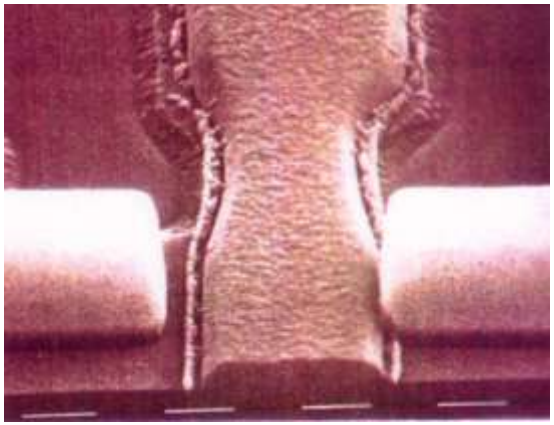
Generic simulation of a MOS FET process flow

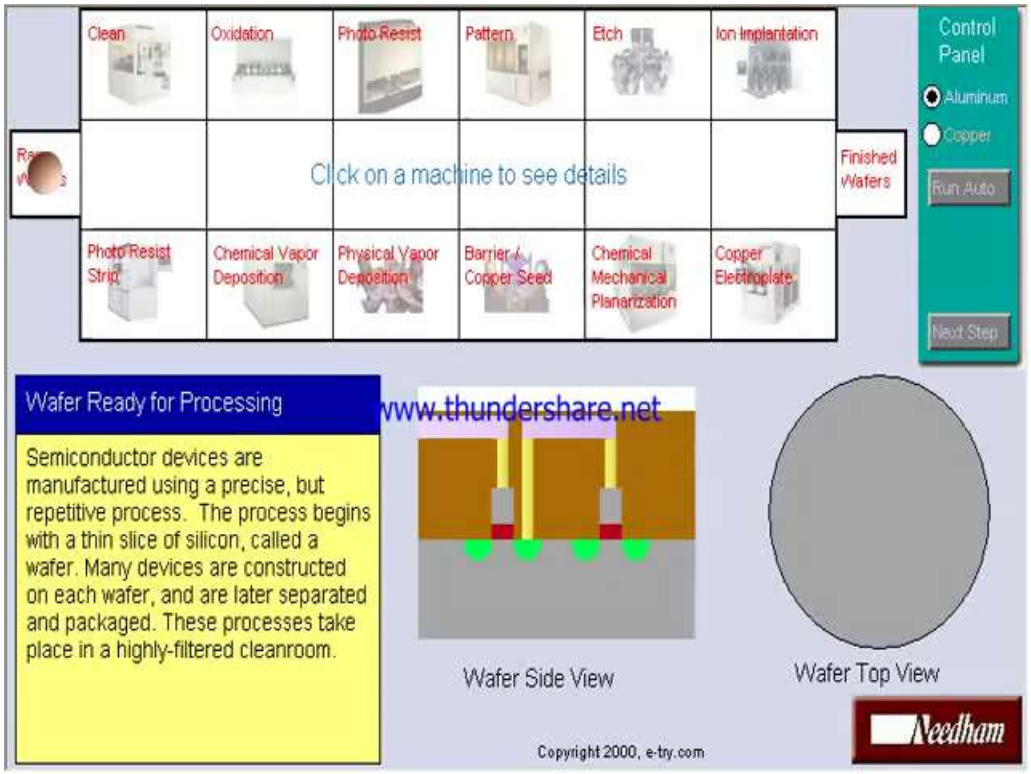


http://www.e-try.com/

Generic simulation of a MOS FET process flow

DRAM
Polycide
RIE





http://www.e-try.com/

A Production Organization Typical Departments

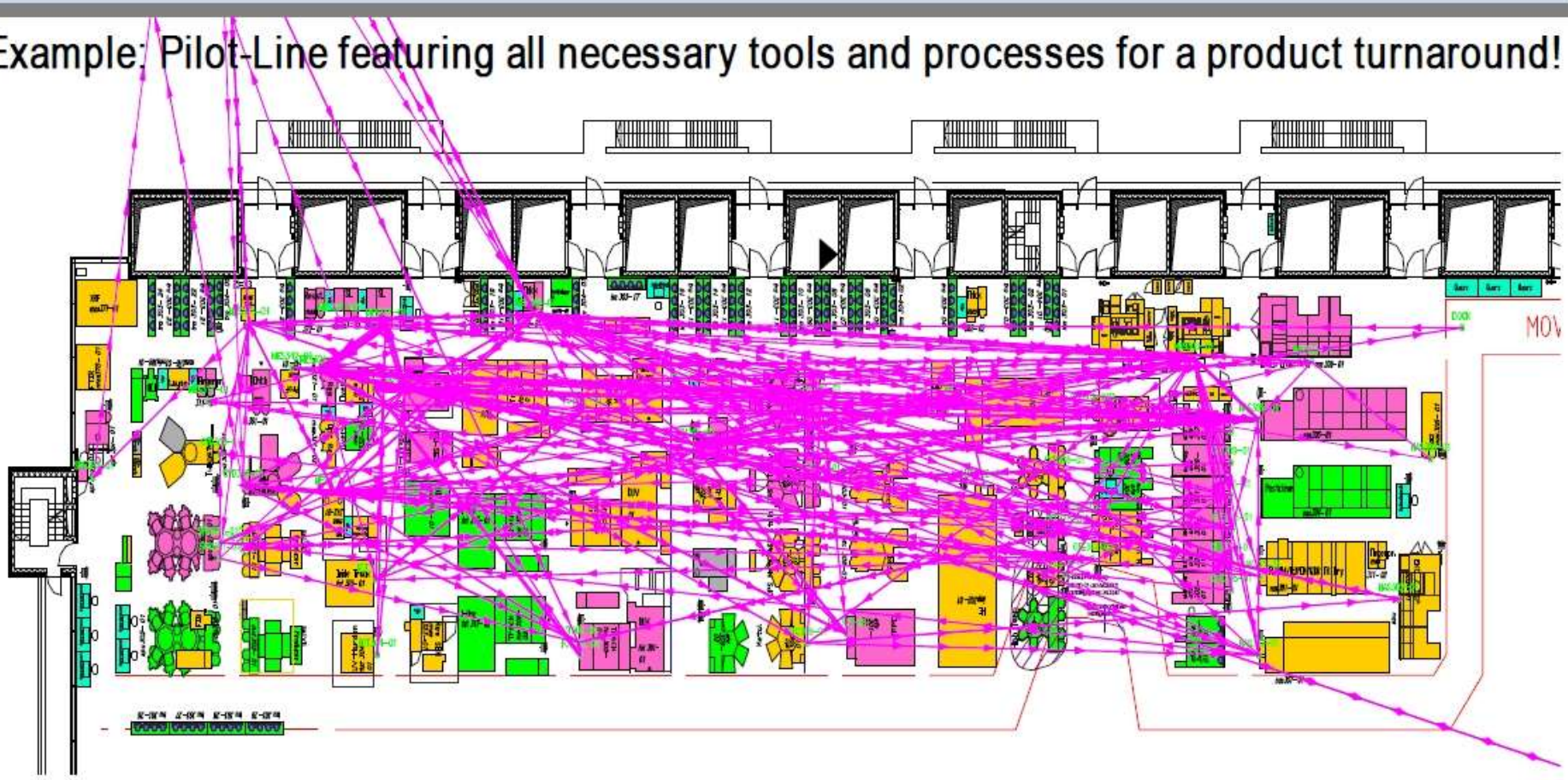
P R O D U C T I O N

FrontEnd Process Depts. Technology & Production	BackEnd Process Depts. Technology & Production	Support Departments	Process Technology & Integration
⊙ Furnace / RTP	⊙ Assembly	⊙ IT / C I M	⊙ Process Integration Logic
⊙ WET-Processing	⊙ Final Test	⊙ Transport System	⊙ Process Integration Memory
⊙ Lithography	⊙ Burn-In	⊙ Production Control	⊙ Product Engineering
⊙ Etch	⊙ BE-Technology	⊙ Production Coordination	⊙ Defect Density Engineering
⊙ CMP	⊙ ...	⊙ Facilities	⊙ Electrical Para. Engineering
⊙ Ion-Implantation		⊙ HR Human Resources	⊙ Yield Enhancement Eng.
⊙ PVD / Sputter		⊙ ...	⊙ Physical Failure Analysis
⊙ CVD			⊙ ...
⊙ Metrology			
⊙ Wafer Test			

Now focus on Sub-Organization
of a single
FrontEnd Production Department!

Illustration of Production Complexity

Example: Pilot-Line featuring all necessary tools and processes for a product turnaround!



Outline

SC-Basics

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

Outline

SC-Basics

Continue

"SCT_SS20_04.2" 52:50

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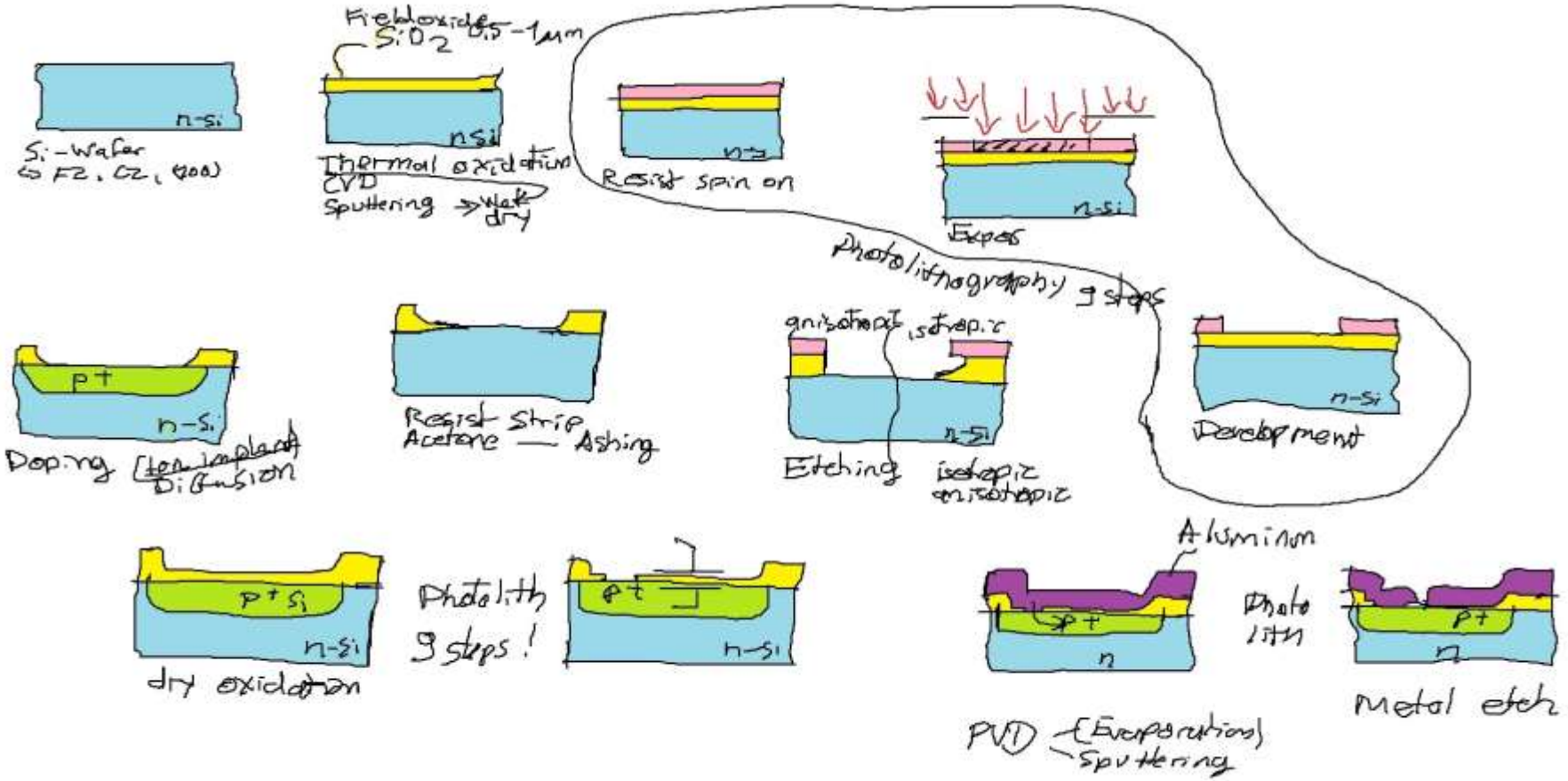
http://www.computerhistory.org/siliconengine/timeline/

1.1 MOS Structure – MOS Capacitor



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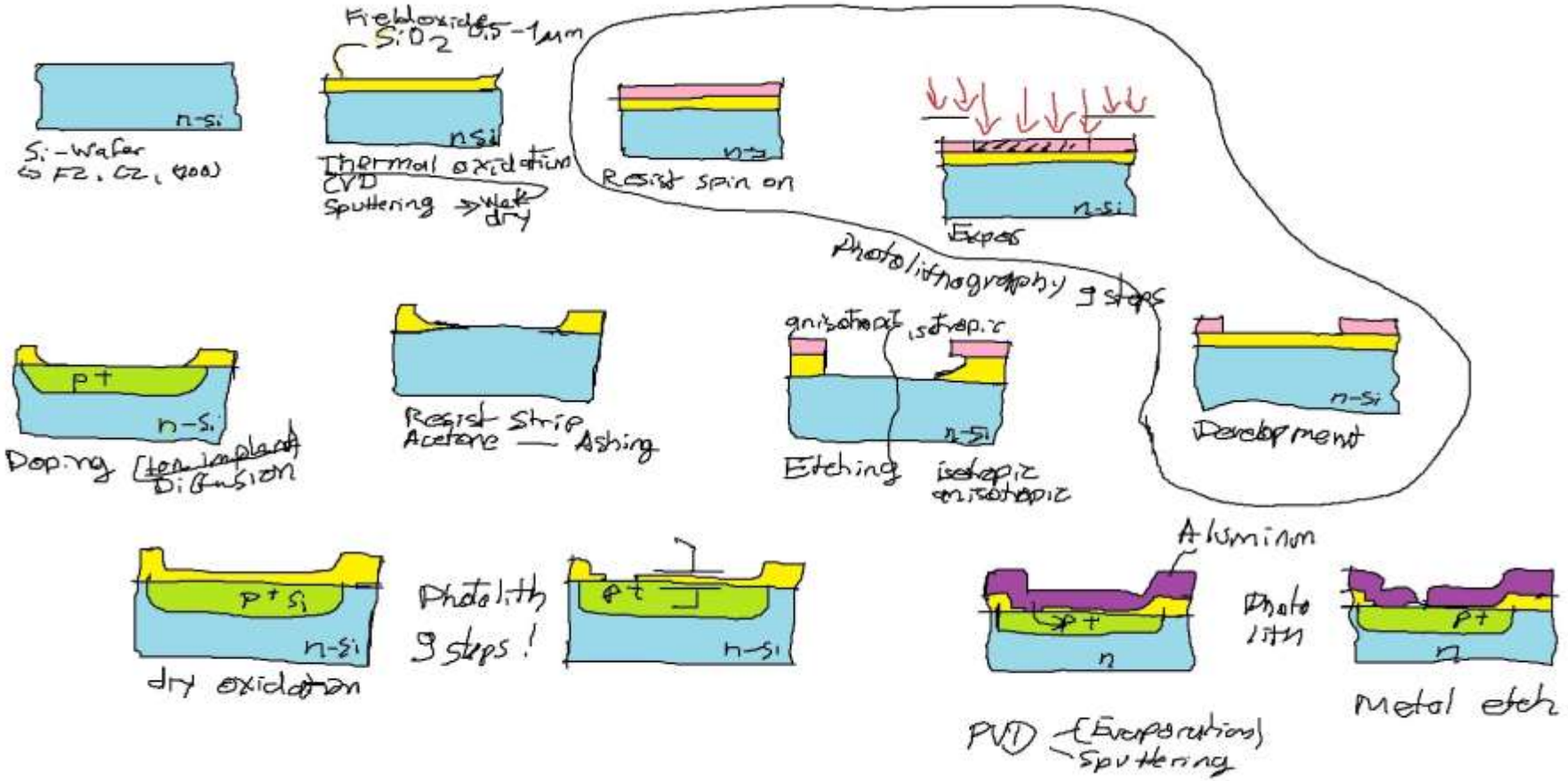

Continue

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Aspects of process integration

Process Integration means:
Compilation of process steps to generate a Chip

Aspects of process integration

Process Integration means:
Compilation of process steps to generate a Chip

and is related to: Electrical performance
Dimensions
Materials
Design

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Example: Capacitor

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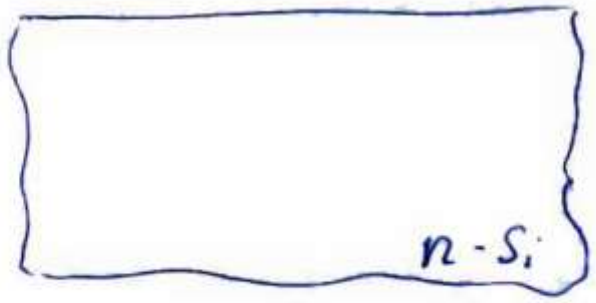

Si Substrat

Aspects of process integration

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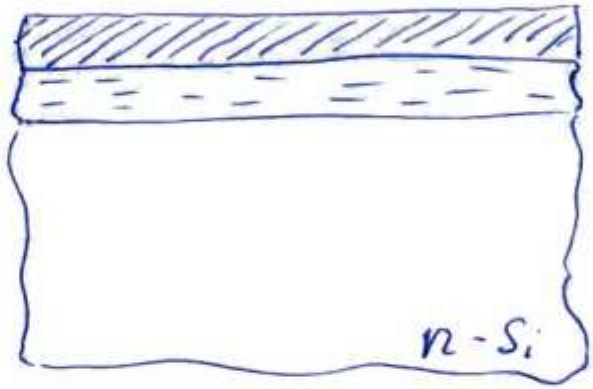
Example: Capacitor



Resist Apply

Aspects of process integration

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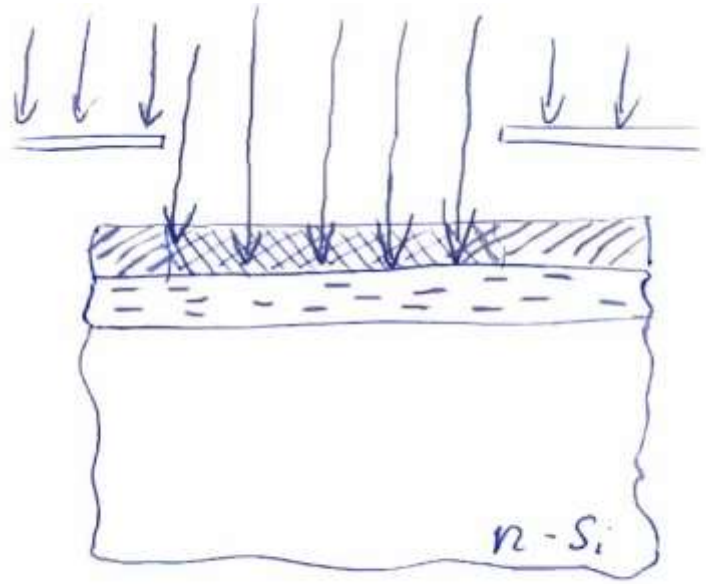
Design



Expose

Example: Capacitor

Aspects of process integration

Process Integration means:
Compilation of process steps to generate a Chip

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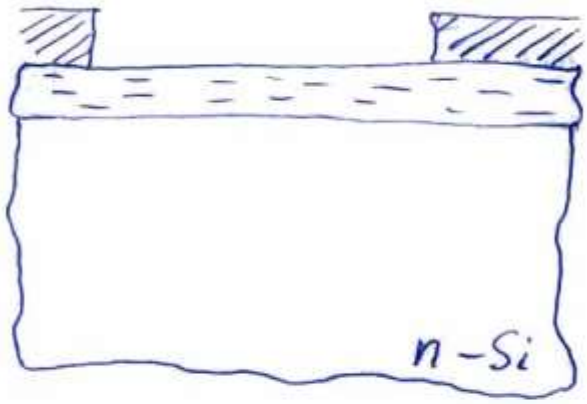
Example: Capacitor



Develop

Aspects of process integration

Process Integration means:
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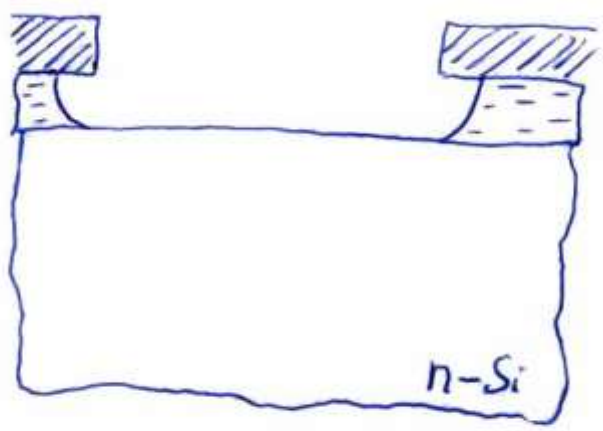
Dimensions
Materials
Design

Example: Capacitor



Oxide Etch

Aspects of process integration

Process Integration means:
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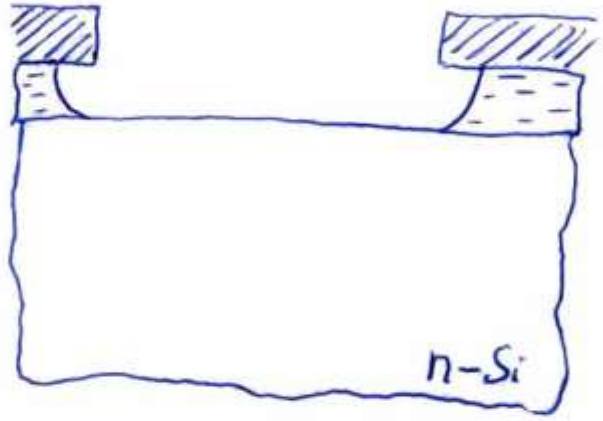
Dimensions
Materials
Design

Example: Capacitor

Oxide Etch



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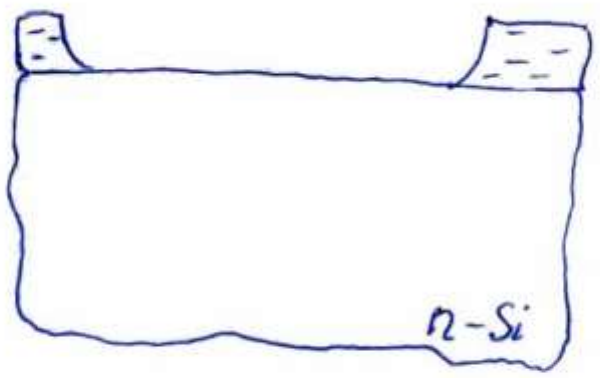

Resist Strip

Aspects of process integration

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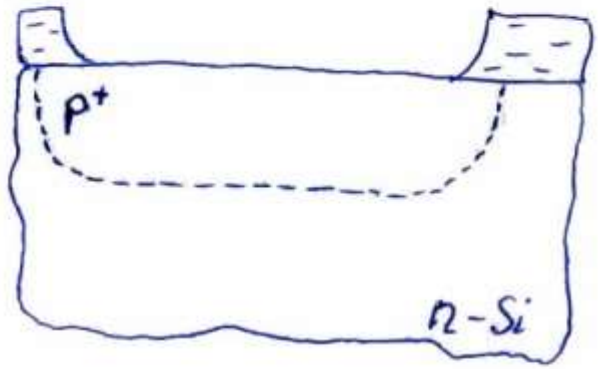
Dimensions
Materials
Design

Example: Capacitor



Diffusion or Implant

Aspects of process integration

Process Integration means:
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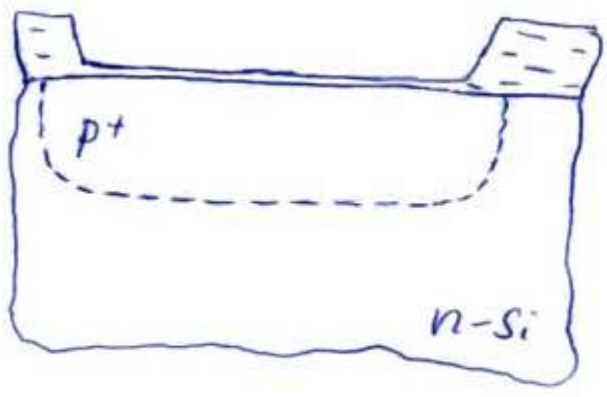
Dimensions
Materials
Design

Example: Capacitor



Dry Oxidation

Aspects of process integration

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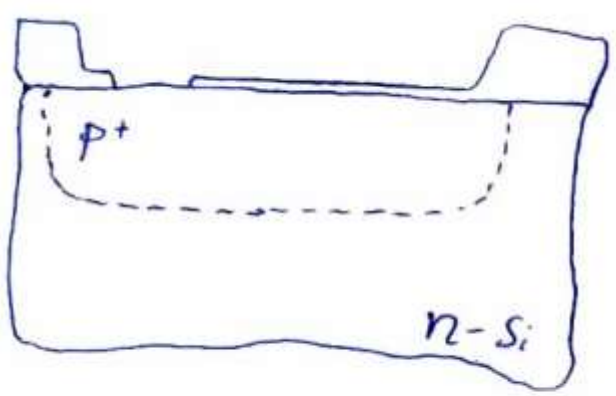
Dimensions
Materials
Design

Example: Capacitor



Litho and Etch Oxide

Aspects of process integration

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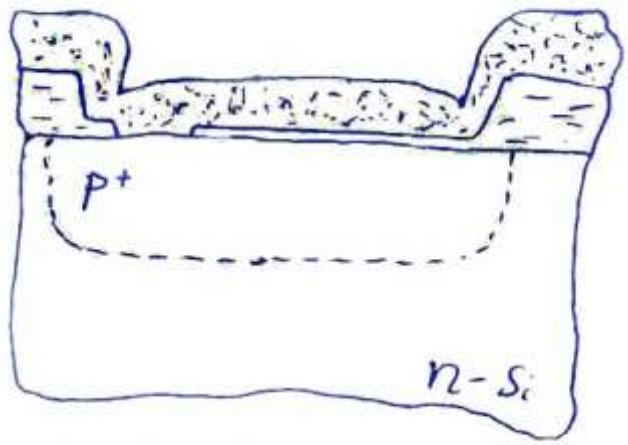
Dimensions
Materials
Design

Example: Capacitor



Sputter Deposition

Aspects of process integration

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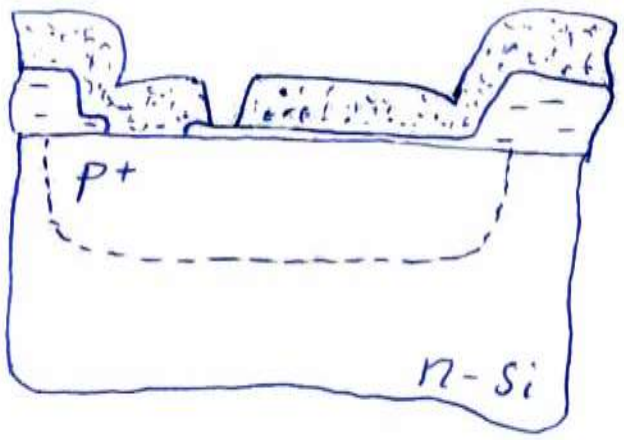
Dimensions
Materials
Design

Example: Capacitor



Litho and Etch Metal

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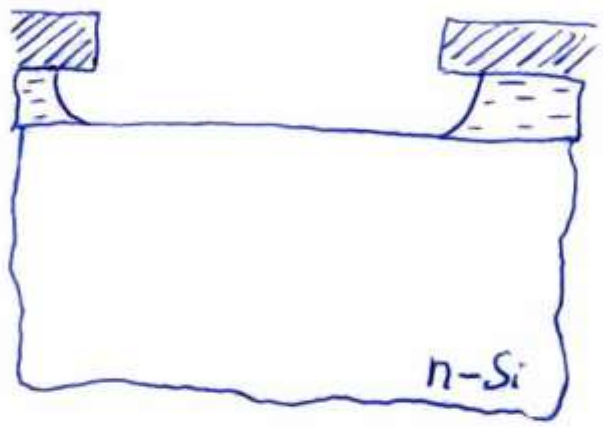
Example: Capacitor



Oxide Etch

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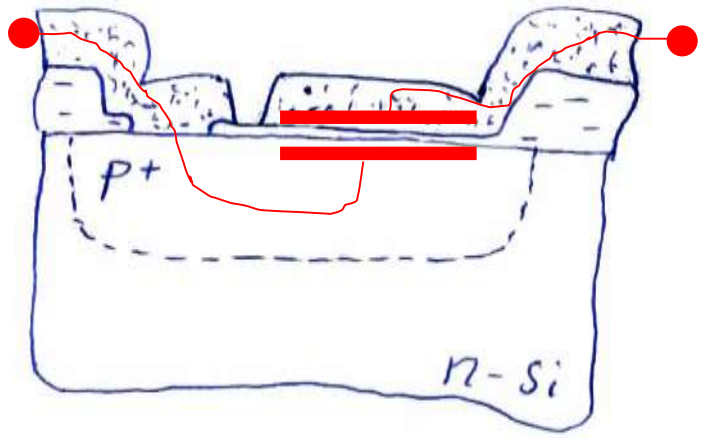
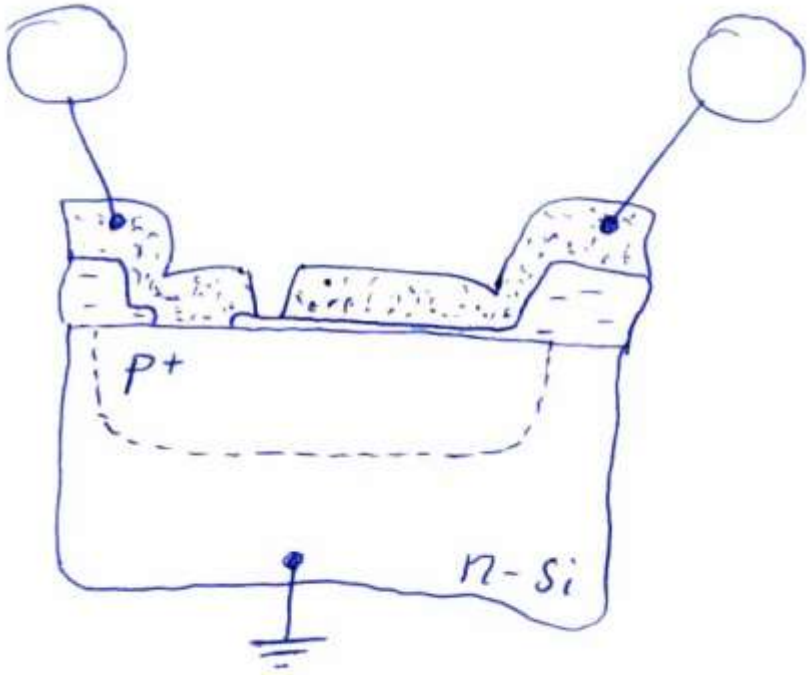


Litho and Etch Metal

Process - integration

MOS Capacitor

Question: If the substrate is grounded, is there a certain polarity required?



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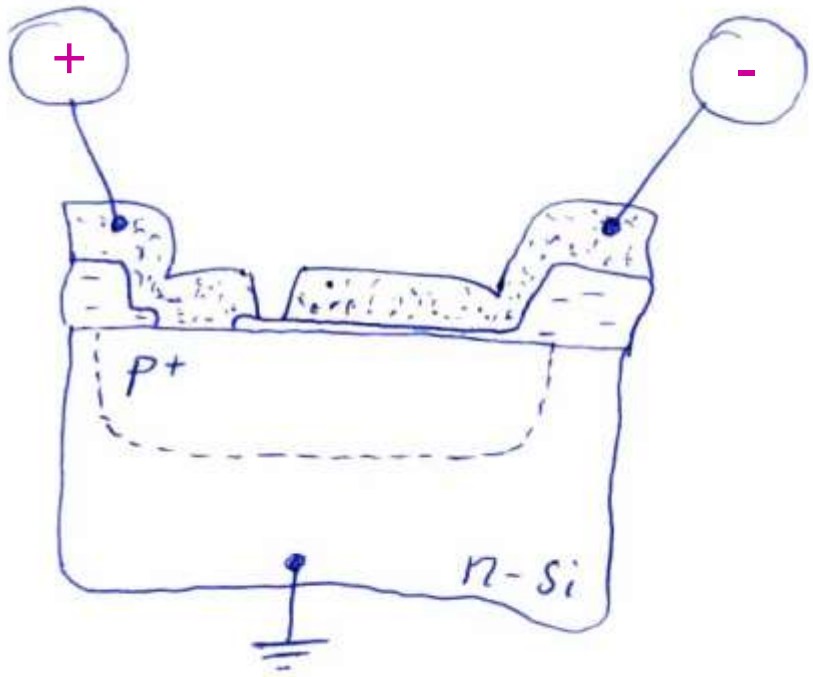

Process - integration

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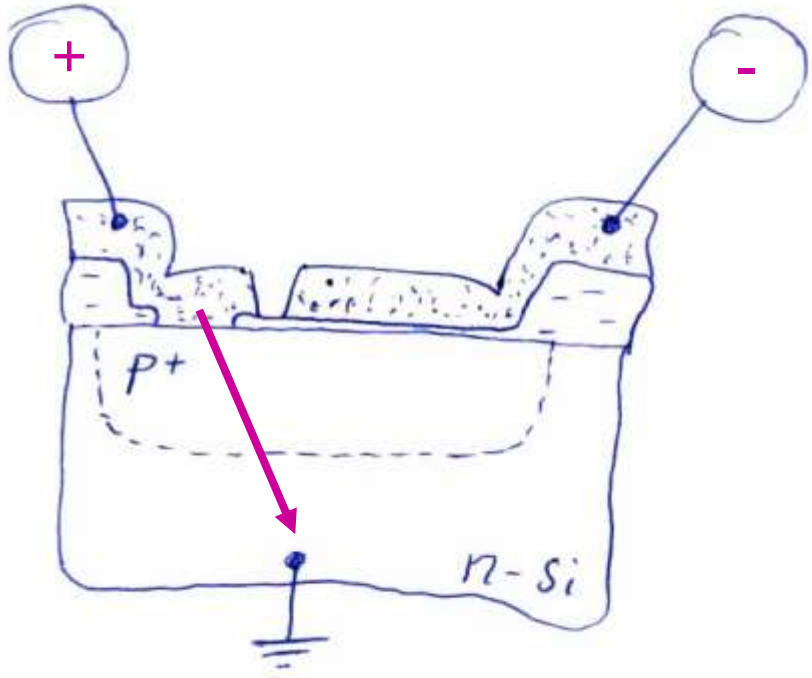


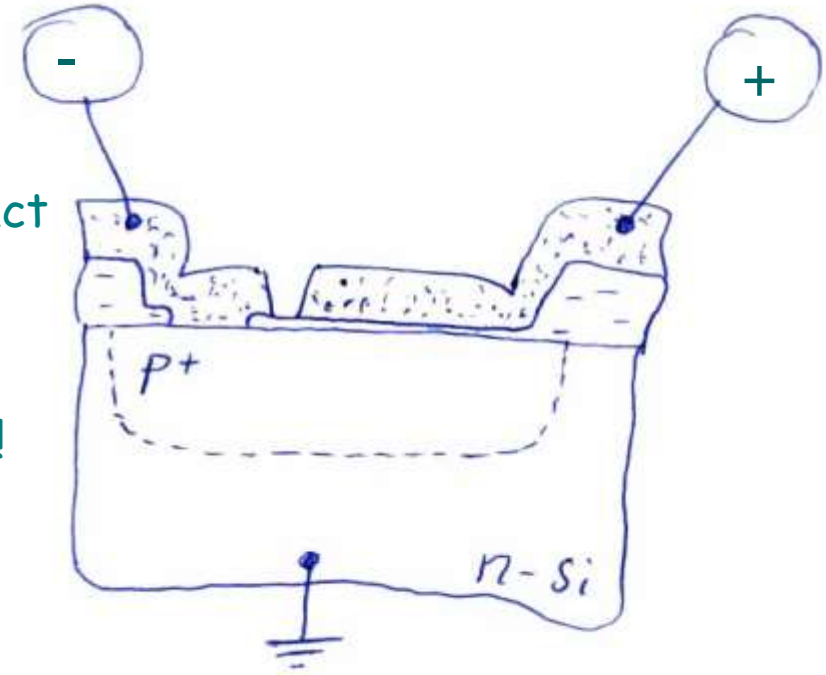
If the p+ terminal is connected to + we have a short to ground through the p^+/n substrate diode

Process - integration

MOS Capacitor

Question: If the substrate is grounded, is there a certain polarity required?

The substrate contact has to be minus otherwise the p^+/n junction is in forward direction!



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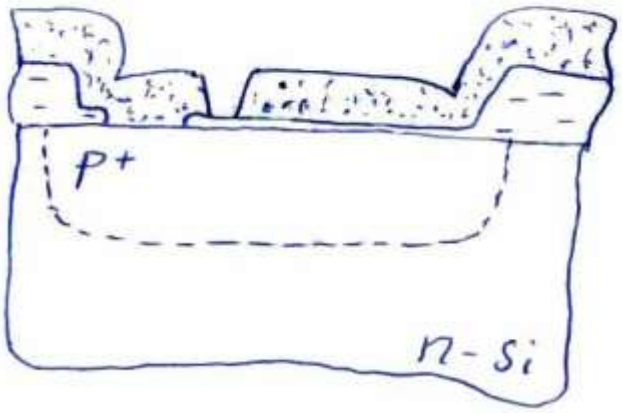


Impact of material and layout:

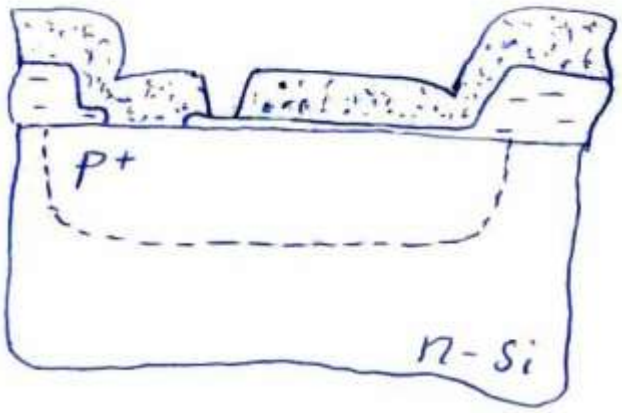
Typical DRAM capacitor C = 30 fF

$C = Q/U$; $C = \varepsilon_0 \varepsilon_r A/d$; $\varepsilon_0 = 8.85\ 10^{-12}$ F/m

$\varepsilon_r(SiO_2) = 3.9$

Process - integration

MOS Capacitor



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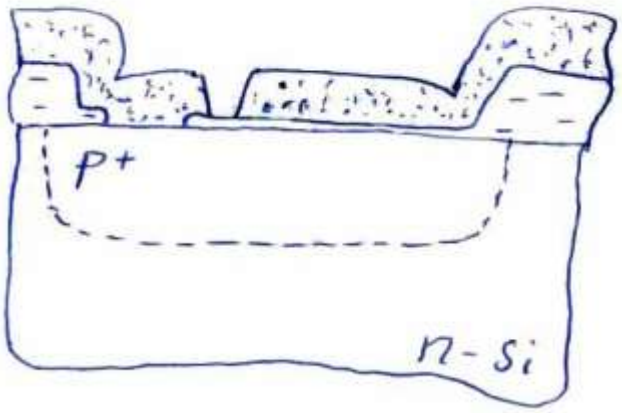
charges at U = 2.5 V: $Q = C \cdot U = 30 \cdot 10^{-15}$ F $\cdot$ 2.5 V = $75 \cdot 10^{-15}$ As

($e = 1.6 \cdot 10^{-19}$ C) or 469000 Electrons (↳ Noise)

Process - integration

MOS Capacitor



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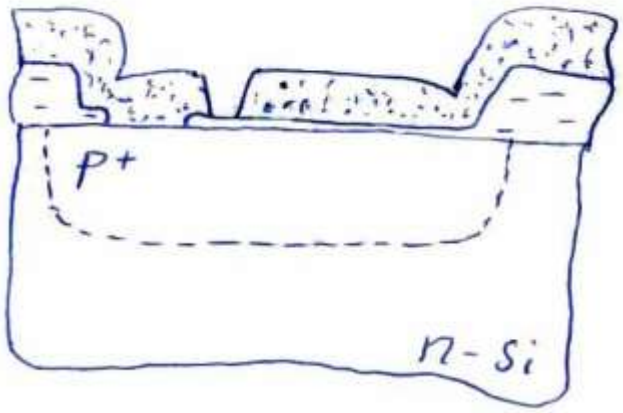
Can this be realized with a cell size of $1\mu m^2$?

Process - integration

MOS Capacitor



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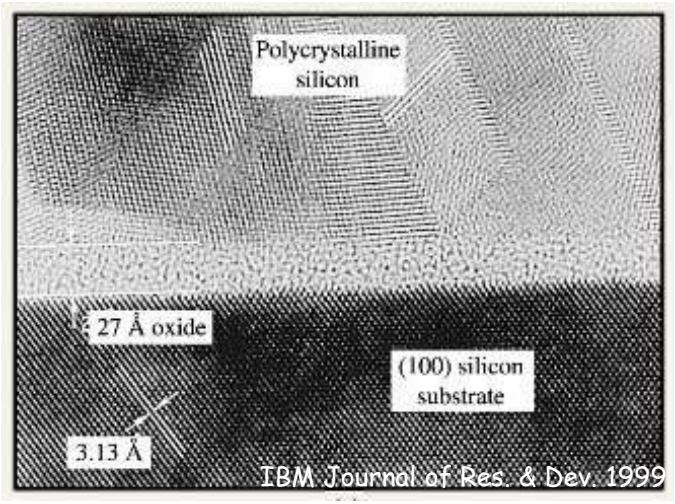
Required oxide thickness: $d = \varepsilon_0\varepsilon_r A/C$ = 1.1 nm

Process - integration

MOS Capacitor



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Can this be realized with a cell size of $1\mu m^2$?

Required oxide thickness: $d = \varepsilon_0\varepsilon_r A/C = 1.1$ nm

(Break Down Voltage of SiO_2 is 7 MV/cm, Further problem – tunnel current!)

U/d = 2.5V/1.1 nm = 22 MV/cm !! Therefore minimum oxide thickness d = 3.3 nm

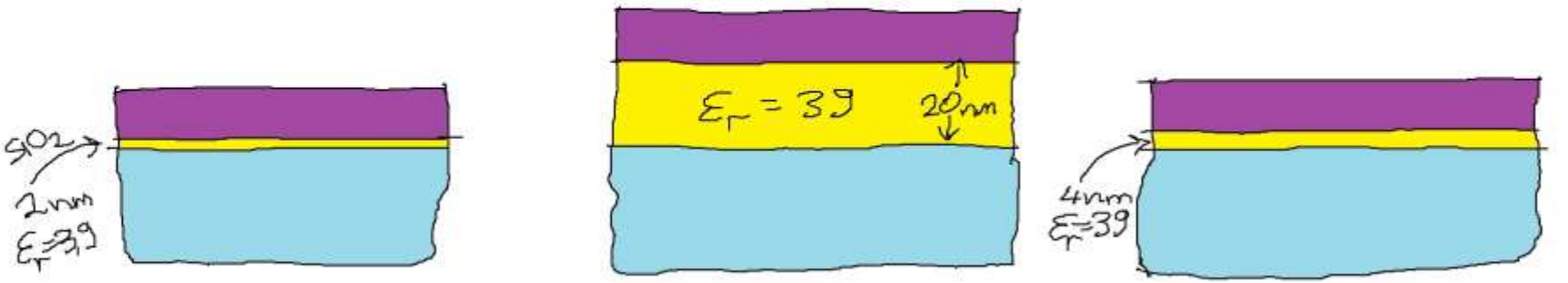
This requires $A = 3\ \mu m^2$ or a different dielectric material (for example high k)!

High K - EOT

$C = \varepsilon_0 \varepsilon_r \frac{A}{t}$

Equivalent Oxide Thickness

$EOT = t_{high\,k} \frac{\varepsilon_r(SiO_2)}{\varepsilon_r(high\,K)}$



$C_0 = C_1$

$C_2 = 5 \cdot C_1 = 5 C_0$

$C_2 \triangleq$ Oxide 0,4nm

Equivalent oxide thickness

From Wikipedia, the free encyclopedia

An **Equivalent oxide thickness** is a distance, usually given in nanometers (nm), which indicates how thick a silicon oxide film would need to be to produce the same effect as the high-κ material being used.

The term is often used when describing field effect transistors which rely on an electrically insulating pad of material between a gate and a doped semiconducting region. Device performance has typically been improved by reducing the thickness of a silicon oxide insulating pad. As the thickness approached 5–10 nm, leakage became a problem and alternate materials were necessary to increase the thickness while retaining the switching speed. Materials having larger dielectric constants enable thicker films to be used for this purpose while retaining fast reaction of the transistor. For example, a high-κ material with dielectric constant of 39 (compared to 3.9 for silicon oxide) can be made ten times thicker than silicon oxide which helps to reduce the leakage of electrons across the dielectric pad, while achieving the same capacitance. Commonly used high-κ gate dielectrics include hafnium oxide and more recently aluminum oxide for gate-all-around devices.

$$\mathrm{EOT} = t_{\text{high-}\kappa}\left(\frac{k_{\mathrm{SiO_2}}}{k_{\text{high-}\kappa}}\right)$$

The EOT definition is useful to quickly compare different dielectric materials to the industry standard silicon oxide dielectric, as:

$$\epsilon_0\,\epsilon_{\mathrm{SiO_2}}\frac{A}{\mathrm{EOT}} = \epsilon_0\,\epsilon_{\text{high-}\kappa}\frac{A}{t_{\text{high-}\kappa}} = C$$

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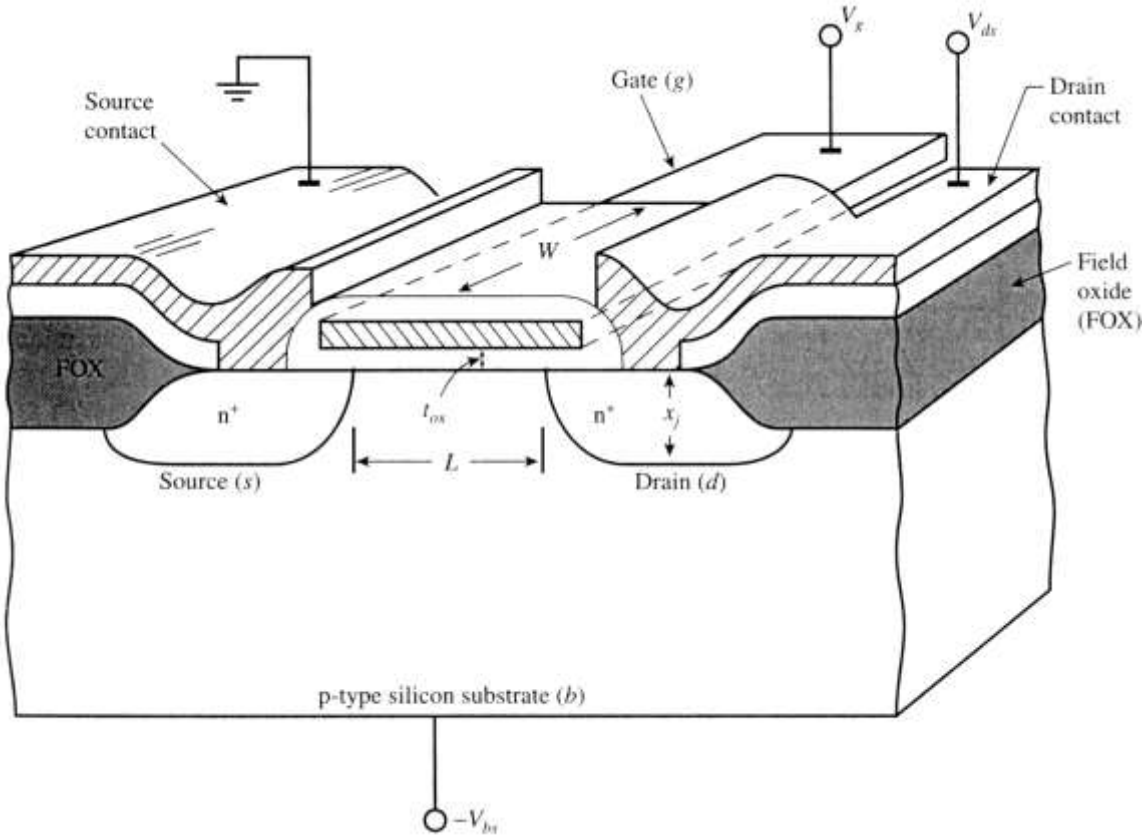
Continue

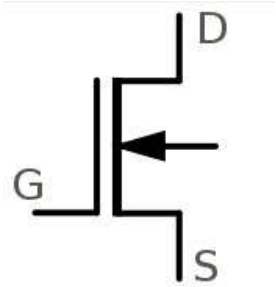
"SCT_SS20_04.4" 02:02

VIDEO CAMPUS SACHSEN

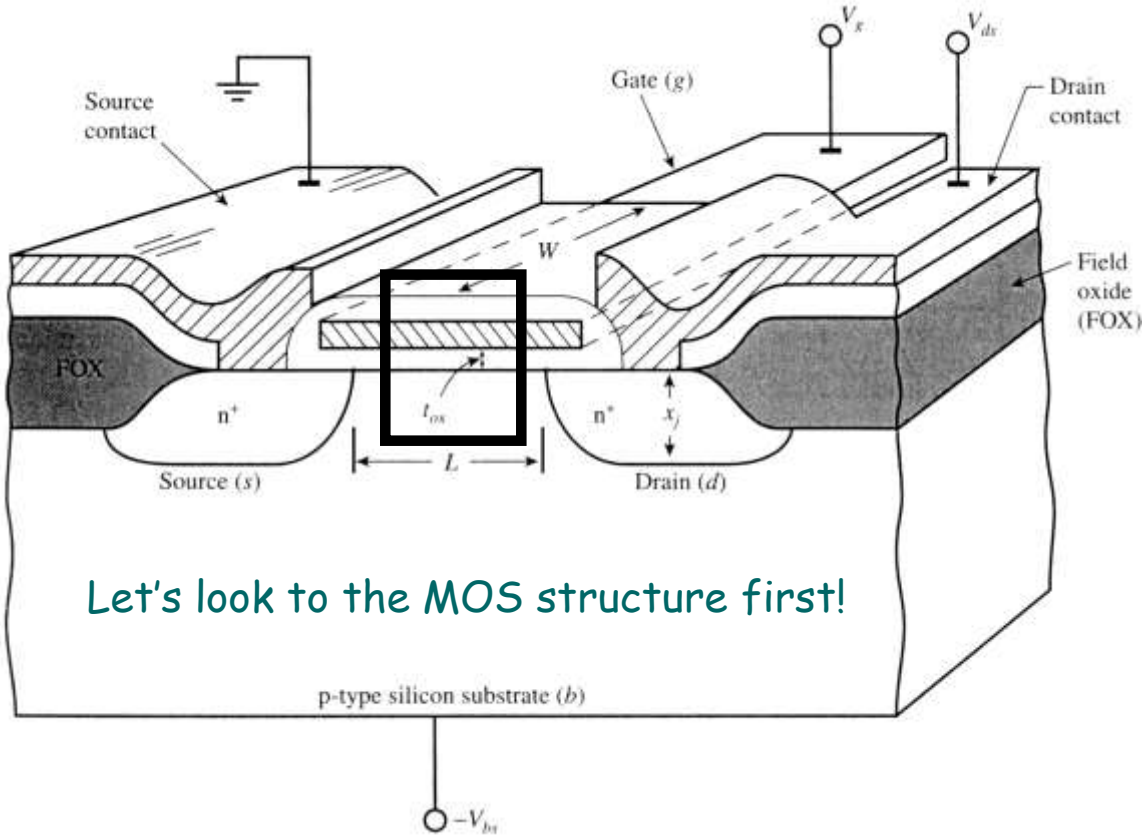
1.2 Transition to the MOSFET



MOS capacitor
CV behavior
-Accumulation
-Depletion
-Inversion

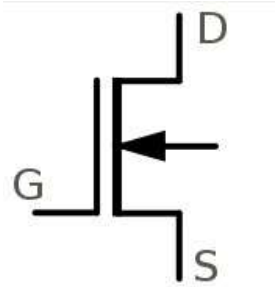


1.2 Transition to the MOSFET



Let's look to the MOS structure first!

MOS capacitor
CV behavior
-Accumulation
-Depletion
-Inversion



»Wissen schafft Brücken.«