TECHNISCHE UNIVERSITÄT DRESDEN

The hyperlinks to the video streams in this virtual lecture are marked by the Video Campus Sachsen Logo.
To watch them you need to be logged on at the host: VCS. Please click on: https://videocampus.sachsen.de/login
select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 – Process Integration

5. Web-based virtual Lecture: May 13 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here  

"SCT_SS21_05.1" 14:59

This document including the contained video streams is only available to students of the lecture „Semiconductor Technology 2" at TU-Dresden.
It must not be copied and published outside of TUD!
It is intended for
TUD internal use only!

TECHNISCHE UNIVERSITÄT DRESDEN

Outline

Review:
- SC-Basics
- DRAM Device
- POLYCIDE
- RIE
- MOS Capacitor
- Feld/Gate Oxide
- EOT

Today: MOS-CV +

SC-Basics

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

Outline

SC-Basics

0. Introduction/Lab organization/DMA/SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

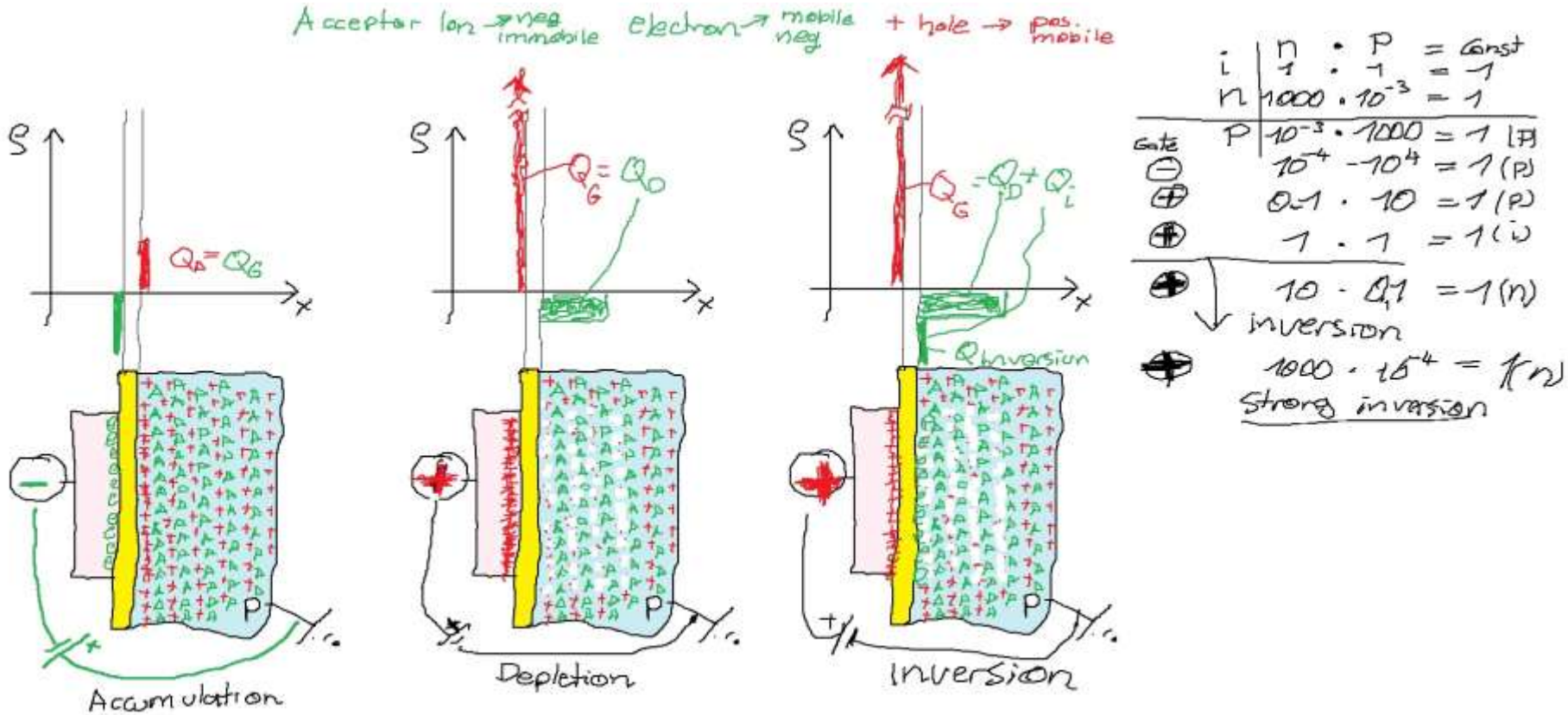
Review:
- SC-Basics
- DRAM Device
- POLYCIDE
- RIE
- MOS Capacitor
- Feld/Gate Oxide
- EOT

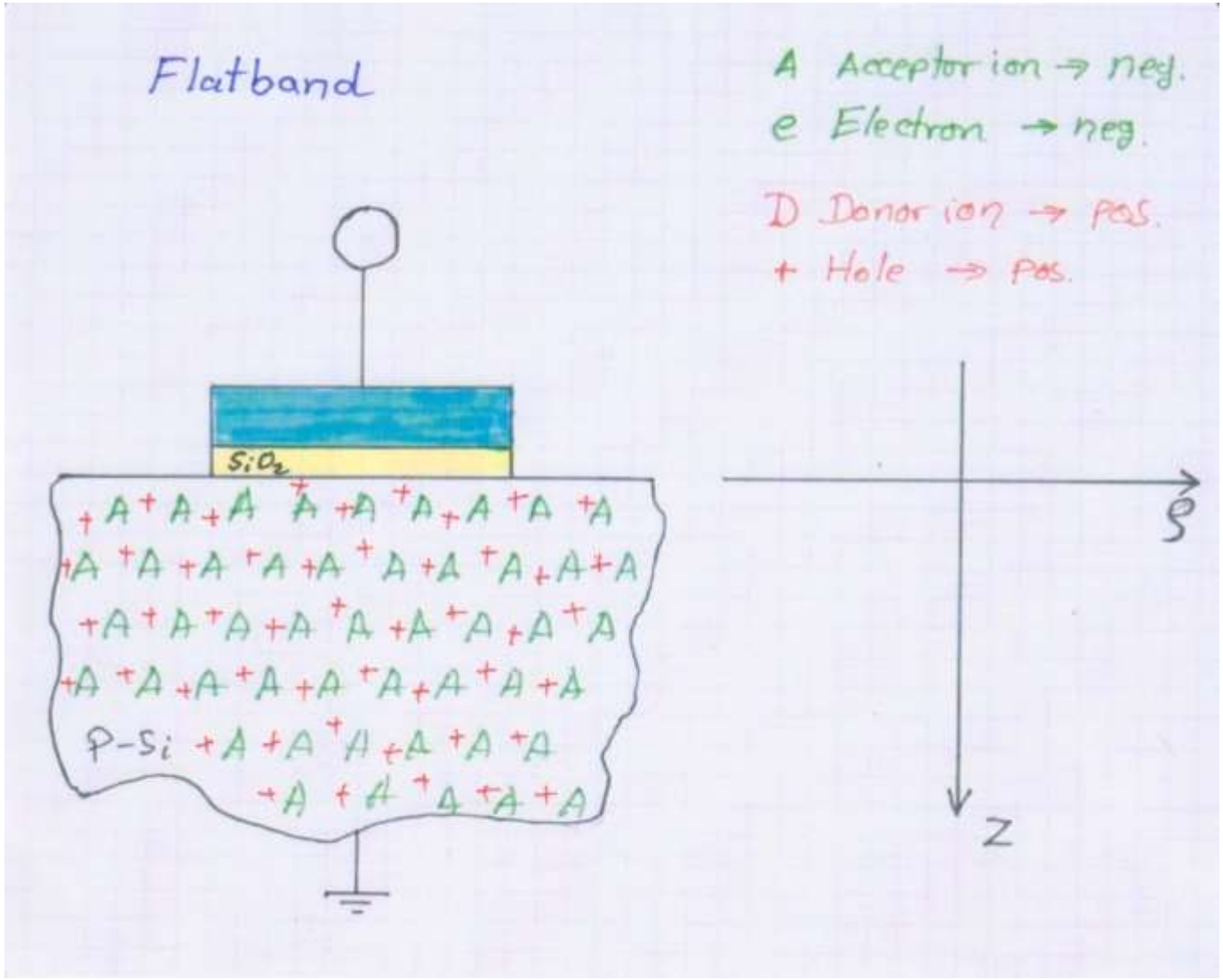
Today: MOS-CV +

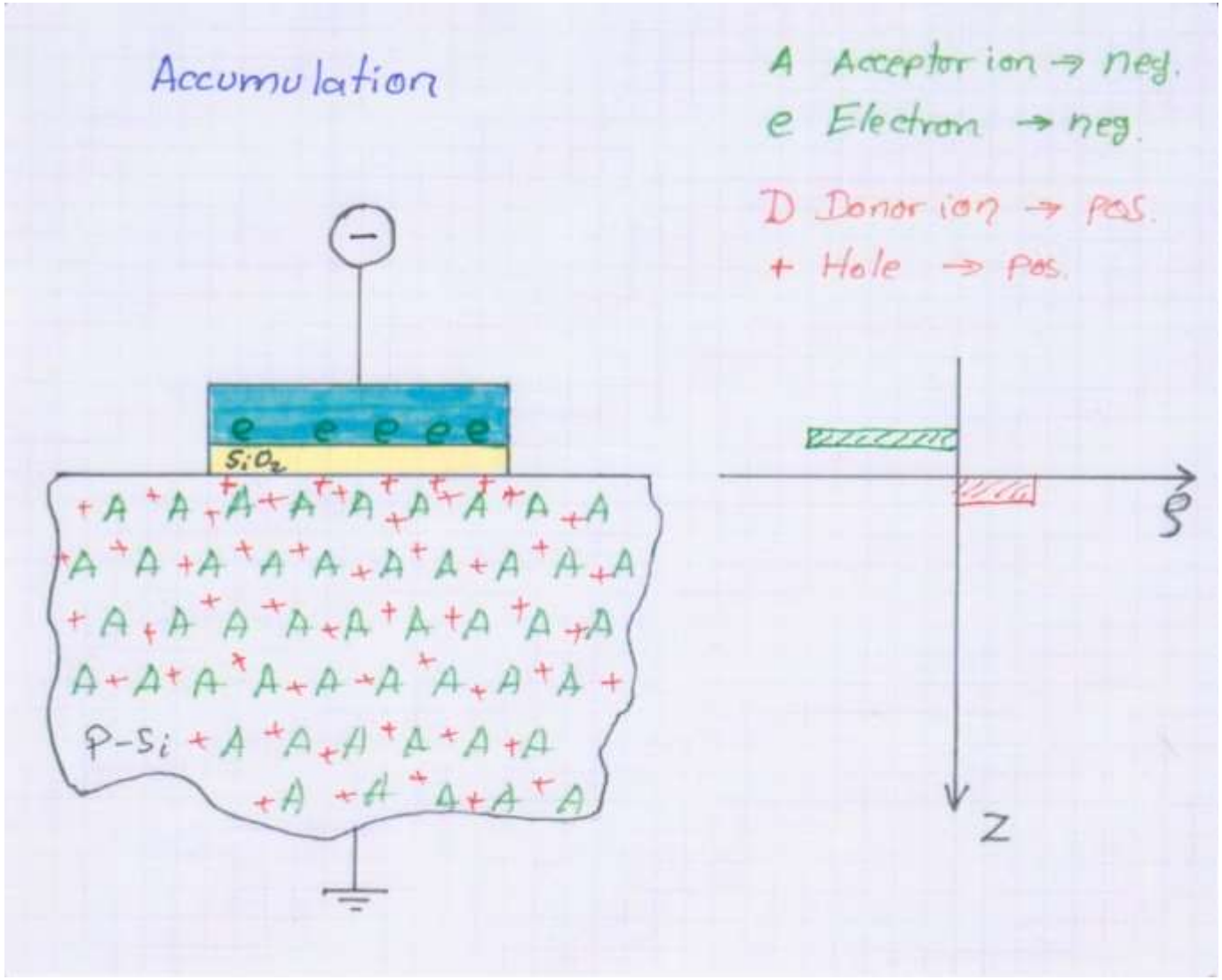
Continue

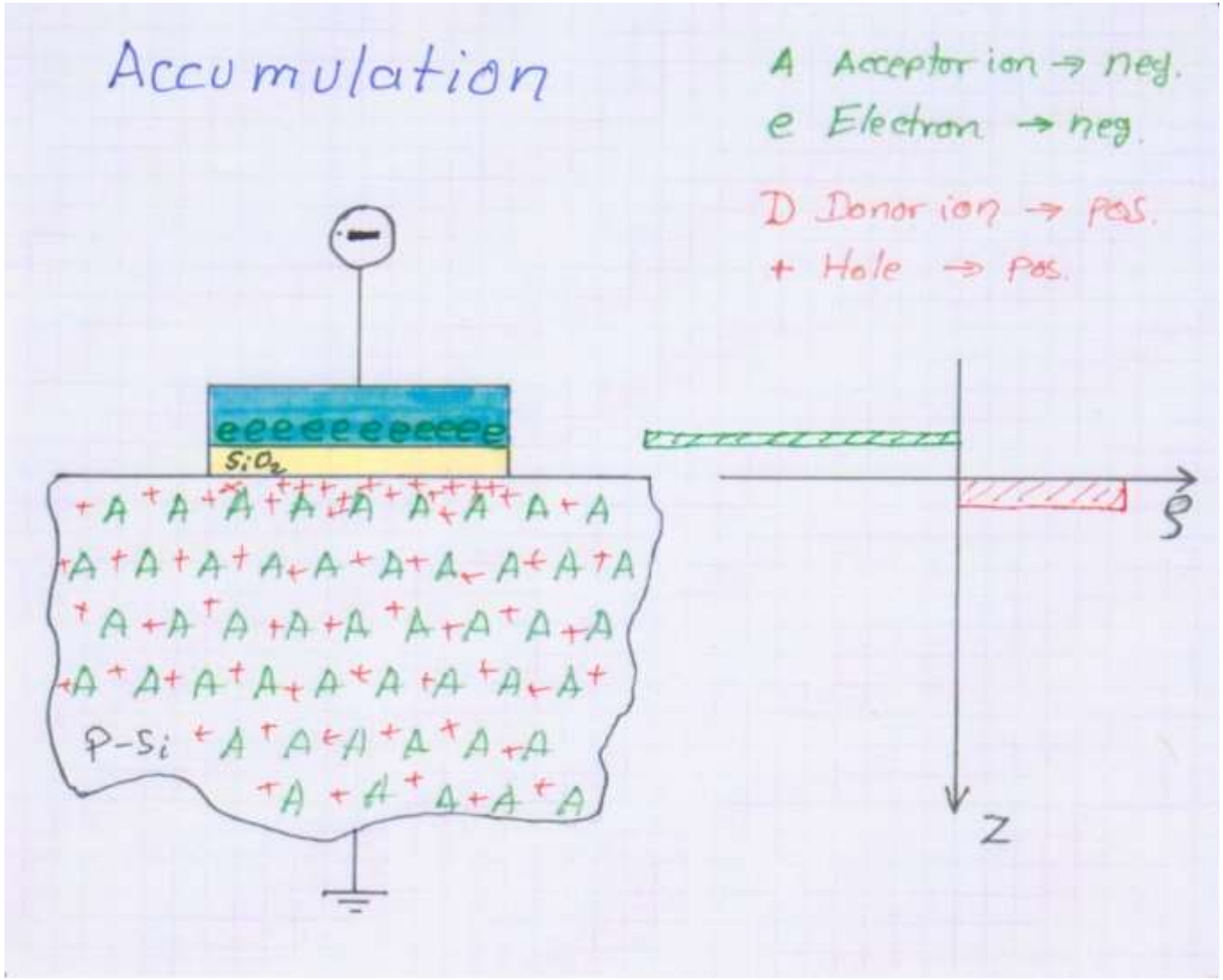
"SCT_SS20_05.2" 45:38

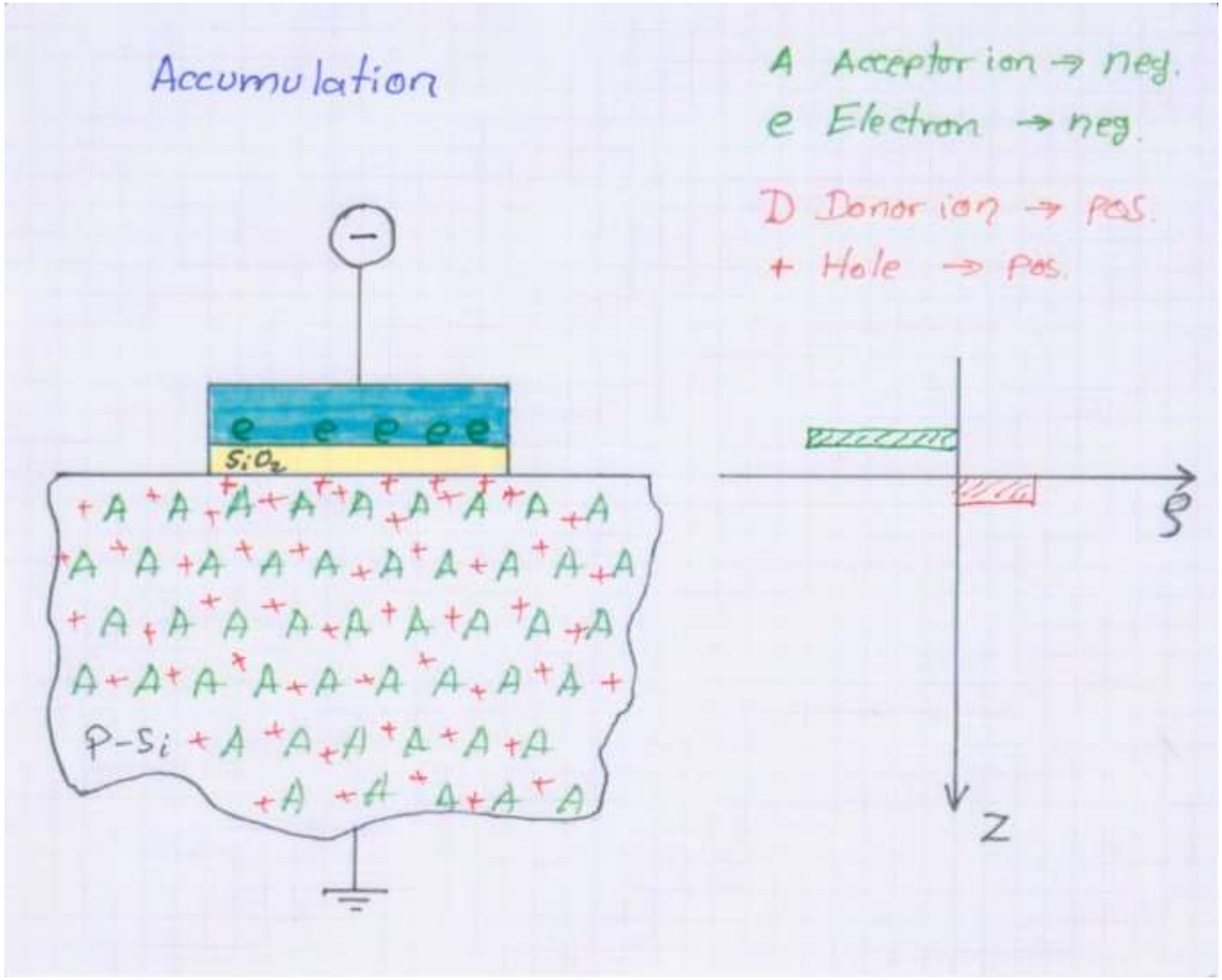
http://www.computerhistory.org/siliconengine/timeline/

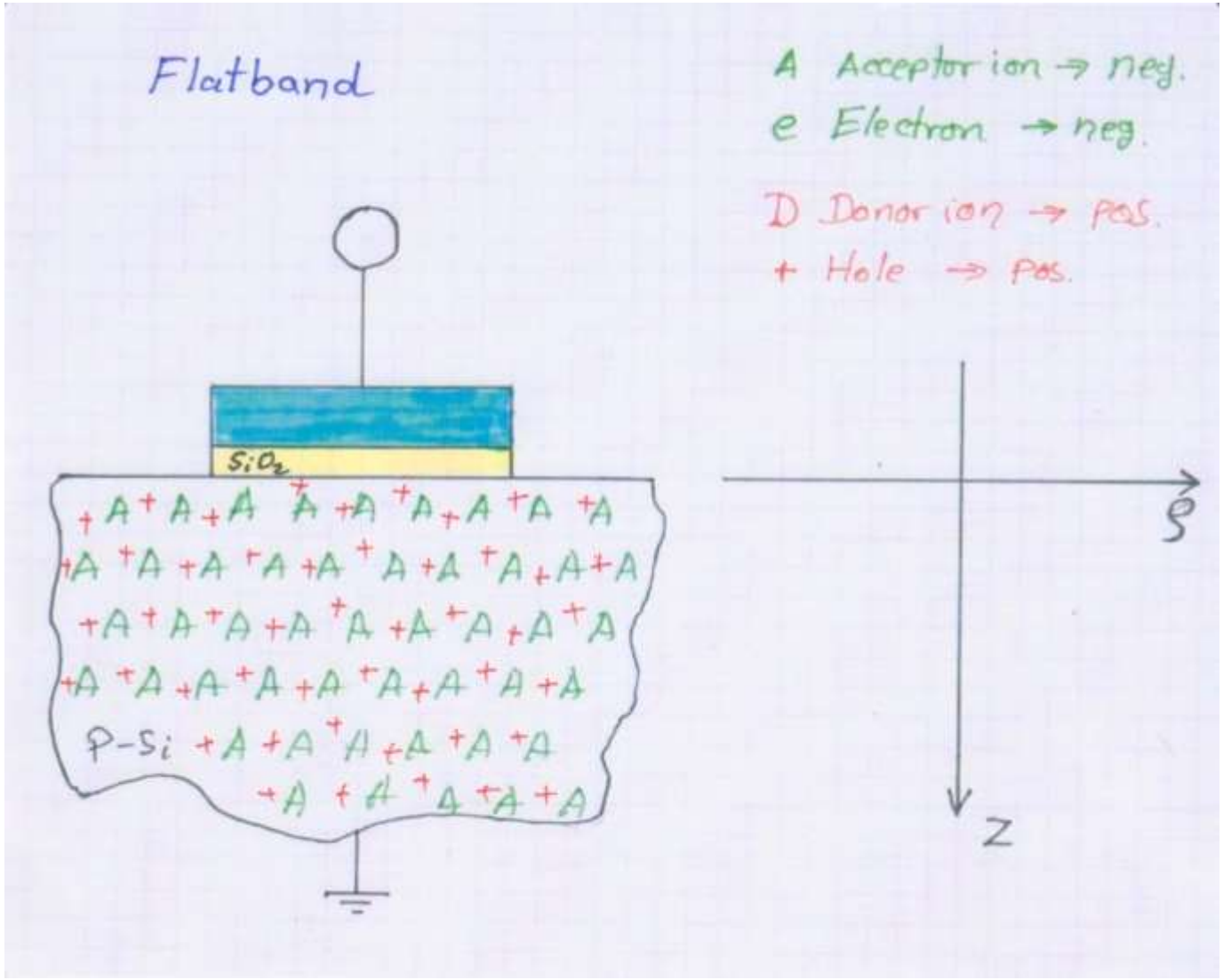

Acceptor Ion → neg immobile
Electron → mobile neg
+ hole → pos. mobile
ρ
x
$Q_A = Q_G$
$Q_G = Q_D$
$Q_G = Q_D + Q_i$
$Q_{inversion}$
P
Accumulation
Depletion
Inversion
i | n · P = const
i | 1 · 1 = 1
n | 1000 · 10^{-3} = 1
P | 10^{-3} · 1000 = 1 (n)
Gate
10^{-4} · 10^{4} = 1 (p)
0,1 · 10 = 1 (p)
1 · 1 = 1 (i)
10 · 0,1 = 1 (n)
inversion
1000 · 10^{-4} = 1 (n)
strong inversion

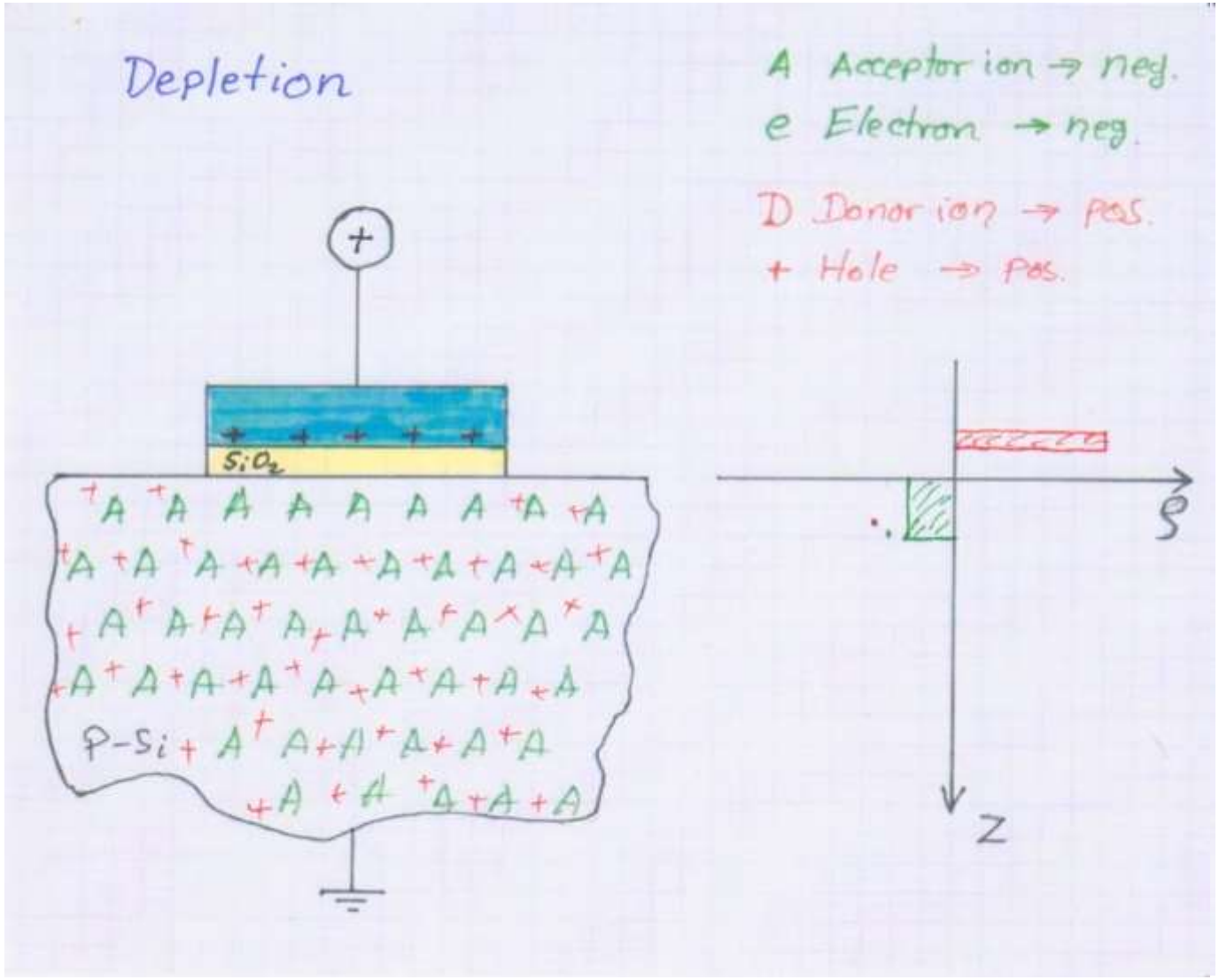

Flatband
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
SiO2
p-Si
ρ
z

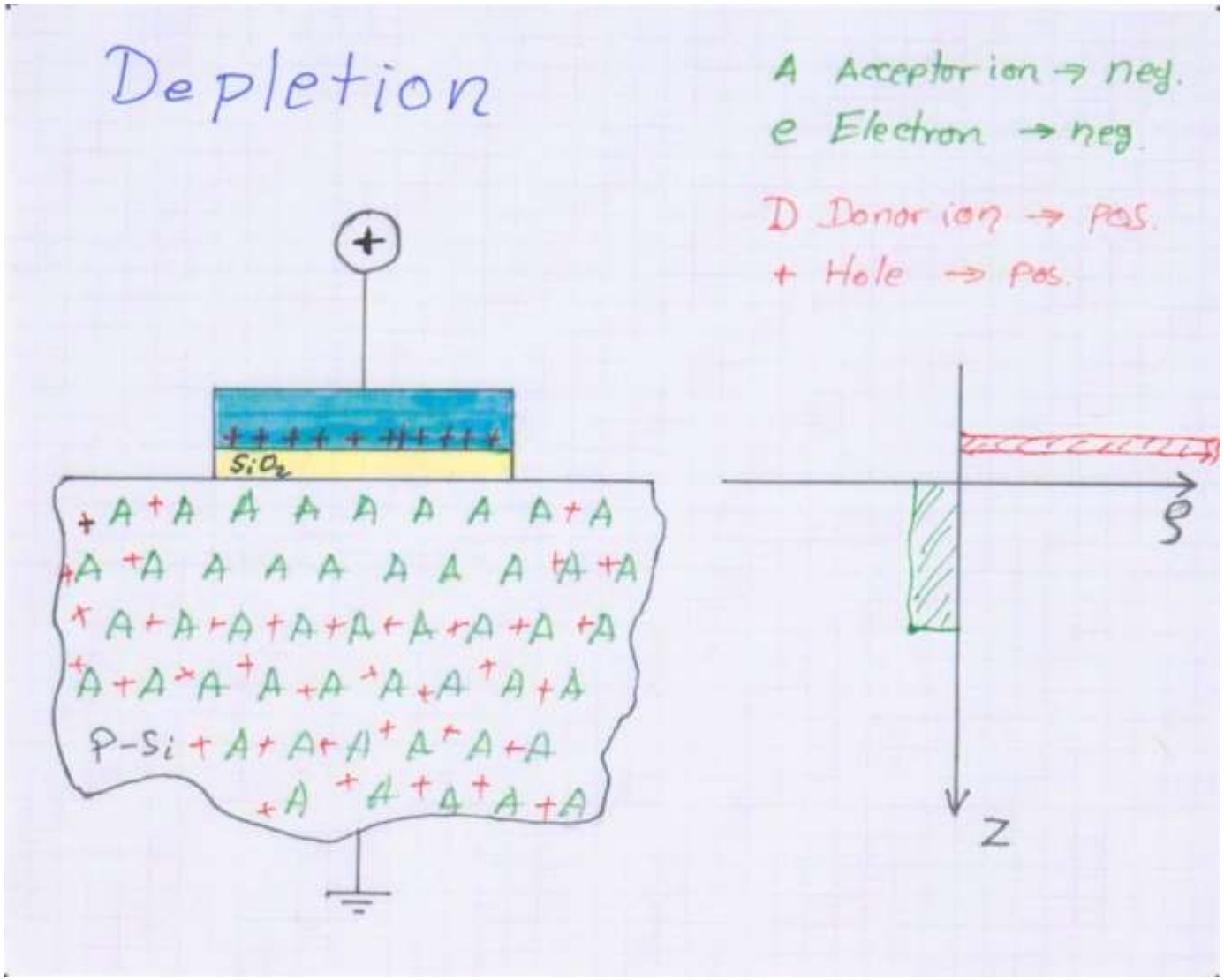

Accumulation
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
e e e e e
SiO2
p-Si
ρ
z

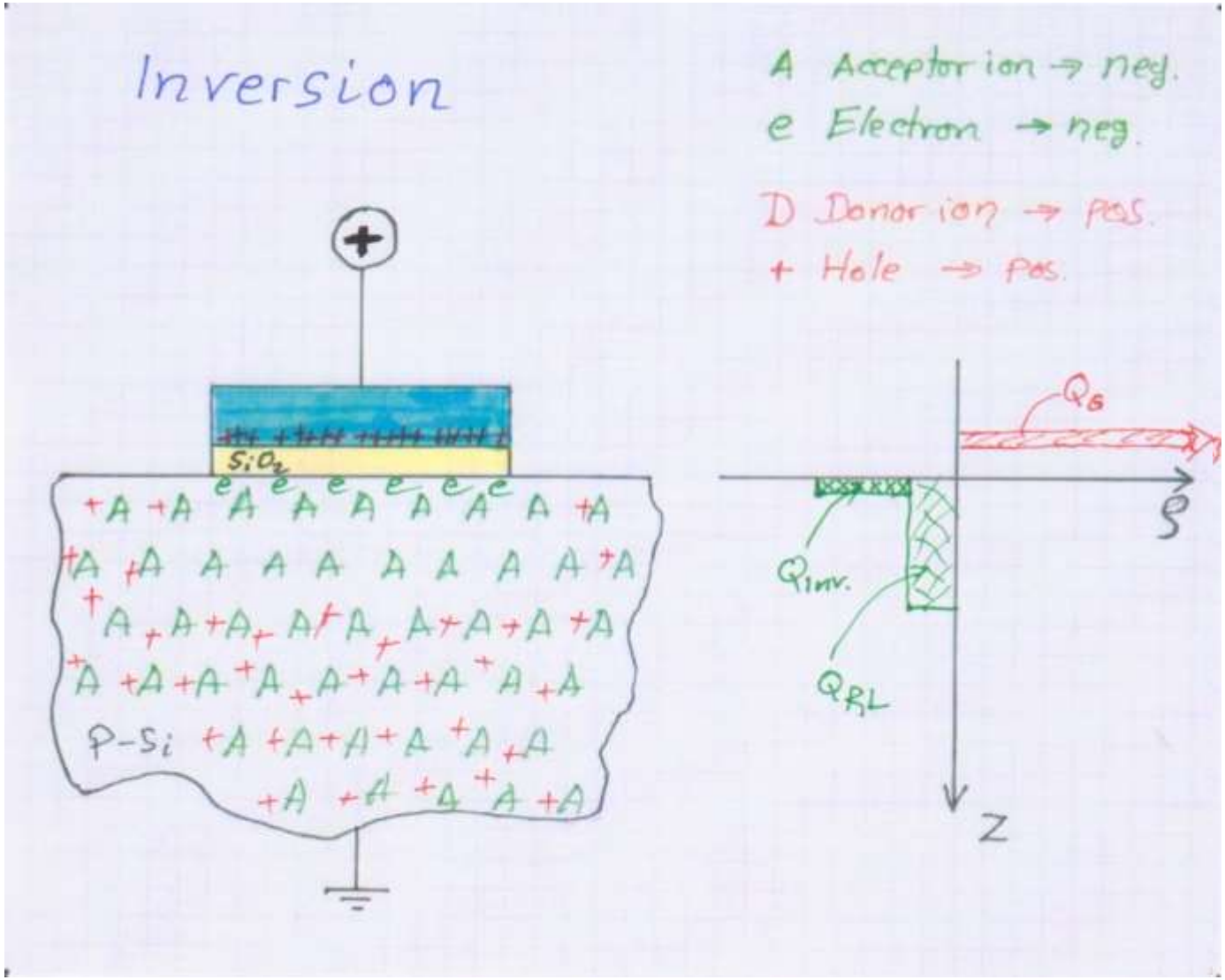

Accumulation
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
eeeeeeeeeee
SiO2
p-Si
ρ
z

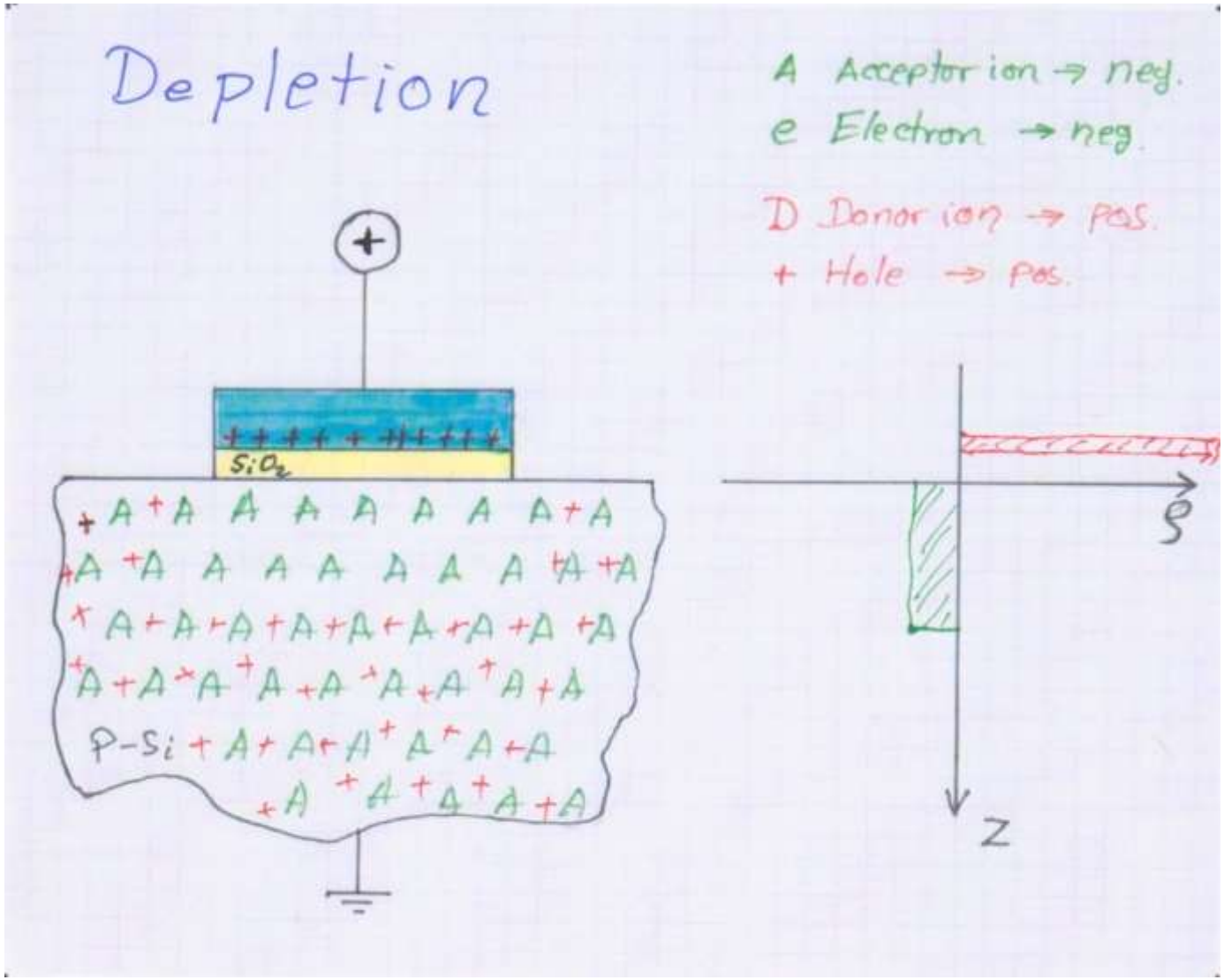

Accumulation
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
e e e e e
SiO2
p-Si
ρ
z

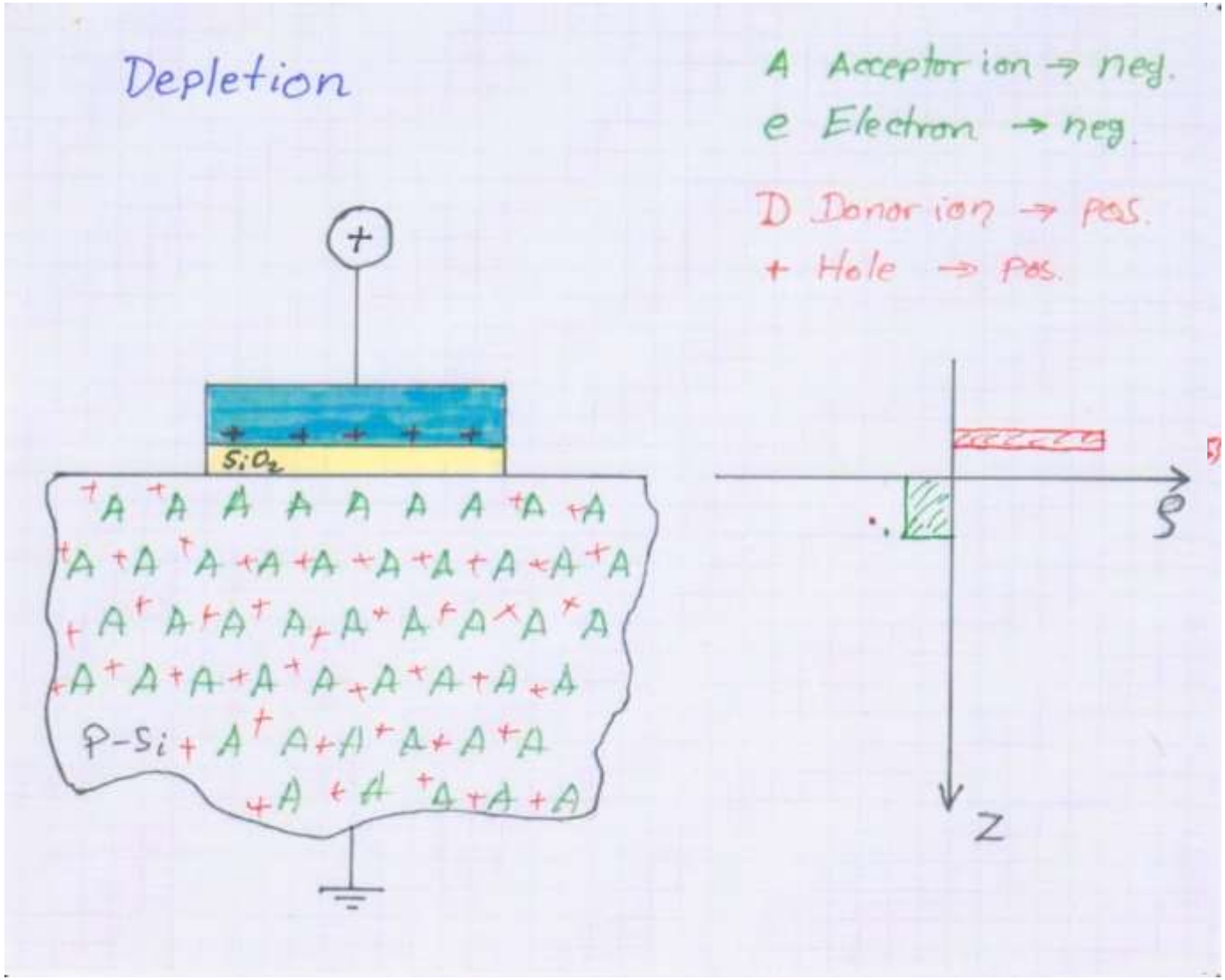

Flatband
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
SiO2
p-Si
ρ
z

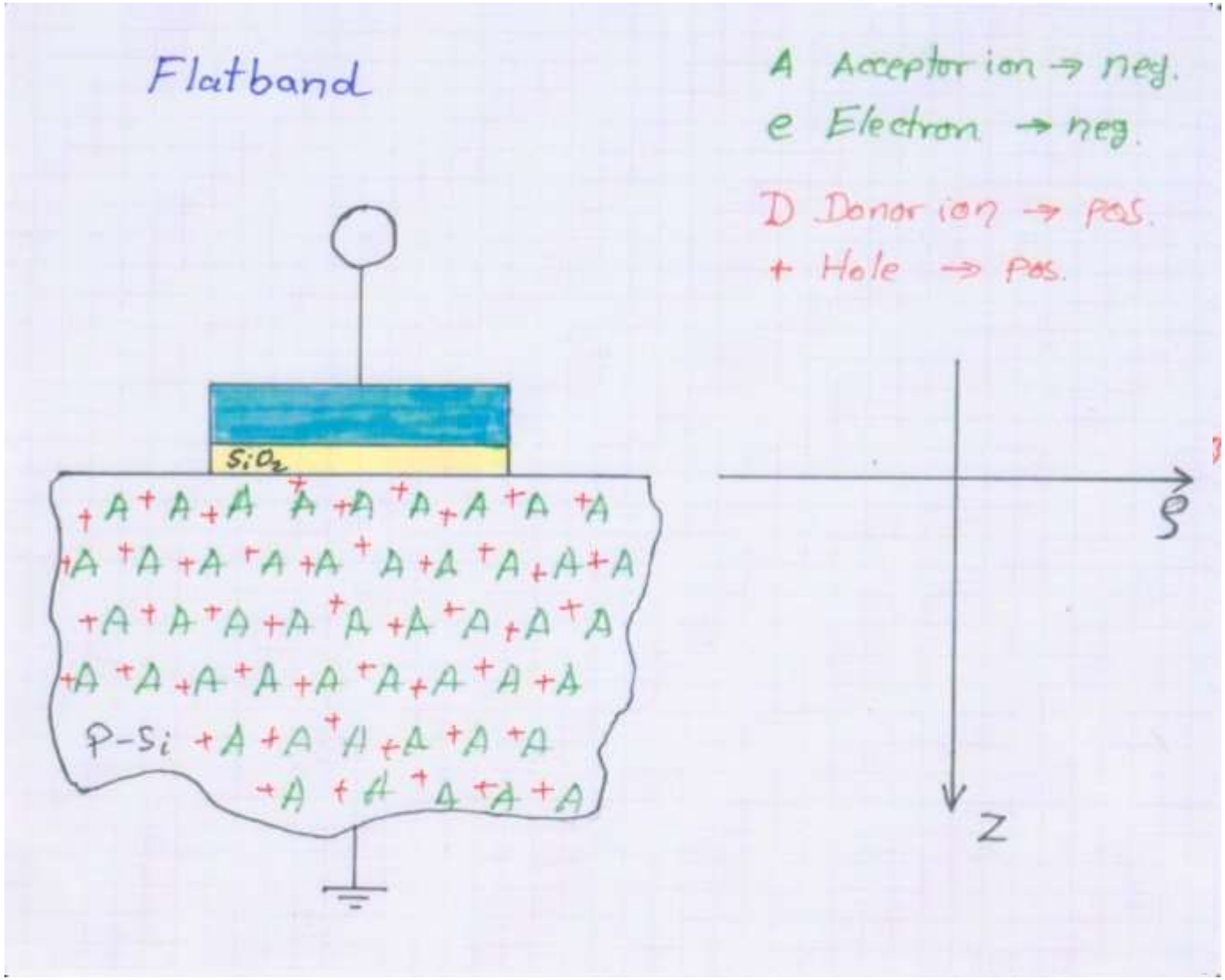

Depletion
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
+
SiO_2
p-Si
ρ
z

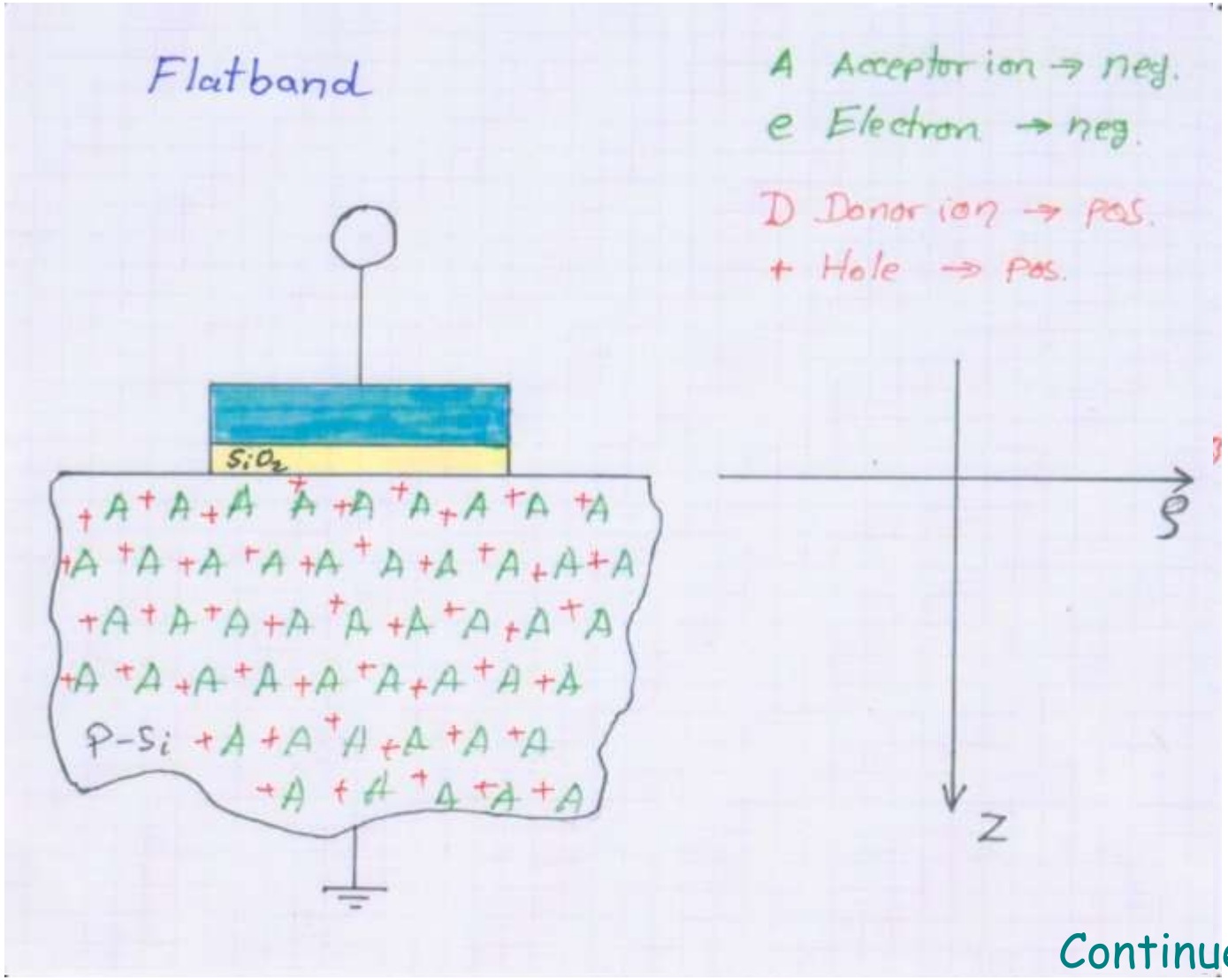

Depletion
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
SiO2
P-Si
ρ
z


Inversion
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
SiO_2
P-Si
Q_G
$Q_{inv.}$
Q_{RL}
S
Z


Depletion
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
+
SiO_2
P-Si
ρ
z


Depletion
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
+
SiO_2
p-Si
ρ
z

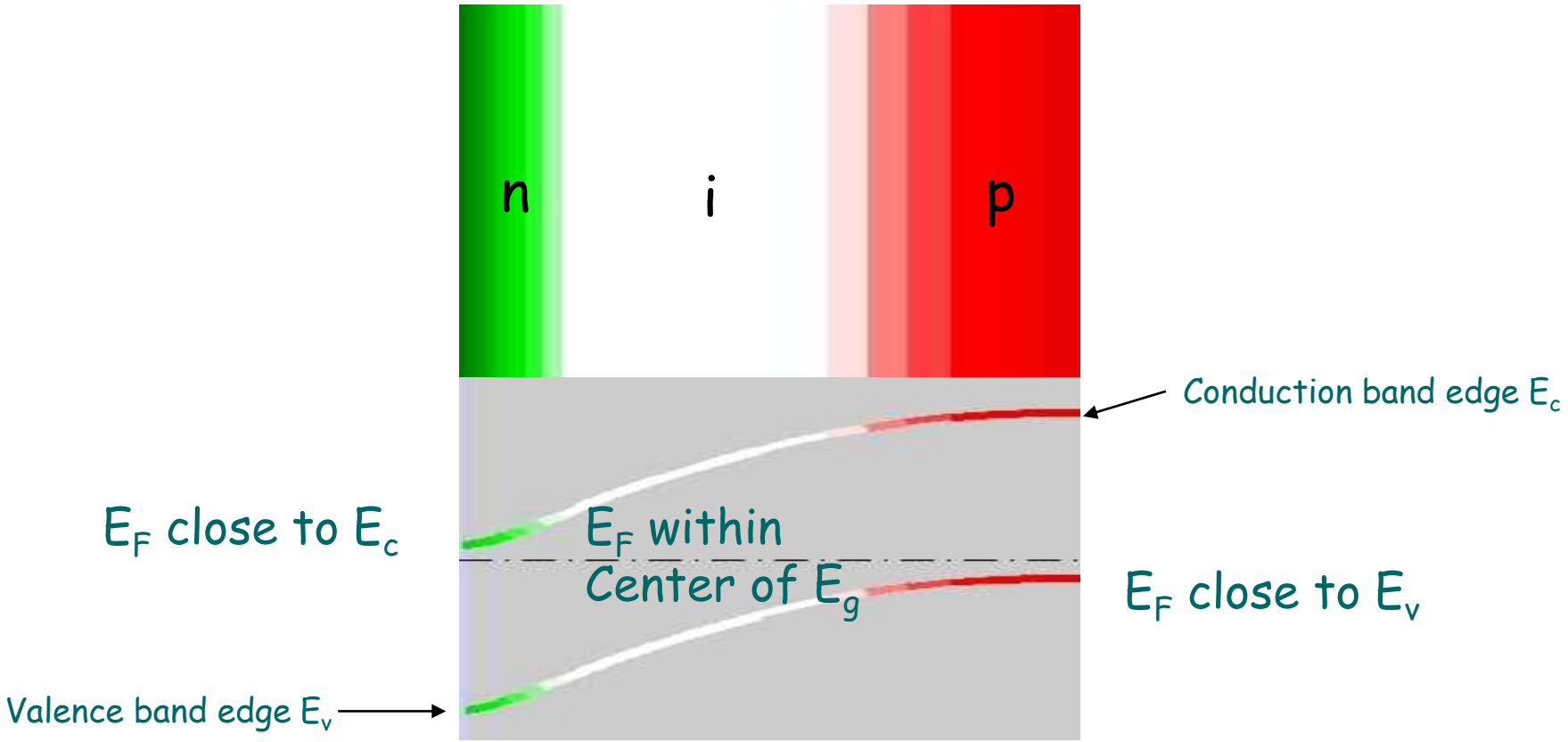

Flatband
A Acceptor ion → neg.
e Electron → neg.
D Donor ion → pos.
+ Hole → pos.
SiO2
p-Si
ρ
z



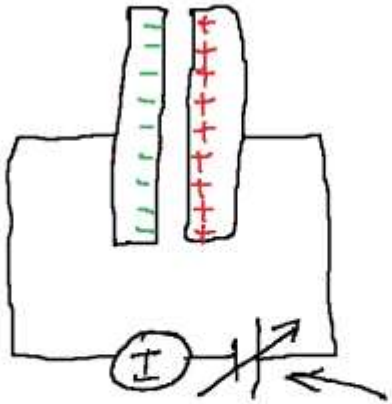
Continue

"SCT_SS20_05.03" 45:19

Relation between Position of E_F and majority carrier concentration



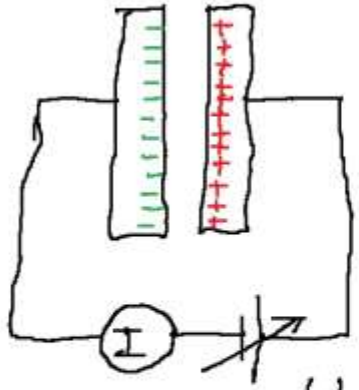
Capacitance



$Q = \int I(t)\,dt$ U

$$C = \frac{Q}{U}$$

Differential Capacitance

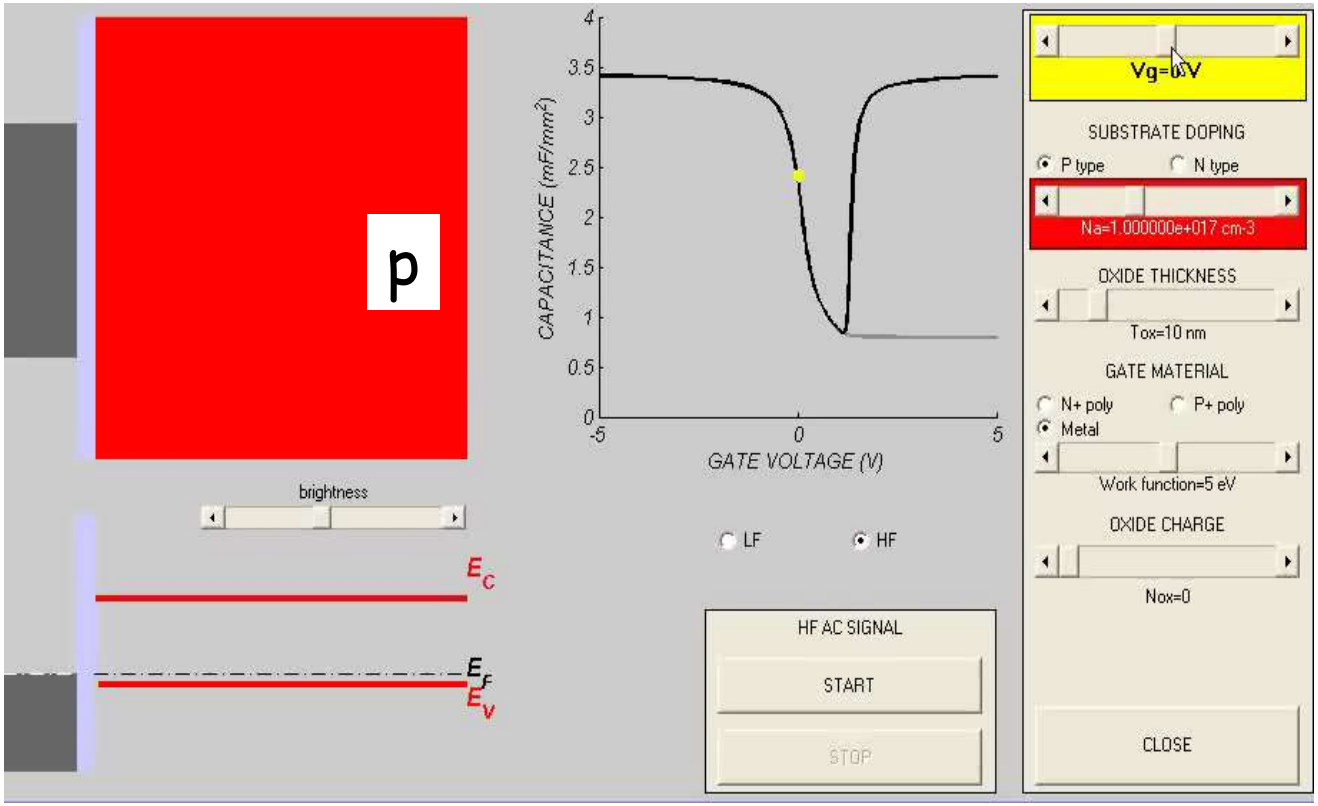


$U = U_0 + \Delta U(\omega)$

$Q = Q_0 + \Delta Q \leftarrow \int_0^{T_2} I(t)\,dt$

$$C_{diff} = \frac{\Delta Q}{\Delta U}$$

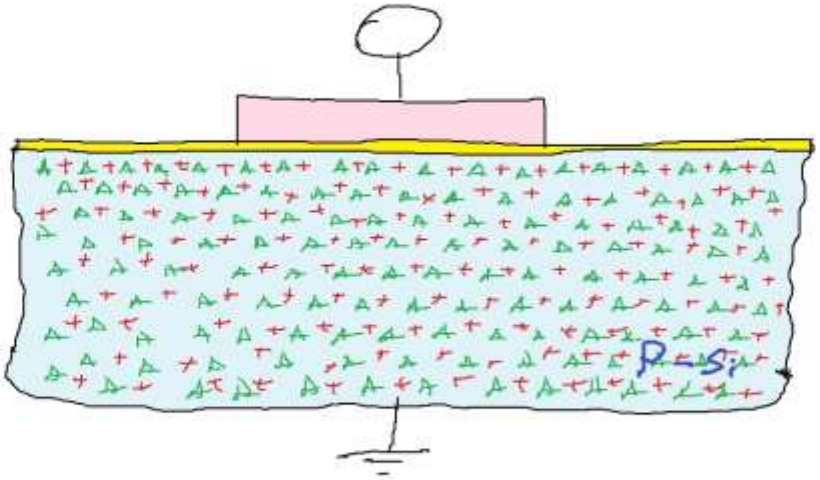
MOS Capacitance = $f(V_G)$



Terms:
- accumulation
- depletion
- inversion

Dependency on:
- oxide thickness
- doping level

Please pay attention to the pdf MOScapAnim in OPAL



A neg acceptor
e (neg) electron
+ (pos) hole
D pos donor

»Wissen schafft Brücken.«