The hyperlinks to the video streams in this virtual lecture are marked by the Video Campus Sachsen Logo. To watch them you need to be logged on at the host: VCS. Please click on: https://videocampus.sachsen.de/login select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 - Process Integration

6. Web-based virtual Lecture: May 20 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here → VIDEO CAMPUS SACHSEN

"SCT_SS21_06.1" 05:00

TECHNISCHE UNIVERSITÄT DRESDEN

This document including the contained video streams is only available to students of the lecture „Semiconductor Technology 2“ at TU-Dresden.
It must not be copied and published outside of TUD!
It is intended for
TUD internal use only!

TECHNISCHE UNIVERSITÄT DRESDEN

Outline

SC-Basics

Review:
- SC-Basics
- DRAM Device
- POLYCIDE
- RIE
- MOS Capacitor
- Feld/Gate Oxide
- EOT
- MOS-Cap-CV ..

Today: MOSFET +

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

Outline

TECHNISCHE UNIVERSITÄT DRESDEN

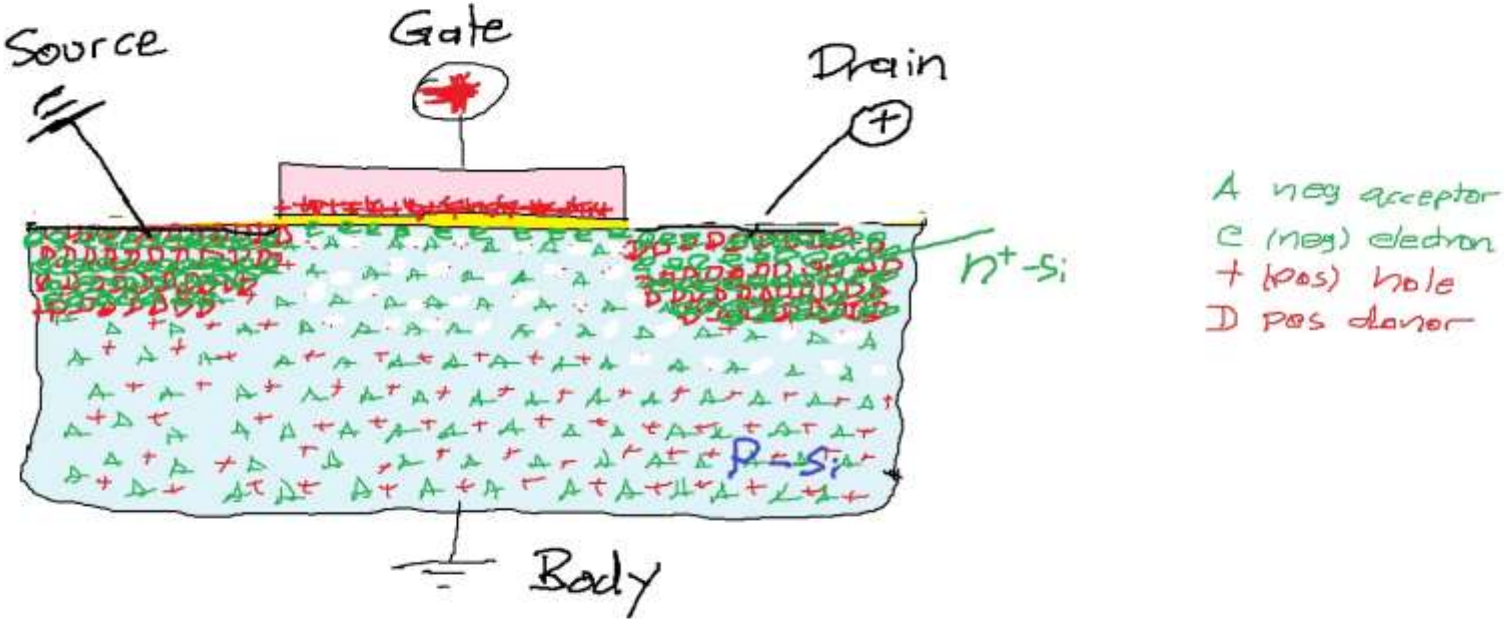
Review:
- SC-Basics
- DRAM Device
- POLYCIDE
- RIE
- MOS Capacitor
- Feld/Gate Oxide
- EOT
- MOS-Cap-CV ..

Today: MOSFET +

Continue → VIDEO CAMPUS SACHSEN

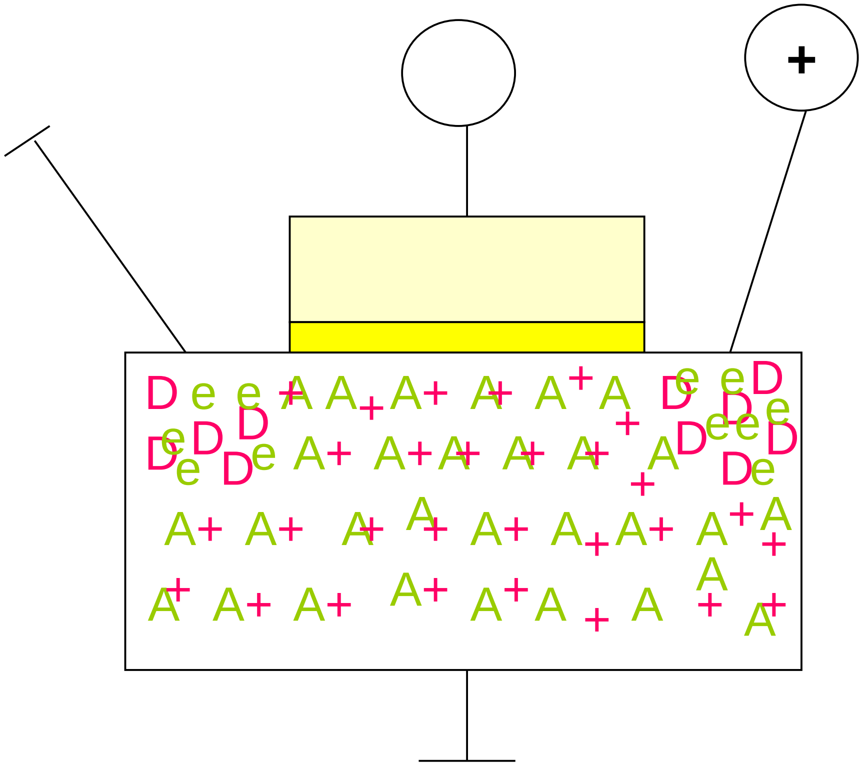
"SCT_SS20_06.2" 16:29

http://www.computerhistory.org/siliconengine/timeline/


Source
Gate
Drain
Body
n+-Si
p-Si
A neg acceptor
e (neg) electron
+ (pos) hole
D pos donor

MOS Capacity plus source + drain

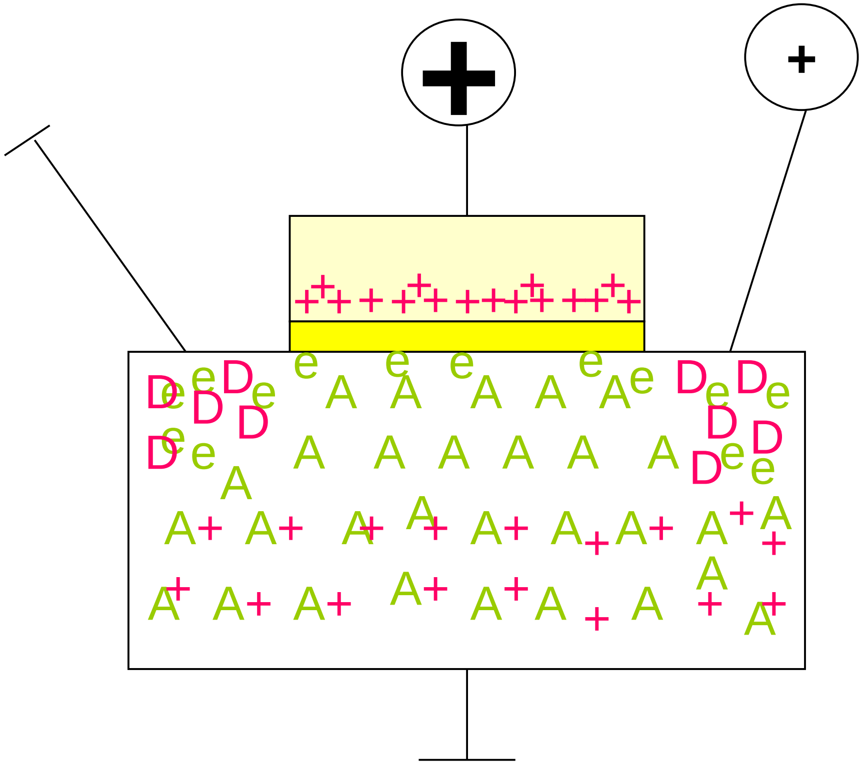
Current can not flow!



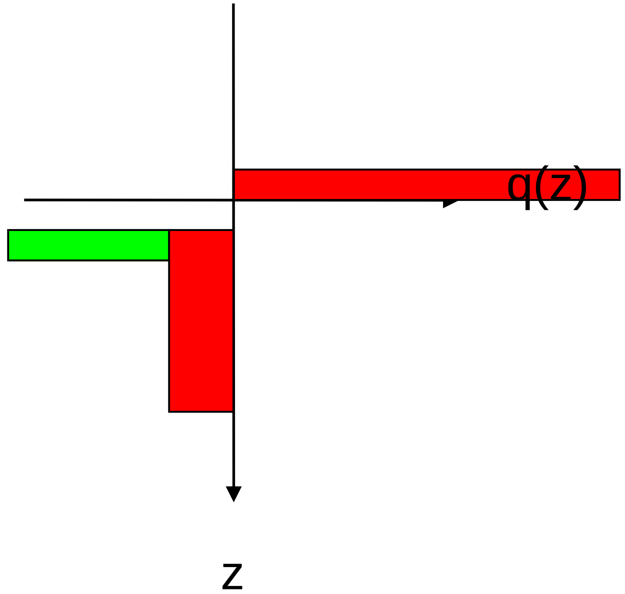
D = pos. charged donor
A = neg. charged acceptor
+ = pos. charge (hole)
e = neg. charge (electron)

MOS Capacity

Current can flow!



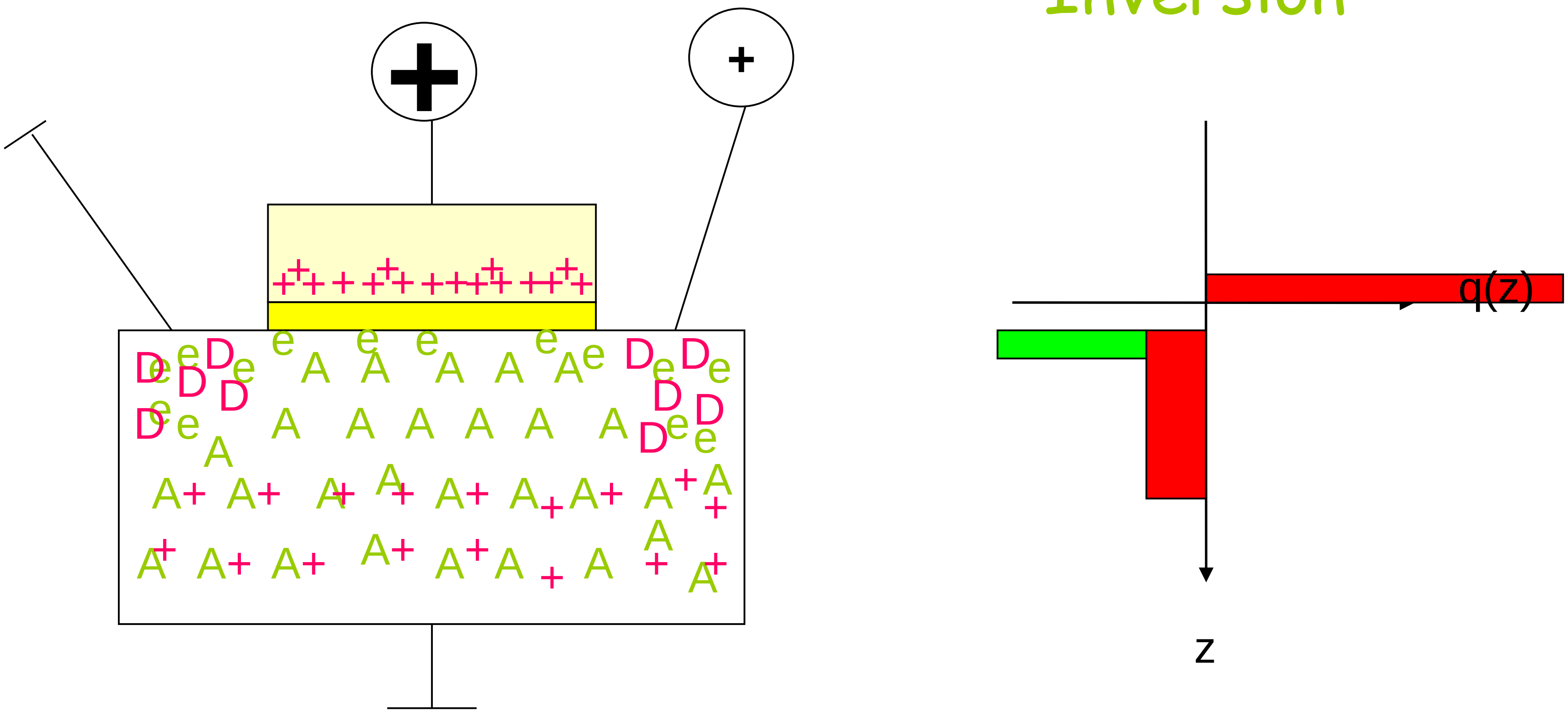
Inversion



MOS Capacity

Current can flow!

Inversion

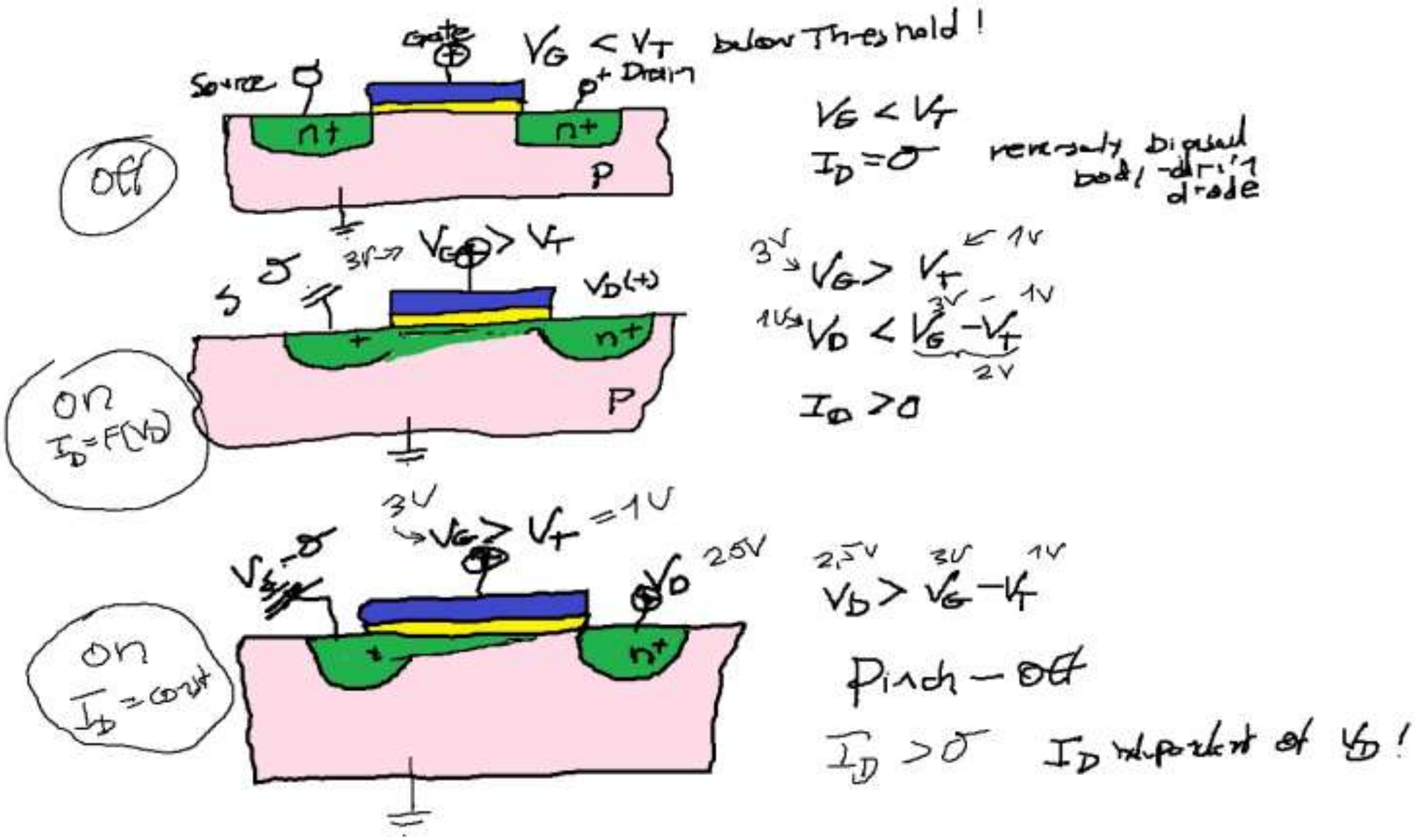


Continue → VIDEO CAMPUS SACHSEN

"SCT_SS20_06.03" 23:51

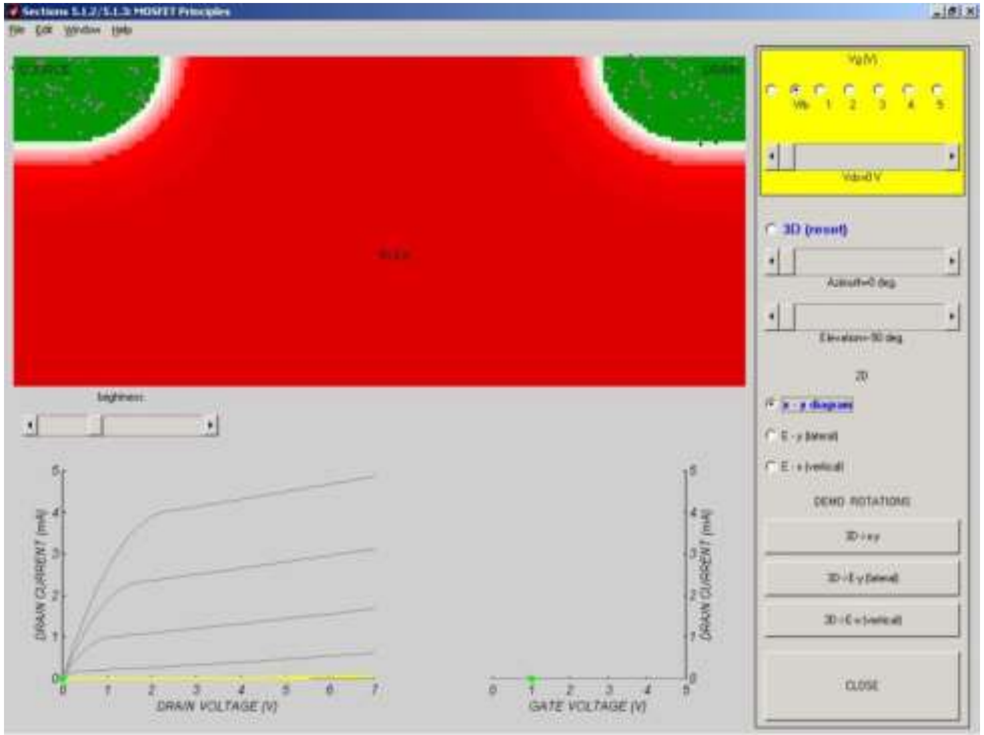
Blackboard

Blackboard


Gate
Source
Drain
$V_G < V_T$ below Threshold !
n+
n+
p
off
$V_G < V_T$
$I_D = 0$
reversely biased body-drain diode
$V_G > V_T$
$V_D(+)$
n+
P
on
$I_D = F(V_D)$
$V_G > V_T$
$V_D < V_G - V_T$
2V
$I_D > 0$
$V_G > V_T = 1V$
25V
n+
on
I_D = const
$V_D > V_G - V_T$
Pinch-off
$I_D > 0$
I_D independent of V_D !

Transistor Behavior

The MOS FET

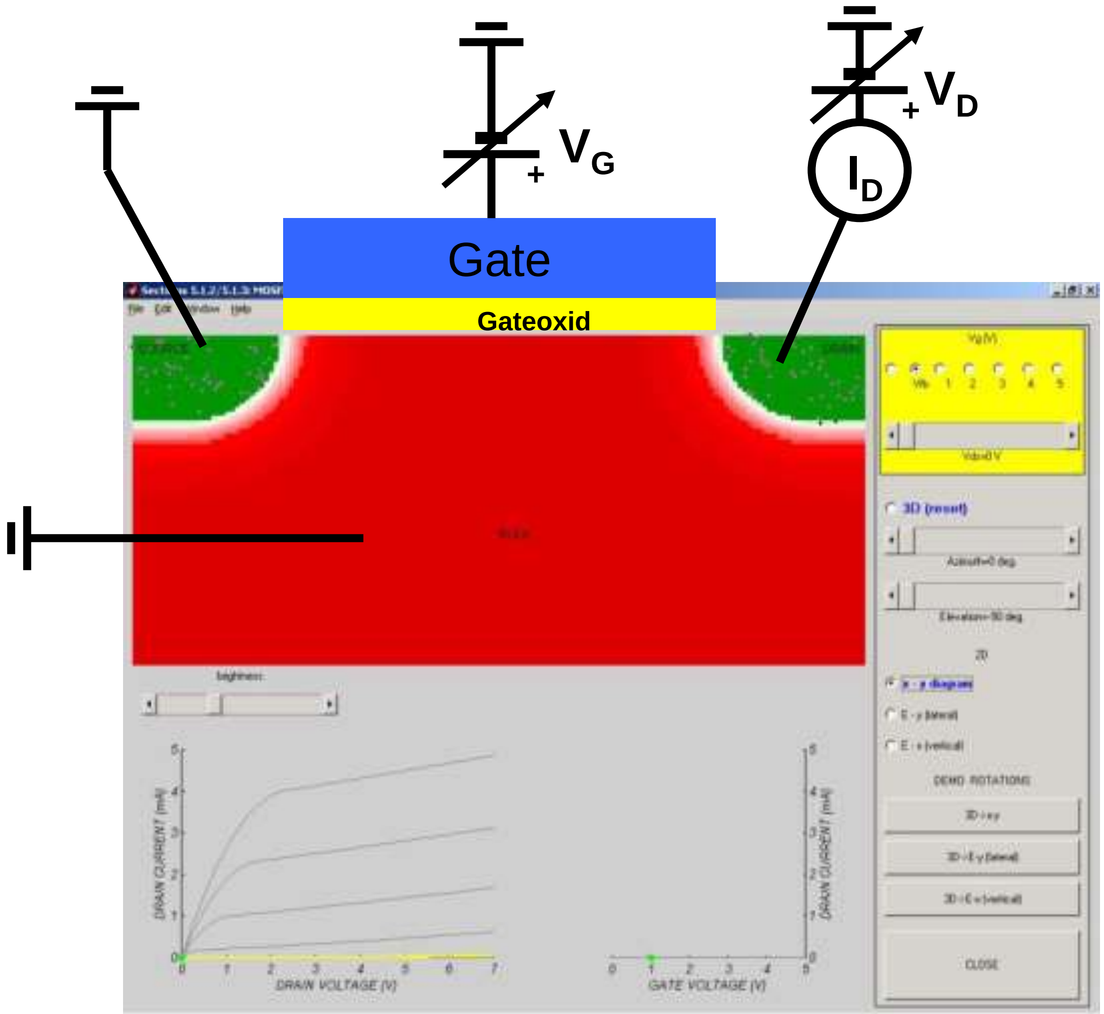


Sima Dimitrijev, Understanding Semiconductor Devices, Oxford University Press 2000

Terms:
- accumulation
- depletion
- inversion
-threshold voltage
- pinch off
- saturation current
- triode mode

Start: FETsimE .pdf

Transistor Behavior



Sima Dimitrijev, Understanding Semiconductor Devices, Oxford University Press 2000

The MOS FET

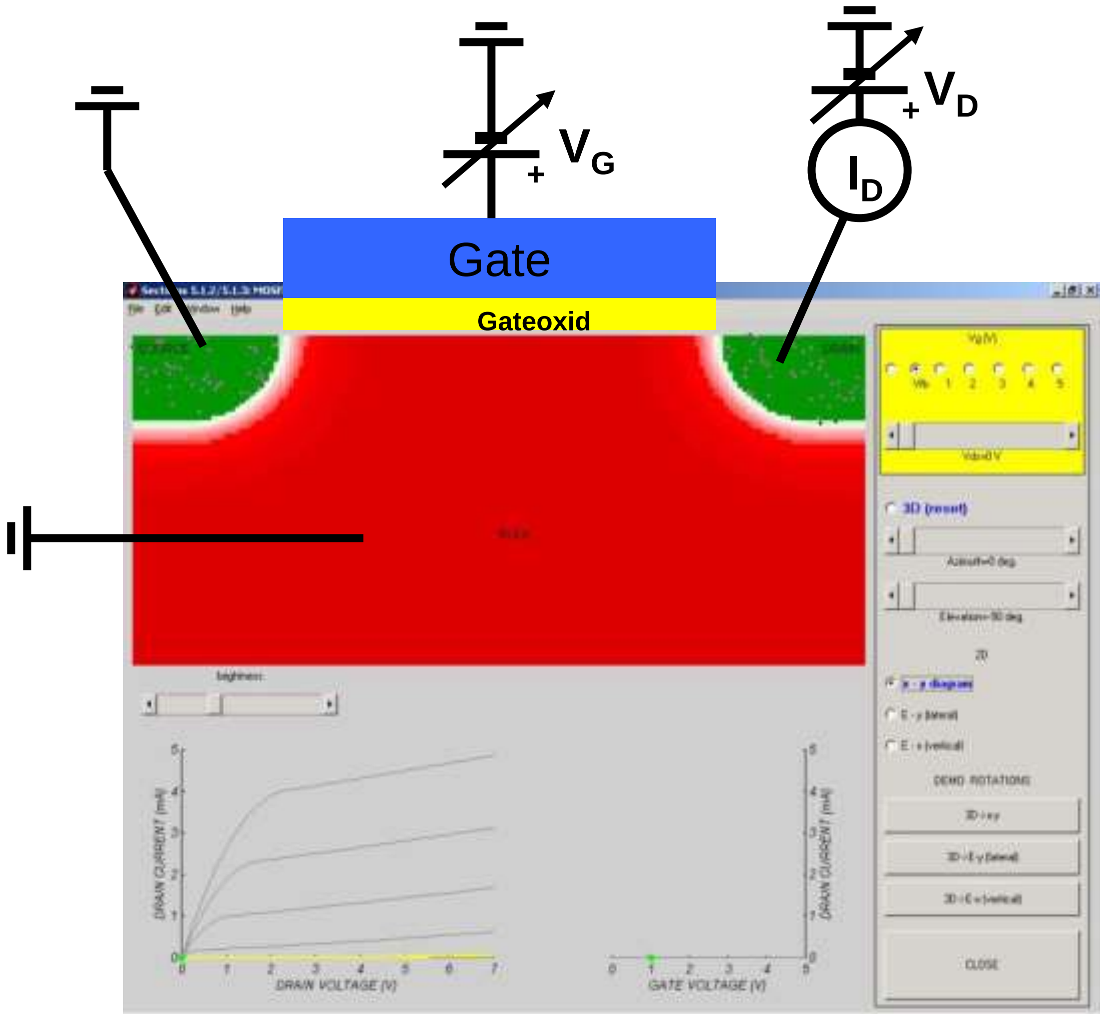
Terms:

- accumulation
- depletion
- inversion
- threshold voltage
- pinch off
- saturation current
- triode mode

Start:
FETsimE
.pdf

Continue
"SCT_SS20_06.04" 15:21

Transistor Behavior



Sima Dimitrijev, Understanding Semiconductor Devices, Oxford University Press 2000

The MOS FET

Terms:

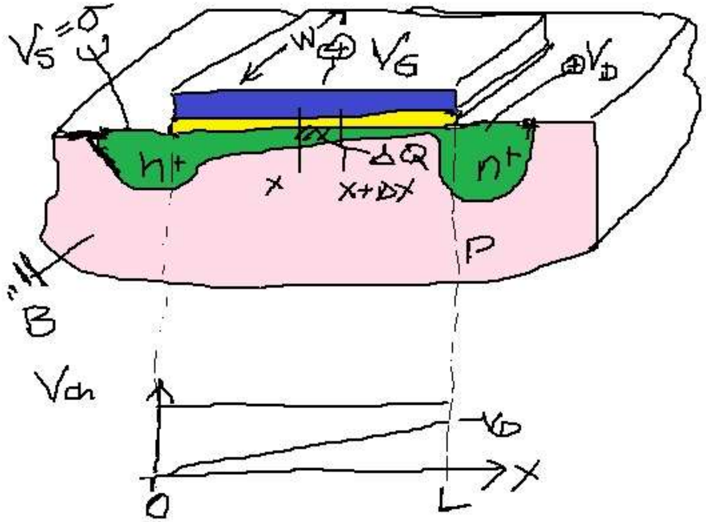
- accumulation
- depletion
- inversion
- threshold voltage
- pinch off
- saturation current
- triode mode

Start: FETsimE.pdf

Continue
"SCT_SS20_06.05" 46:10

Blackboard

Blackboard



- Gate Capacity $C_G = \frac{\varepsilon_0 \varepsilon_r W \cdot L}{d_{ox}}$
- Capacity over Δx $\Delta C = C_G \frac{\Delta x}{L}$
- Charge within Δx
  $\Delta Q = \Delta C (V_G - V(x))$
- El. Field in x $E = -\frac{dV}{dx}$
- velocity of e in the channel
  $v = -\mu E = \mu \frac{dV}{dx}$ / μ ≙ mobility
- carrier density per Length
  $\rho_x = \frac{\Delta Q}{\Delta x}$

Current $I_D = \rho_x v = \frac{\Delta Q}{\Delta x} \mu \frac{dV}{dx} = \frac{\Delta C (V_G - V(x))}{\Delta x} \mu \frac{dV}{dx}$

$$I_D = \frac{C_G \cdot \Delta x (V_G - V(x))}{L \Delta x} \mu \frac{dV}{dx} \qquad \frac{C_G \mu}{L} (V_G - V(x)) \frac{dV}{dx}$$

$$I_D \int_0^L dx = \frac{C_G \mu}{L} \int_0^{V_D} (V_G - V(x))\, dV \qquad \frac{C_G \mu}{L} \left(\int_0^{V_D} V_G\, dV - \int V(x)\, dV \right)$$

$$I_D L = \frac{C_G \mu}{L} \left(V_G V_D - \frac{1}{2} V_D^2\right) = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W L}{L} \left(V_G V_D - \frac{1}{2} V_D^2\right)$$

So far V_T is not considered To repair $V_G \rightarrow V_G - V_T$

$$I_D = \frac{\mu \varepsilon_r \varepsilon_0}{d_{ox}} \frac{W}{L} \left\{ (V_G - V_T) V_D - \frac{1}{2} V_D^2 \right\}$$

Blackboard

Max $I_D'(V_D) = 0$ $\quad (V_G - V_T) - V_D = 0$

Max at $V_D = (V_G - V_T)$ Pinch off condition

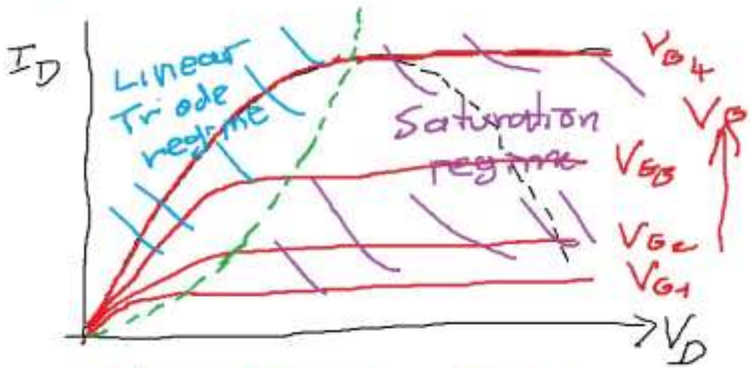
$$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W}{L} \left\{ (V_G - V_T) \cdot V_D - \frac{1}{2} V_D^2 \right\}$$

Pinch off at $V_D = V_G - V_T$

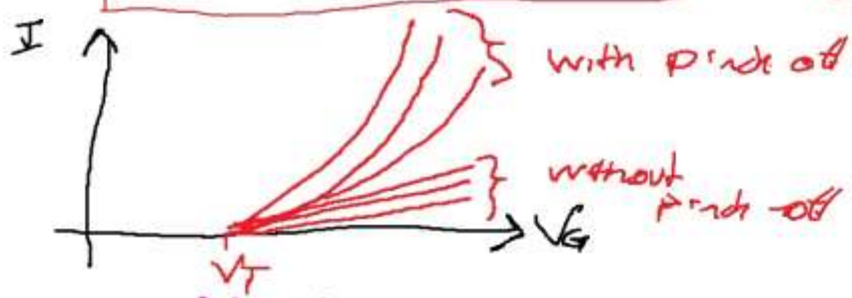
$$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W}{L} \left\{ (V_G - V_T)(V_G - V_T) - \frac{1}{2} (V_G - V_T)^2 \right\}$$

$$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{2\, d_{ox}} \frac{W}{L} (V_G - V_T)^2$$

independent of V_D !



Characteristic Curve



Transfer Curve

1.3 Transistor equation

For the range $V_D=0$ to $V_D=V_G-V_T$

$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{d_{ox}}\frac{W}{L}\left\{(V_G - V_T)(V_D) - \tfrac{1}{2}(V_D)^2\right\}$$

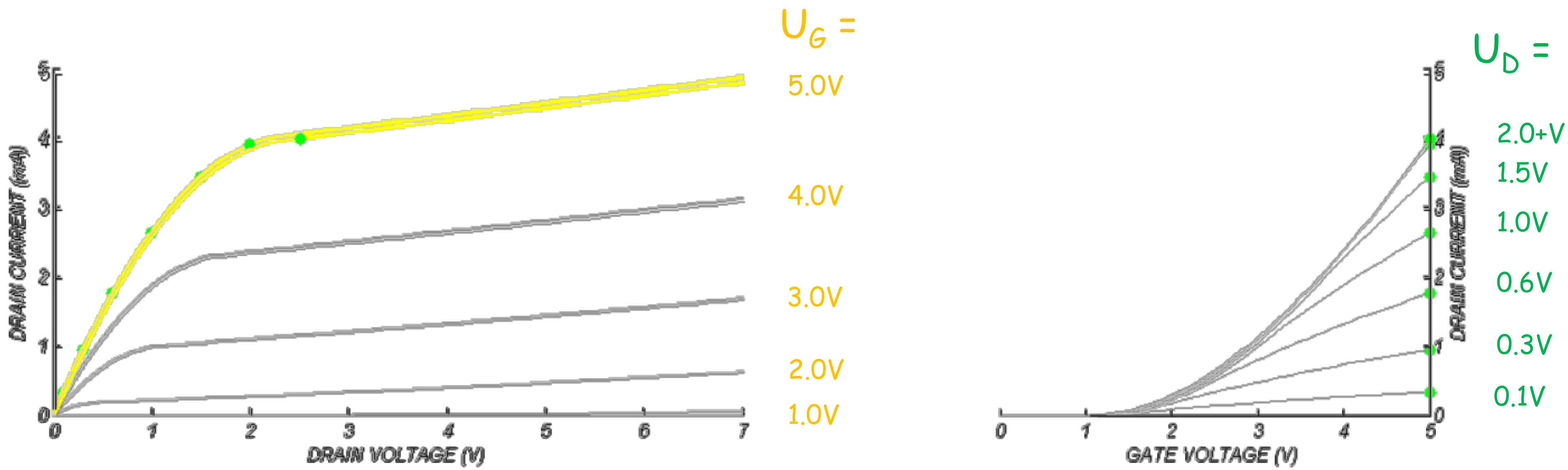
Pinch-Off at:

$$V_D = V_G - V_T$$

From there on:

$$I_{Dsat} = \frac{\mu\varepsilon_0\varepsilon_r}{2d_{ox}}\frac{W}{L}(V_G - V_T)^2$$

Independent of V_D



1.3 Transistor equation

For the range V_D=0 to $V_D=V_G-V_T$

$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{d_{ox}}\frac{W}{L}\left\{(V_G - V_T)(V_D) - \tfrac{1}{2}(V_D)^2\right\}$$

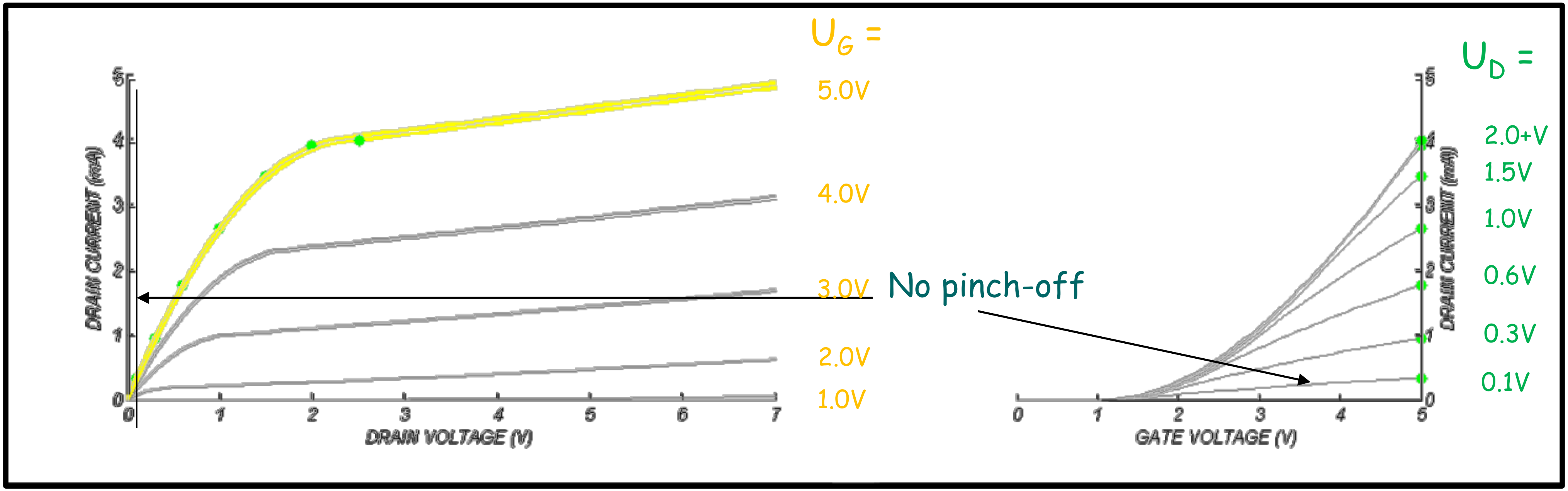
Pinch-Off at:

$$V_D = V_G - V_T$$

From there on:

$$I_{Dsat} = \frac{\mu\varepsilon_0\varepsilon_r}{2d_{ox}}\frac{W}{L}(V_G - V_T)^2$$

Independent of V_D



1.3 Transistor equation

For the range V_D=0 to V_D=V_G-V_T

$$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W}{L} \left\{ (V_G - V_T)(V_D) - \tfrac{1}{2}(V_D)^2 \right\}$$

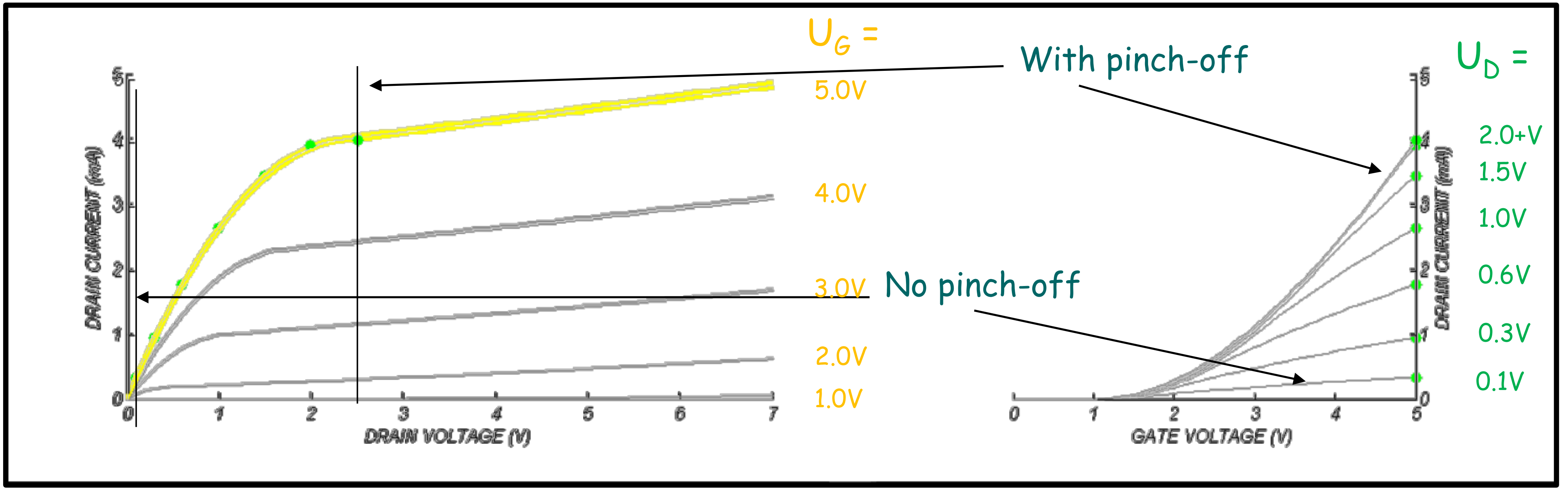
Pinch-Off at:

$$V_D = V_G - V_T$$

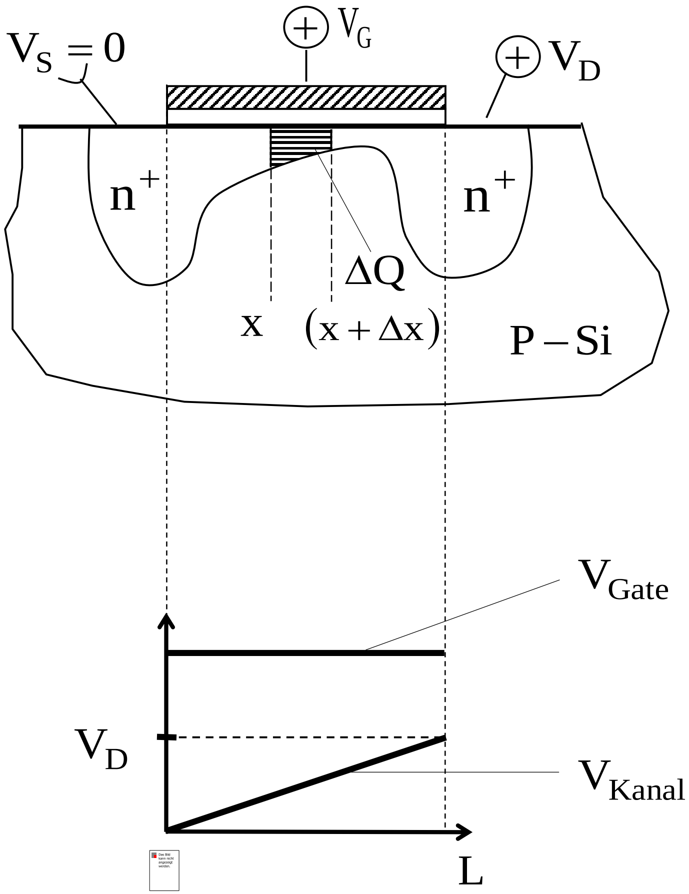
From there on:

$$I_{Dsat} = \frac{\mu \varepsilon_0 \varepsilon_r}{2 d_{ox}} \frac{W}{L} (V_G - V_T)^2$$

Independent of V_D



Derivation



- Gate Capacity: $$C_G = \frac{\varepsilon_0 \varepsilon_r W \cdot L}{d_{ox}}$$
- Capacity within: Δx $$\Delta C = C_G \frac{\Delta x}{L}$$
- Charge between x; $(x + \Delta x)$: $$\Delta Q = \Delta C\left(V_G - V(x)\right)$$
- El. Field in x-Direction: $$E = -\frac{dV}{dx}$$
- Velocity of the Electrons in the channel $$v = -\mu \cdot E = \mu \frac{dV}{dx}$$
  μ: Electron mobility
- Charge carrier density per unit length $$\rho_x = \frac{\Delta Q}{\Delta x}$$

Derivation (2)

Current: $$I_D = \rho_x \cdot v = \frac{\Delta Q}{\Delta x} \cdot \mu \frac{dV}{dx} = \frac{\Delta C(V_G - V(x))}{\Delta x} \cdot \mu \frac{dV}{dx}$$

$$I_D = \frac{C_G \cdot \Delta x (V_G - V(x))}{L \cdot \Delta x} \cdot \mu \frac{dV}{dx} = \frac{C_G \cdot \mu}{L} (V_G - V(x)) \frac{dV}{dx}$$

$$I_D \cdot \int_0^L dx = \frac{C_G \cdot \mu}{L} \int_0^{V_D} (V_G - V(x)) dV = \frac{C_G \cdot \mu}{L} \cdot \left(\int_0^{V_D} V_G dV - \int_0^{V_D} V(x) dV \right)$$

$$I_D \cdot L = \frac{C_G \cdot \mu}{L} \left(V_G V_D - \tfrac{1}{2} V_D^2 \right) = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W \cdot L}{L} \left(V_G V_D - \tfrac{1}{2} V_D^2 \right)$$

So far threshold voltage V_T not considered! Therefore: $V_G \rightarrow V_G - V_T$

$$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W}{L} \left\{ (V_G - V_T) \cdot V_D - \tfrac{1}{2} V_D^2 \right\}$$

Drivation (3)

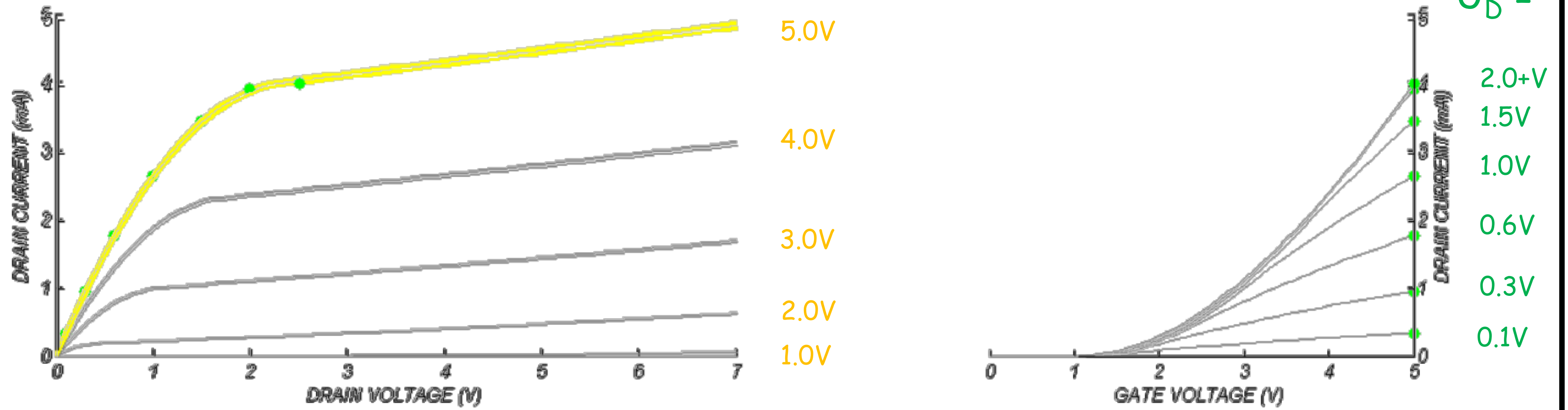
Pinch off at $V_D = V_G - V_T$

It follows

$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{d_{ox}}\frac{W}{L}\left\{(V_G - V_T)(V_G - V_T) - \tfrac{1}{2}(V_G - V_T)^2\right\}$$

$$\boxed{I_D = \frac{\mu\varepsilon_0\varepsilon_r}{2d_{ox}}\frac{W}{L}(V_G - V_T)^2}$$

Independent of V_D



Drivation (3)

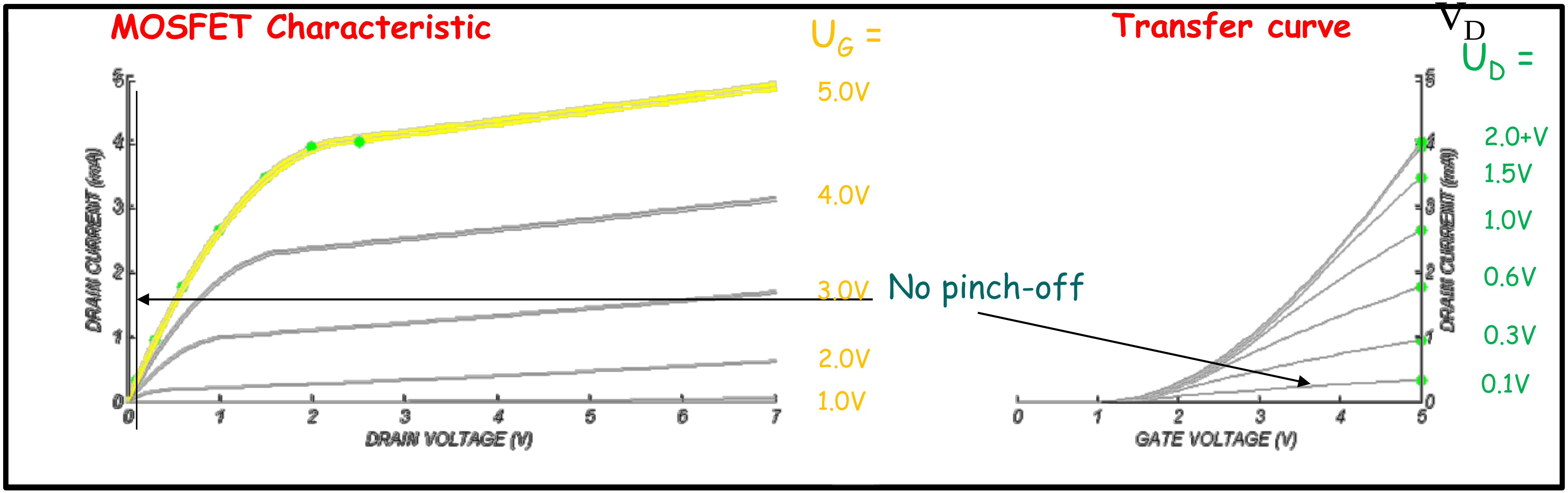
Pinch off at $V_D = V_G - V_T$

It follows

$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{d_{ox}}\frac{W}{L}\left\{(V_G - V_T)(V_G - V_T) - \tfrac{1}{2}(V_G - V_T)^2\right\}$$

$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{2d_{ox}}\frac{W}{L}(V_G - V_T)^2$$

Independent of V_D



Drivation (3)

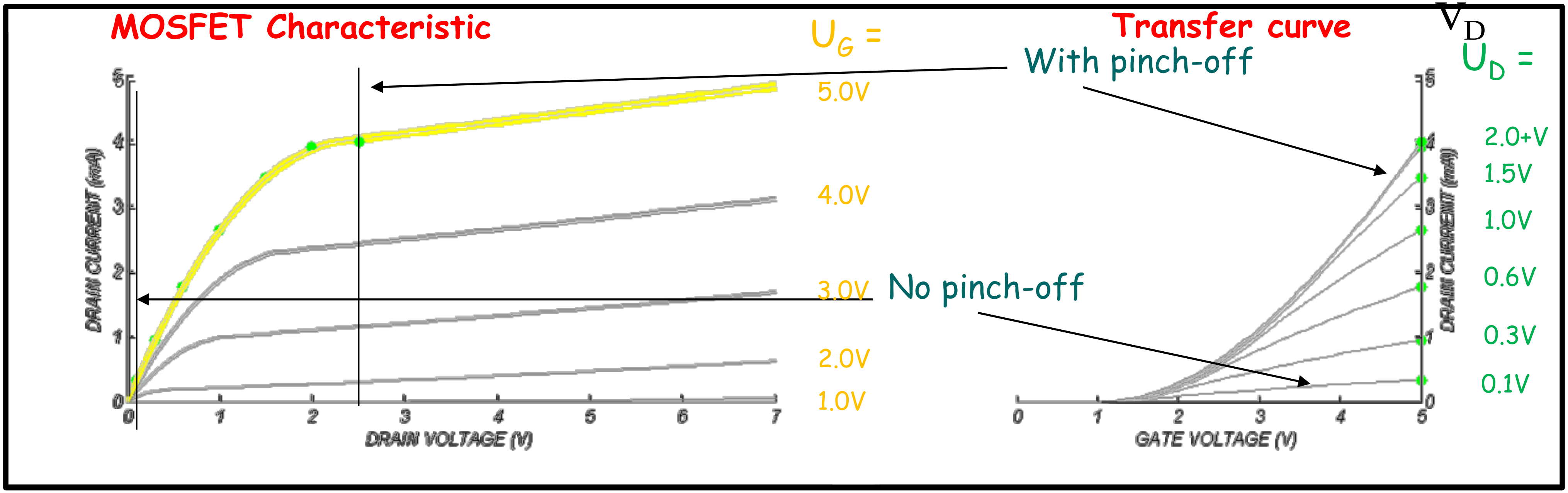
Pinch off at $V_D = V_G - V_T$

It follows

$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{d_{ox}}\frac{W}{L}\left\{(V_G - V_T)(V_G - V_T) - \tfrac{1}{2}(V_G - V_T)^2\right\}$$

$$\boxed{I_D = \frac{\mu\varepsilon_0\varepsilon_r}{2d_{ox}}\frac{W}{L}(V_G - V_T)^2}$$

Independent of V_D



Drivation (3)

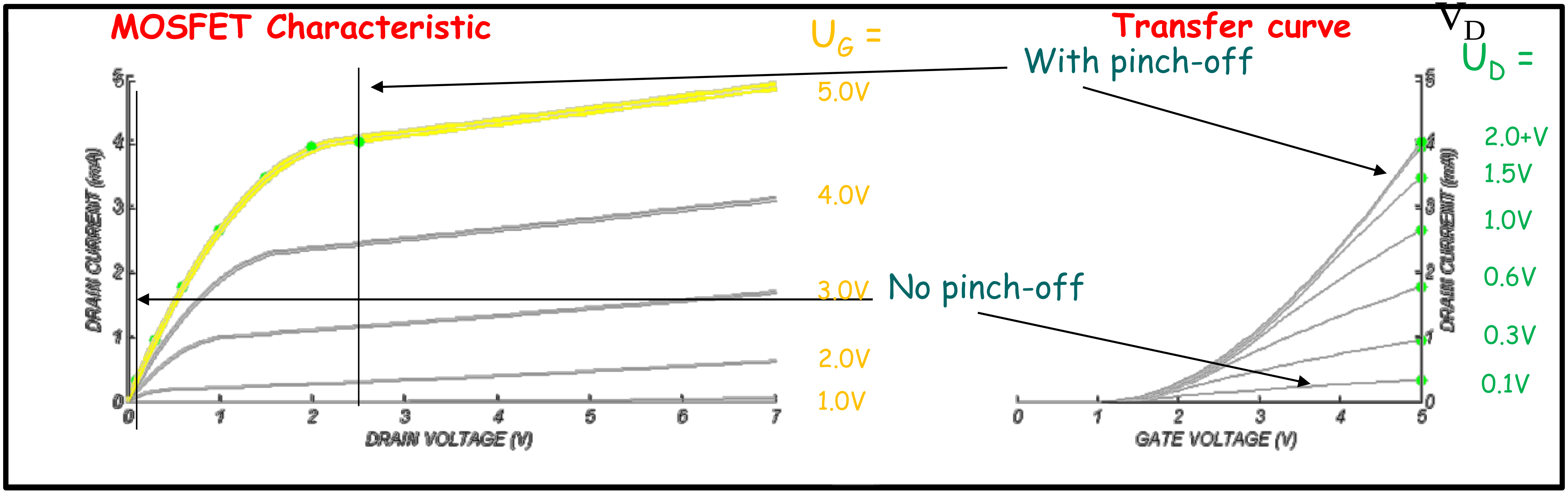
Pinch off at $V_D = V_G - V_T$

It follows

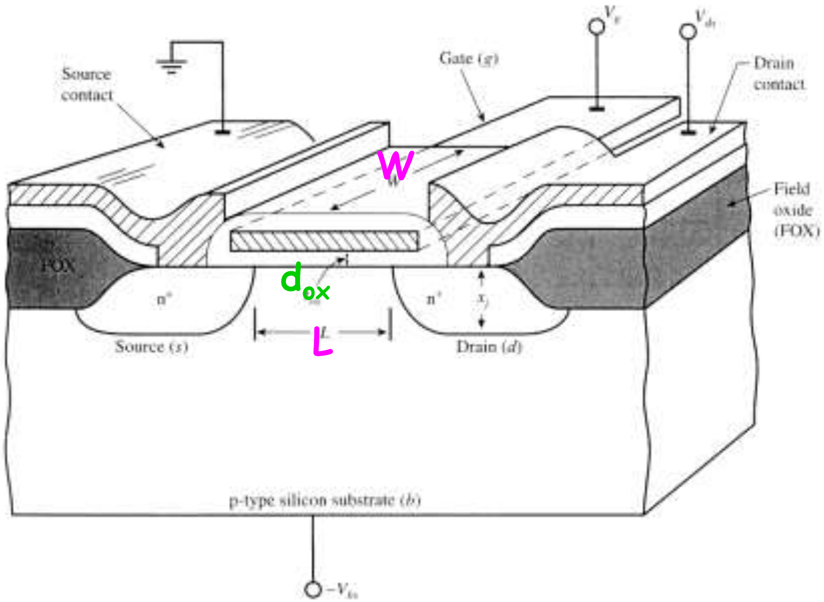
$$I_D = \frac{\mu\varepsilon_0\varepsilon_r}{d_{ox}} \frac{W}{L} \left\{ (V_G - V_T)(V_G - V_T) - \tfrac{1}{2}(V_G - V_T)^2 \right\}$$

$$\boxed{I_D = \frac{\mu\varepsilon_0\varepsilon_r}{2d_{ox}} \frac{W}{L} (V_G - V_T)^2}$$

Independent of V_D



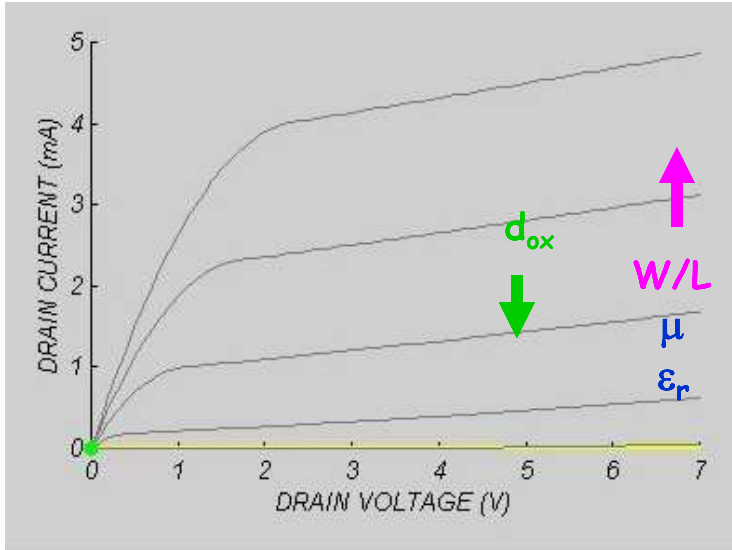
Drain Current vs. Drain Voltage



$I_D = (\mu\varepsilon_0\varepsilon_r / d_{ox}) \cdot W/L \cdot ((V_G - V_T) - \frac{1}{2}V_D)\cdot V_D$

$V_T \sim d_{ox} \cdot N_A$ and Material

Size Effects:



Controlled by:
Design
Process
Material

»Wissen schafft Brücken.«