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Lecture SCT2 – Process Integration

7. Web-based virtual Lecture: June 03 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here  

"SCT_SS21_07.1" 08:31

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Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behaviour
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

Review:
- SC Basics
- MOS Capacitor
- MOS-Cap-CV
- MOS-FET
    - Characteristics
    - Transfer curve
    - Triode behavior
    - Saturation behvr

Today: Al-Gate FET +Inverter

http://www.computerhistory.org/siliconengine/timeline/

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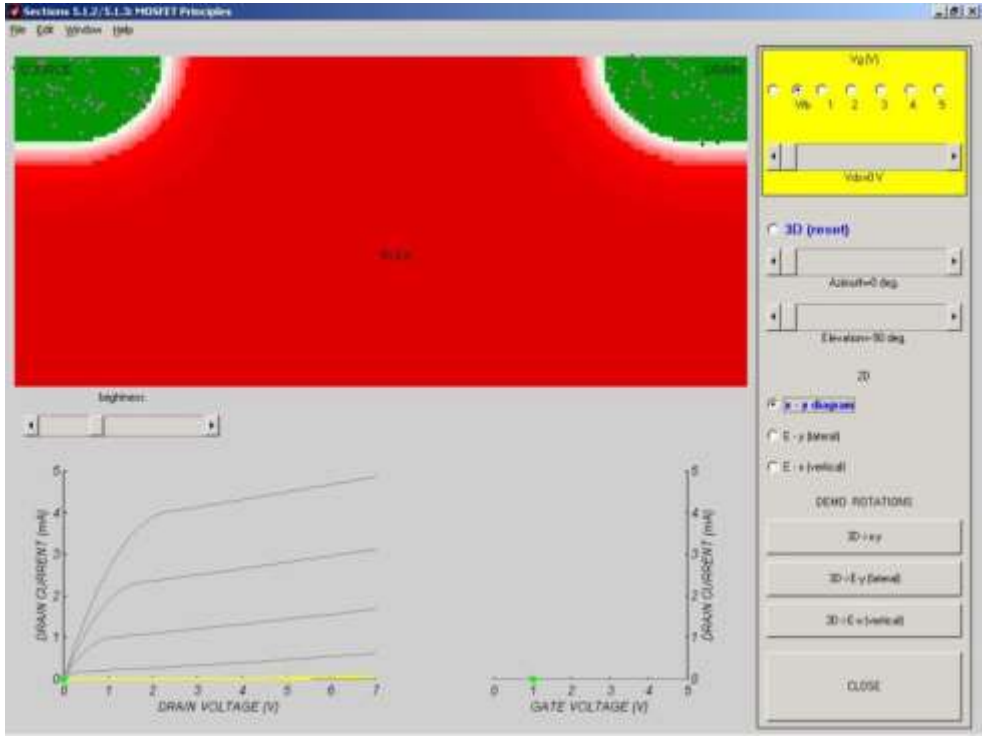
http://www.computerhistory.org/siliconengine/timeline/

Transistor Behavior

The MOS FET

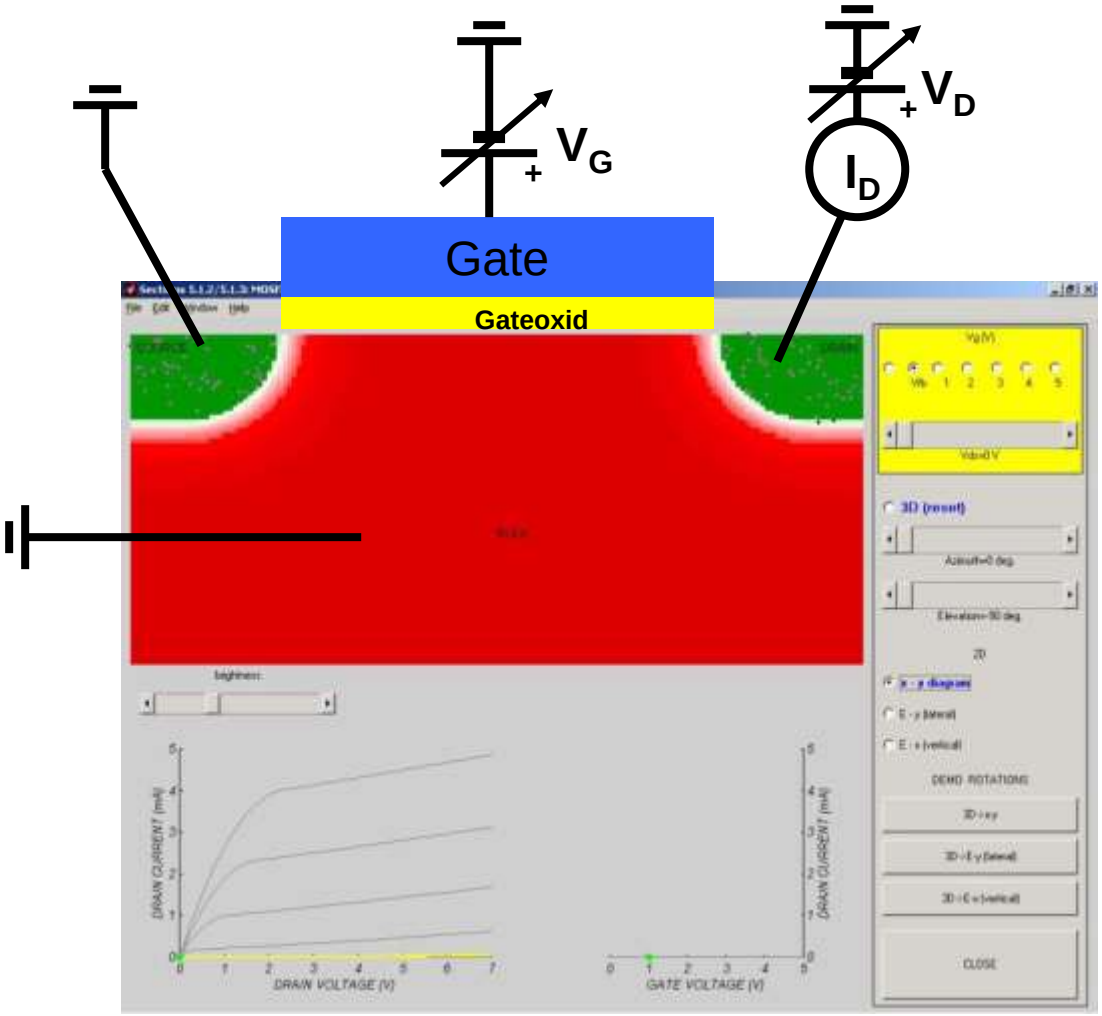


Sima Dimitrijev, Understanding Semiconductor Devices, Oxford University Press 2000

Terms:
- accumulation
- depletion
- inversion
- threshold voltage
- pinch off
- saturation current
- triode mode

Please try the file FETsim.pdf in the OPAL folder!

Transistor Behavior



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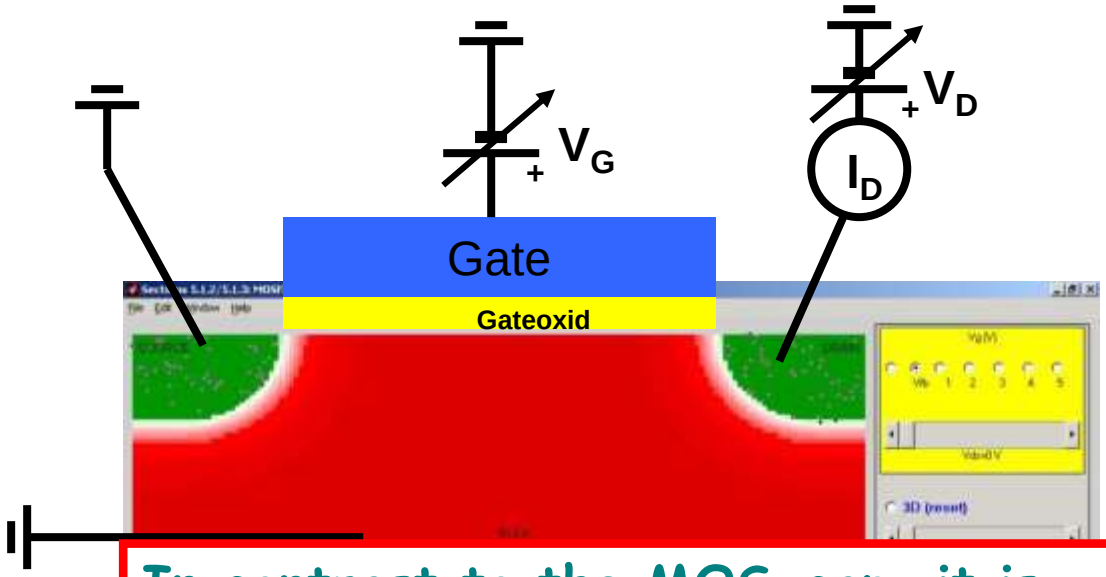

In contrast to the MOS-cap, it is for the MOS-FET not necessary to generate the inversion charge thermally! Here the high S/D doping enables the "flooding" of the channel as soon as the inversion condition is reached.

Sima Dimitrijev, Understanding Semiconductor Devices, Oxford University Press 2000

The MOS FET

Terms:
- accumulation
- depletion
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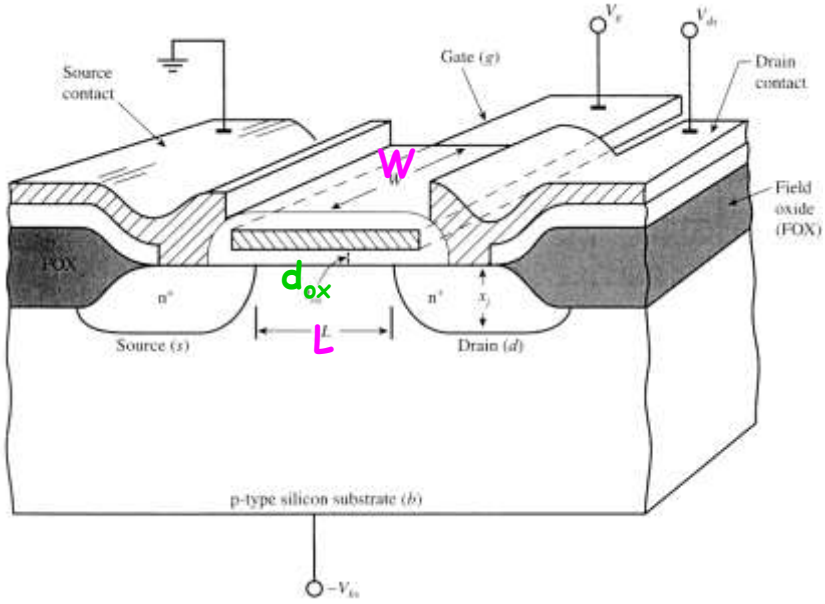
Drain Current vs. Drain Voltage



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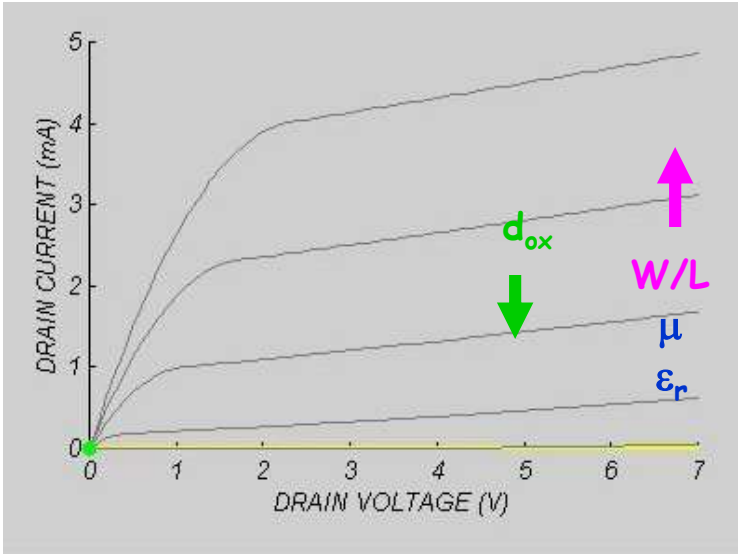


$$I_D = (\mu\varepsilon_0\varepsilon_r/d_{ox})\cdot(W/L)\cdot((V_G - V_T)\cdot V_D - 1/2\cdot V_D^2)$$

$$V_T \sim d_{ox} \cdot N_A$$

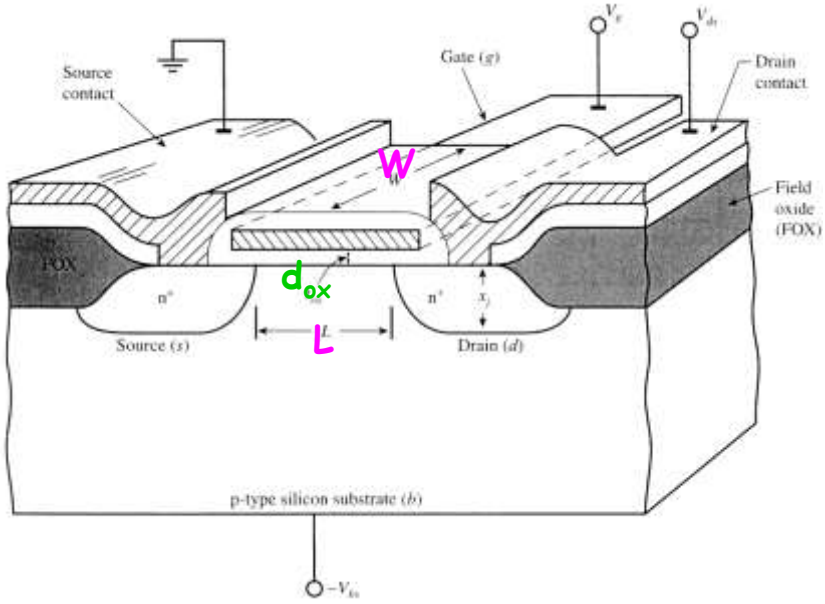
Controlled by:

Design

Process

Material

Drain Current vs. Drain Voltage



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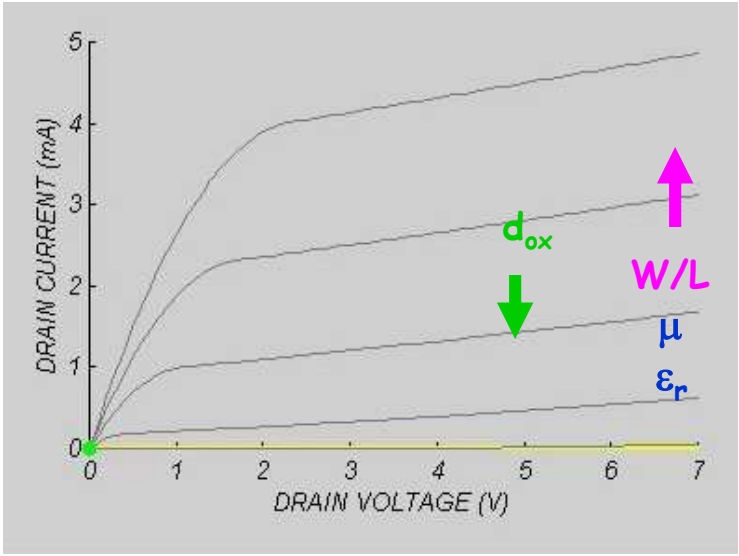

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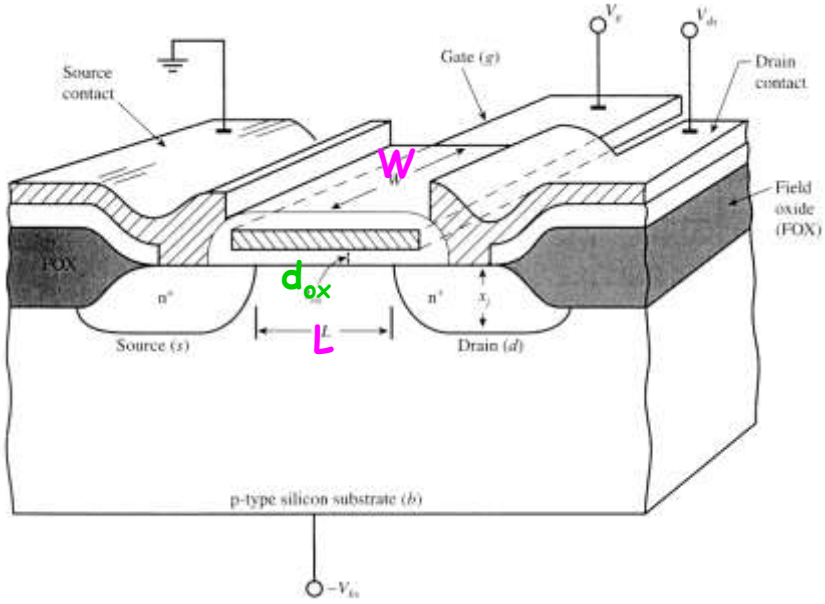
$$V_T \sim d_{ox} \cdot N_A$$

Controlled by:
Design
Process
Material

High I_D requires:
μ, and ε_r as large as possible and
L, and d_{ox} as small as possible!

Drain Current vs. Drain Voltage



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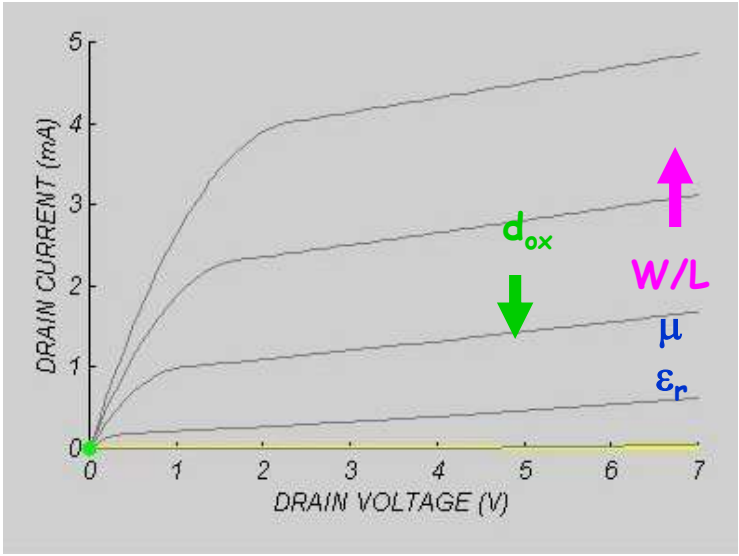

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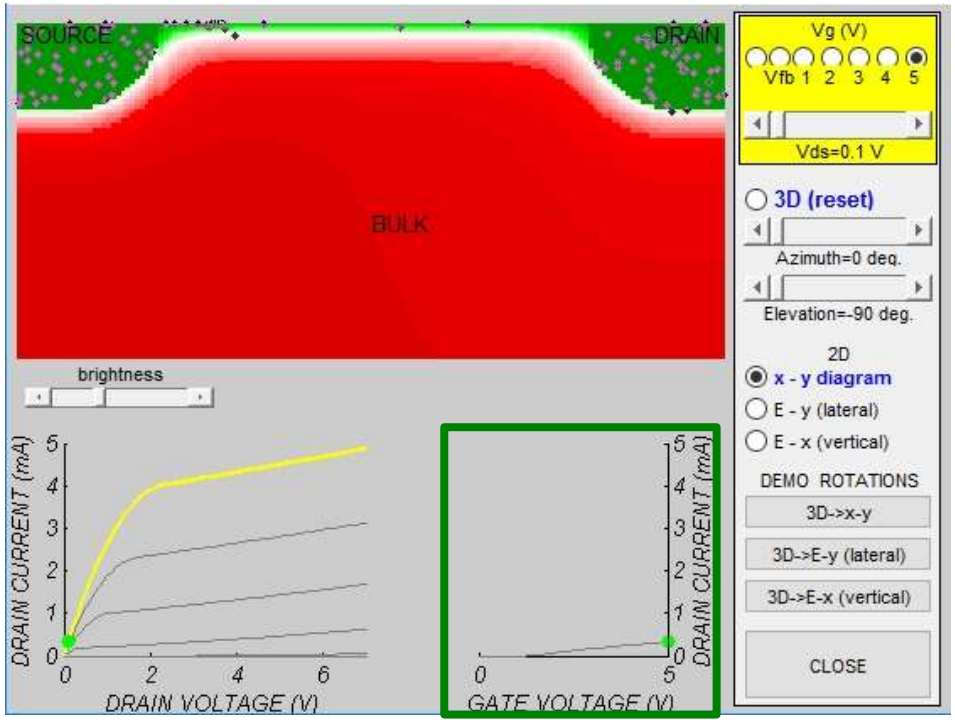
$$V_T \sim d_{ox}\cdot N_A$$

Controlled by:
Design
Process
Material

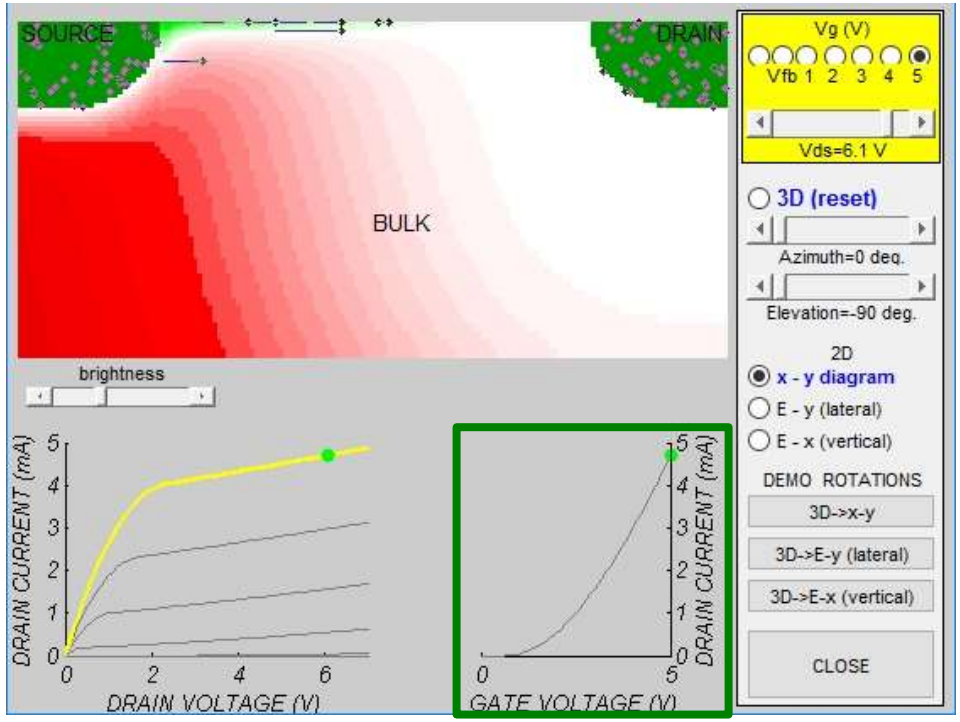
High I_D requires:
μ, and ε_r as large as possible and
L, and d_{ox} as small as possible!

Foundation for shrinking!

Transfer curve $I_D=f(V_G)$



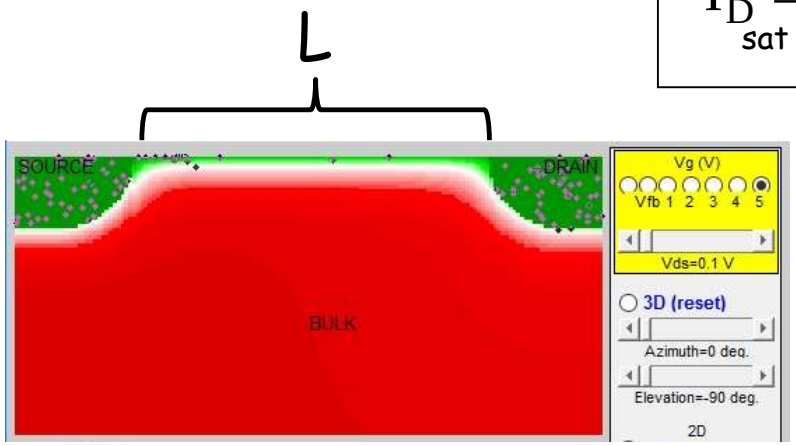
Without pinch-off

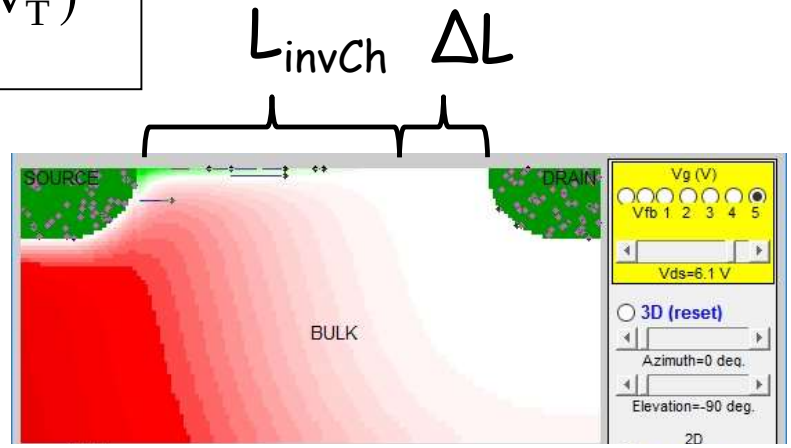


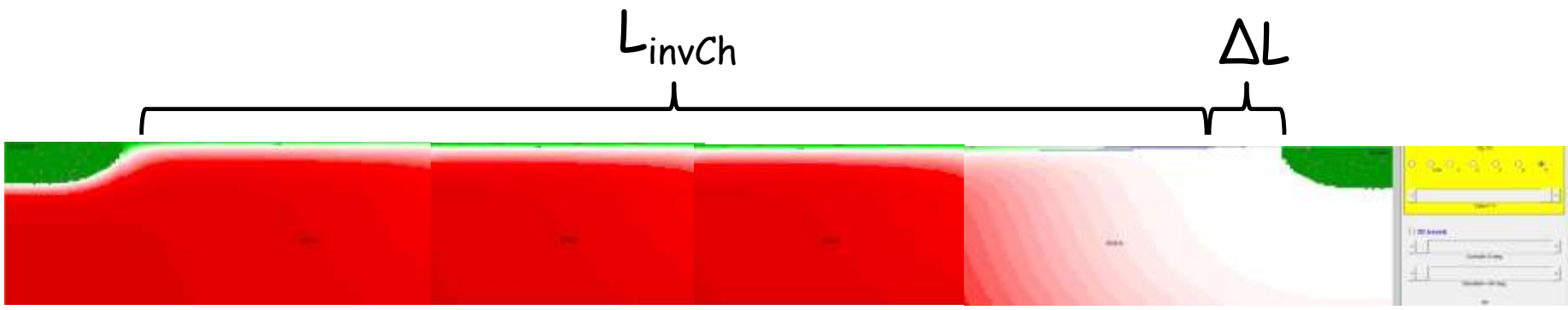
With pinch-off

Inversion channel length:

$$I_{D\,sat} = \frac{\mu \varepsilon_0 \varepsilon_r}{2 d_{ox}} \frac{W}{L} (V_G - V_T)^2$$

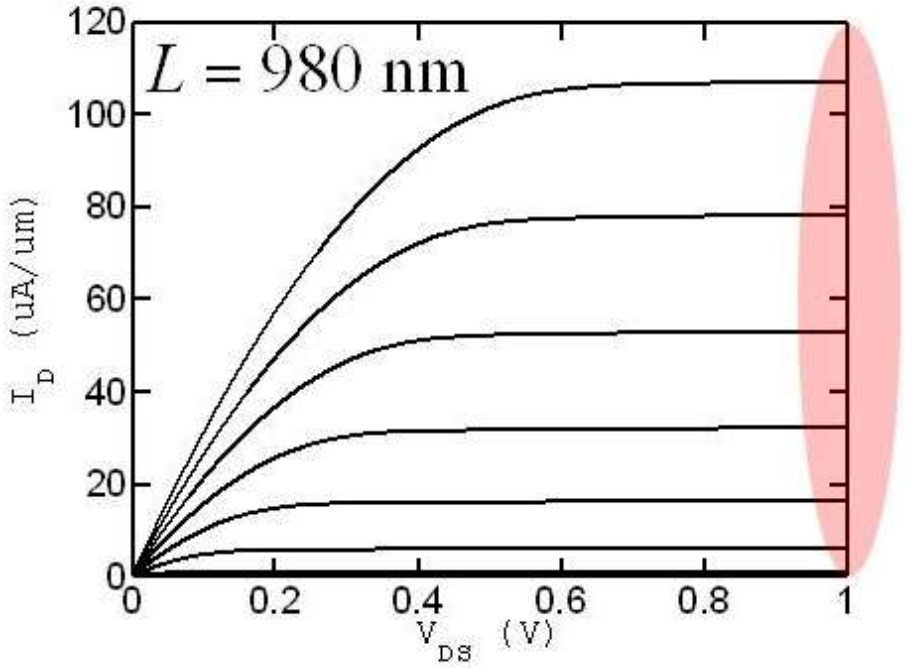


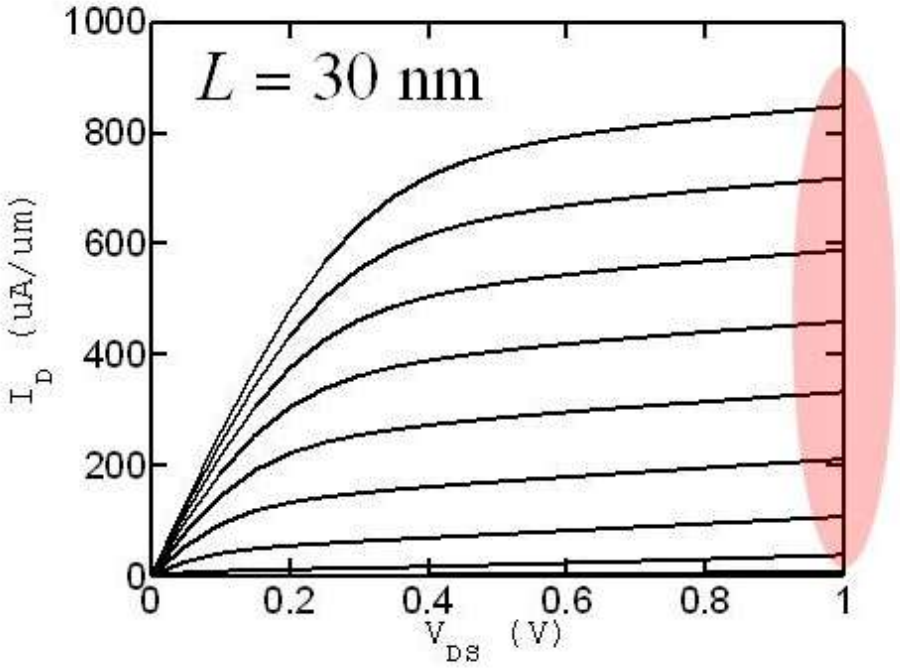




$$I_{D_{sat}} = \frac{\mu \varepsilon_0 \varepsilon_r}{2 d_{ox}} \frac{W}{L} (V_G - V_T)^2$$

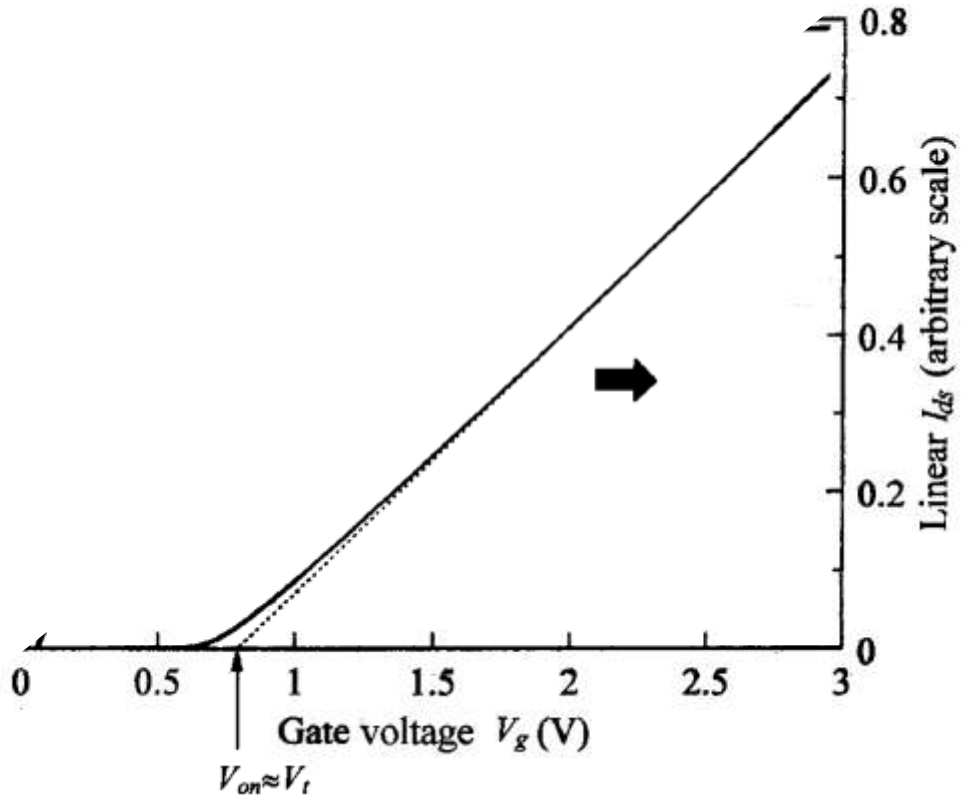
Long Channel vs. Short Channel

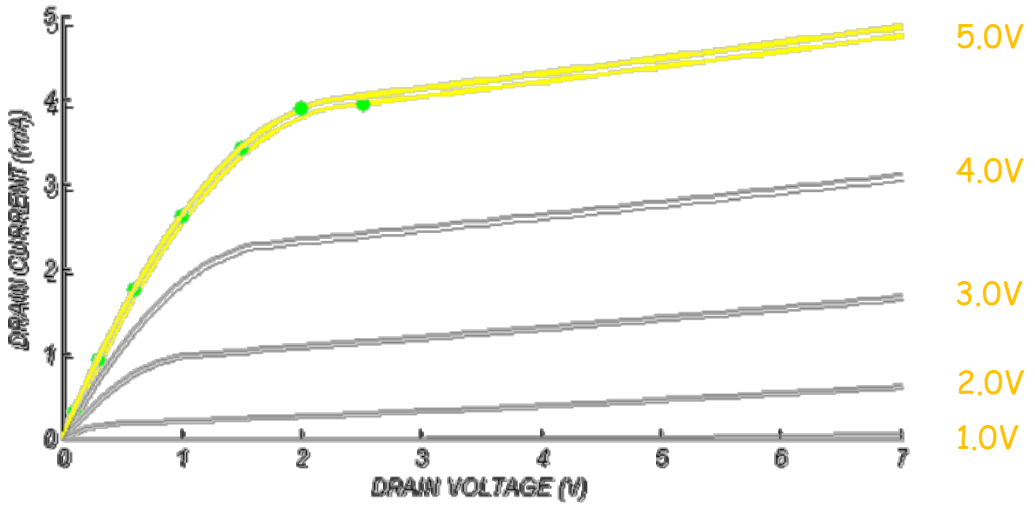




Transfer-Curve : $I_D=f(V_G)$

No current below $V_G=V_T$?





U_G =

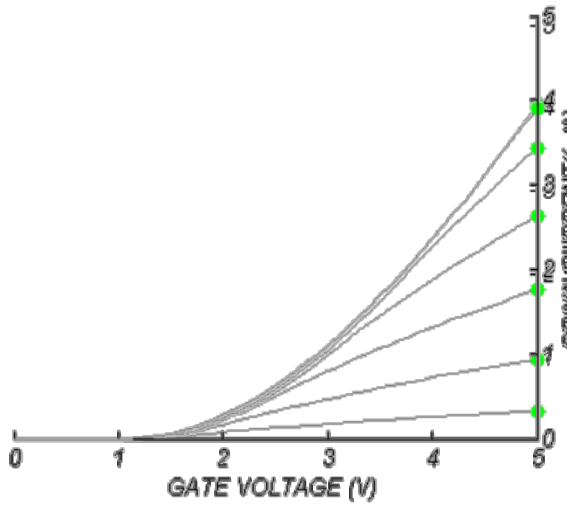
5.0V

4.0V

3.0V

2.0V

1.0V



U_D =

2.0+V

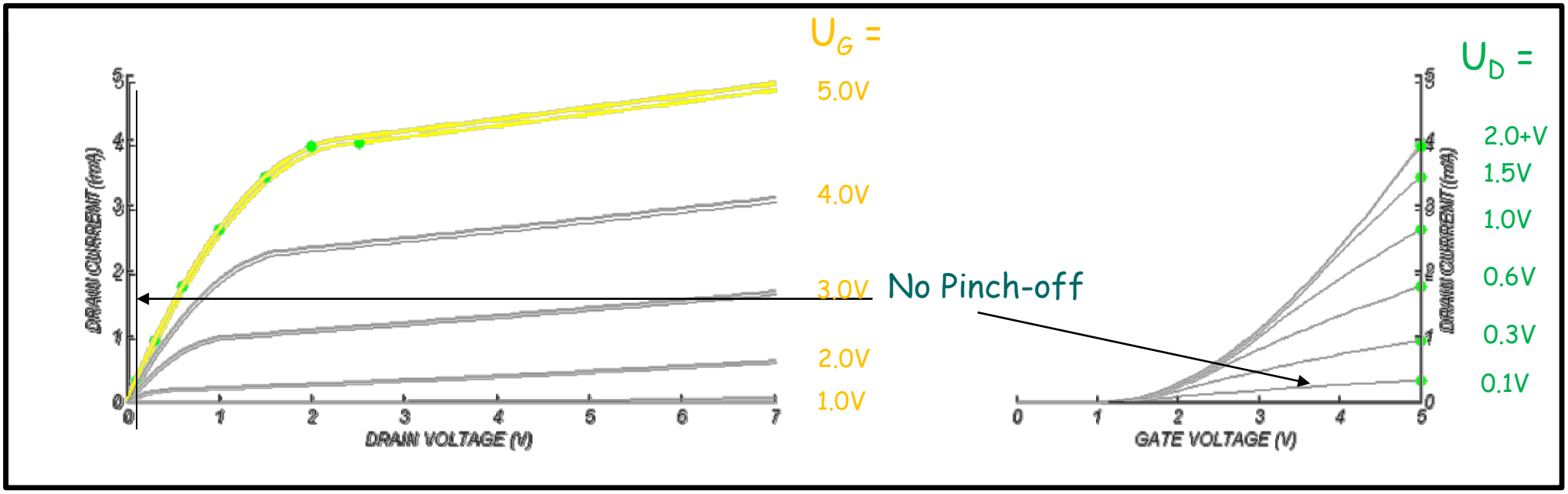
1.5V

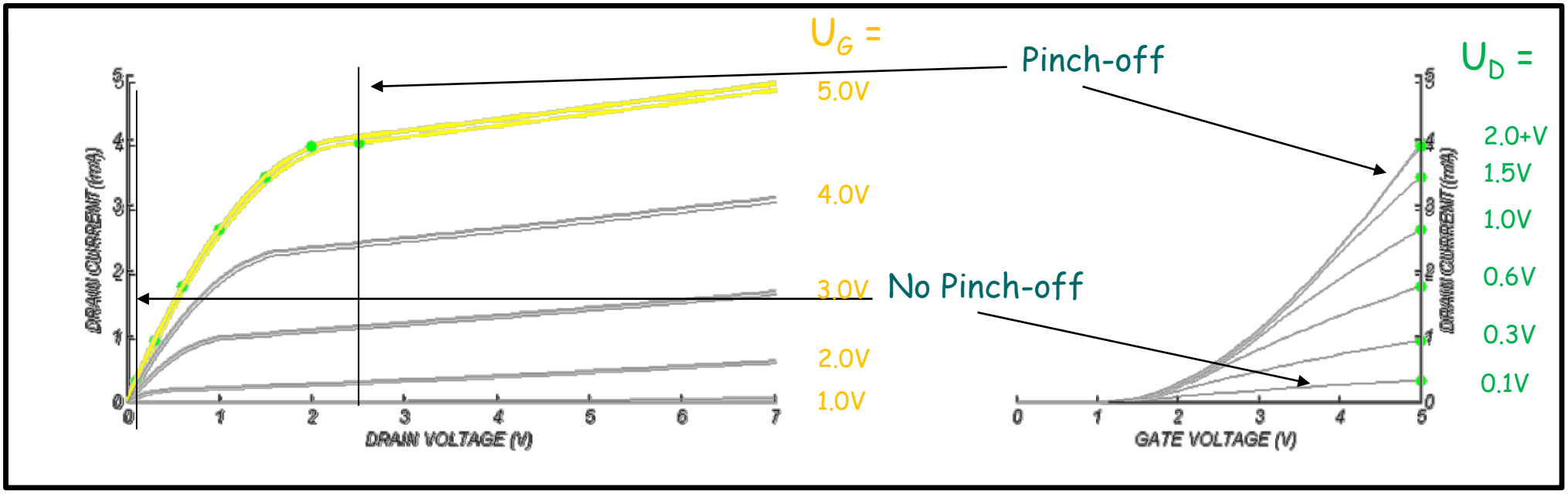
1.0V

0.6V

0.3V

0.1V


U_G =
5.0V
4.0V
3.0V
2.0V
1.0V
DRAIN CURRENT (mA)
DRAIN VOLTAGE (V)
No Pinch-off
U_D =
2.0+V
1.5V
1.0V
0.6V
0.3V
0.1V
DRAIN CURRENT (mA)
GATE VOLTAGE (V)


U_G =
5.0V
4.0V
3.0V
2.0V
1.0V
Pinch-off
No Pinch-off
DRAIN CURRENT (mA)
DRAIN VOLTAGE (V)
U_D =
2.0+V
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Transfer-Curve : $I_D=f(V_G)$

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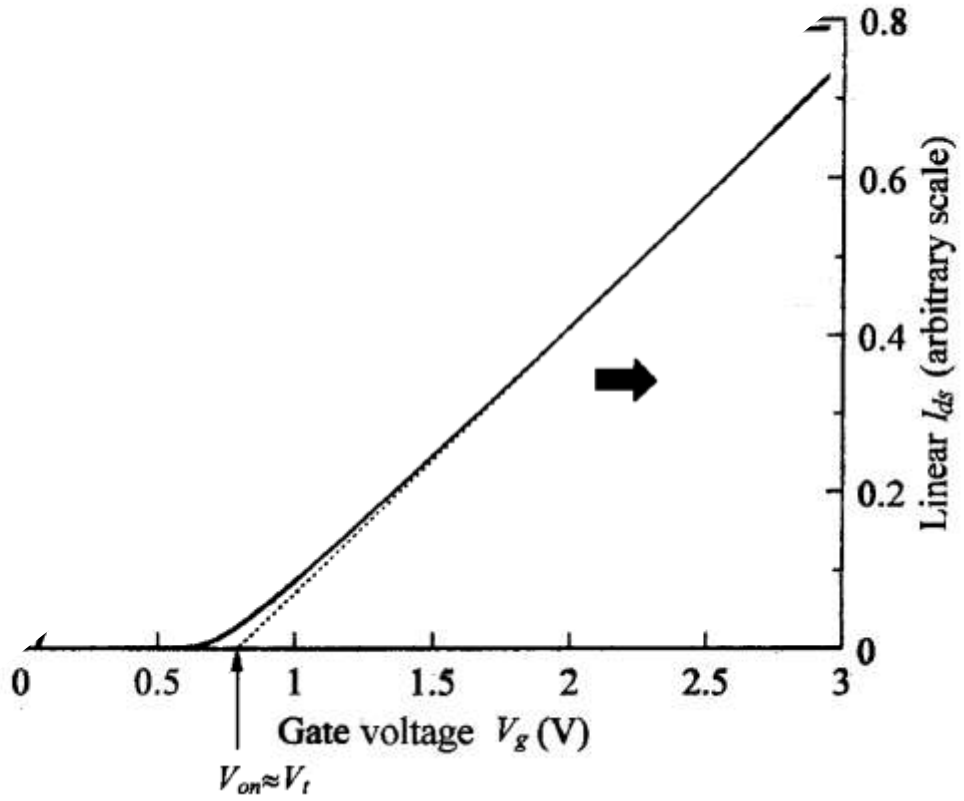
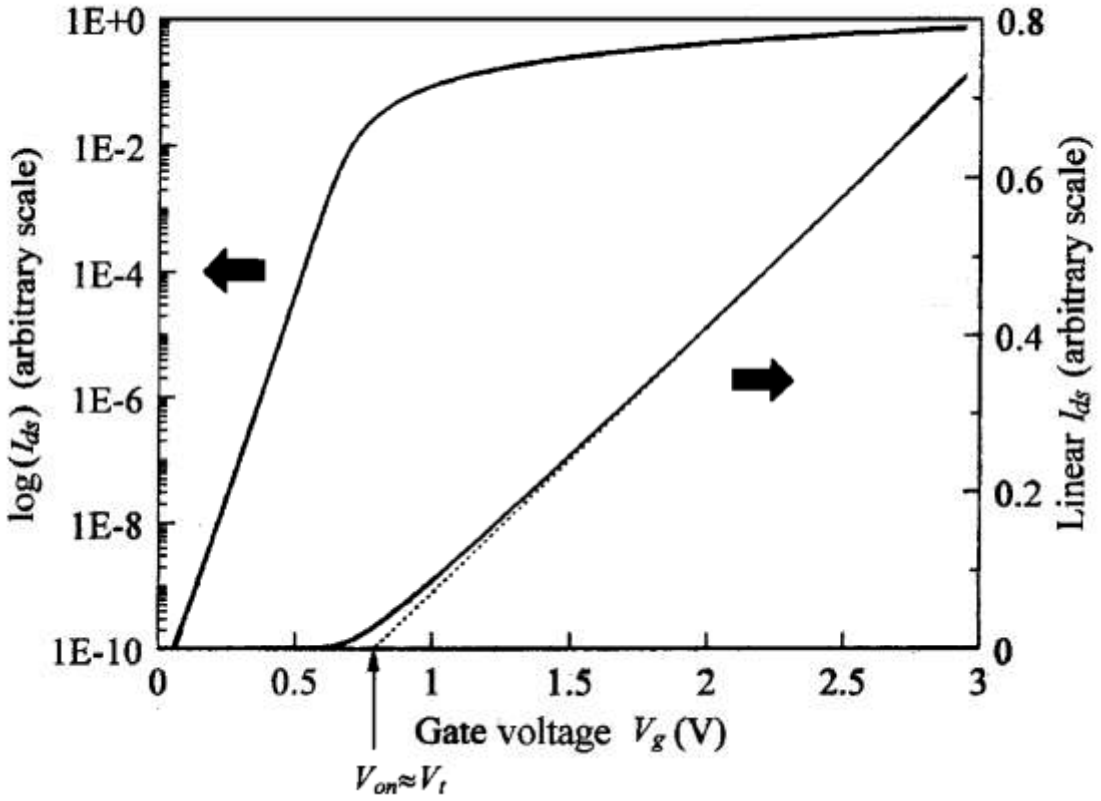


Transfer-Curve : $I_D=f(V_G)$

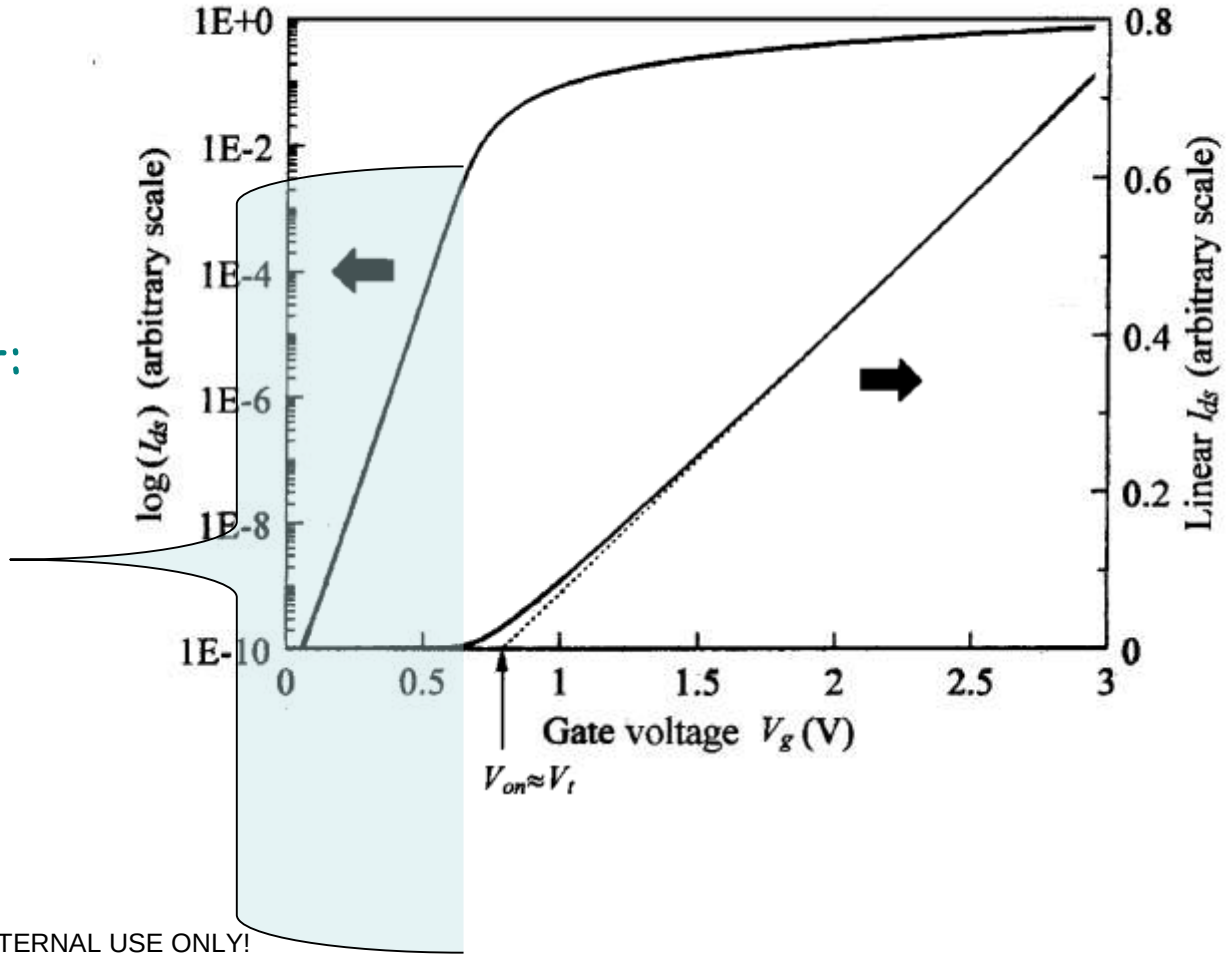
No current below $V_G=V_T$?
It becomes visible in a log-plot!



Transfer-Curve : $I_D=f(V_G)$

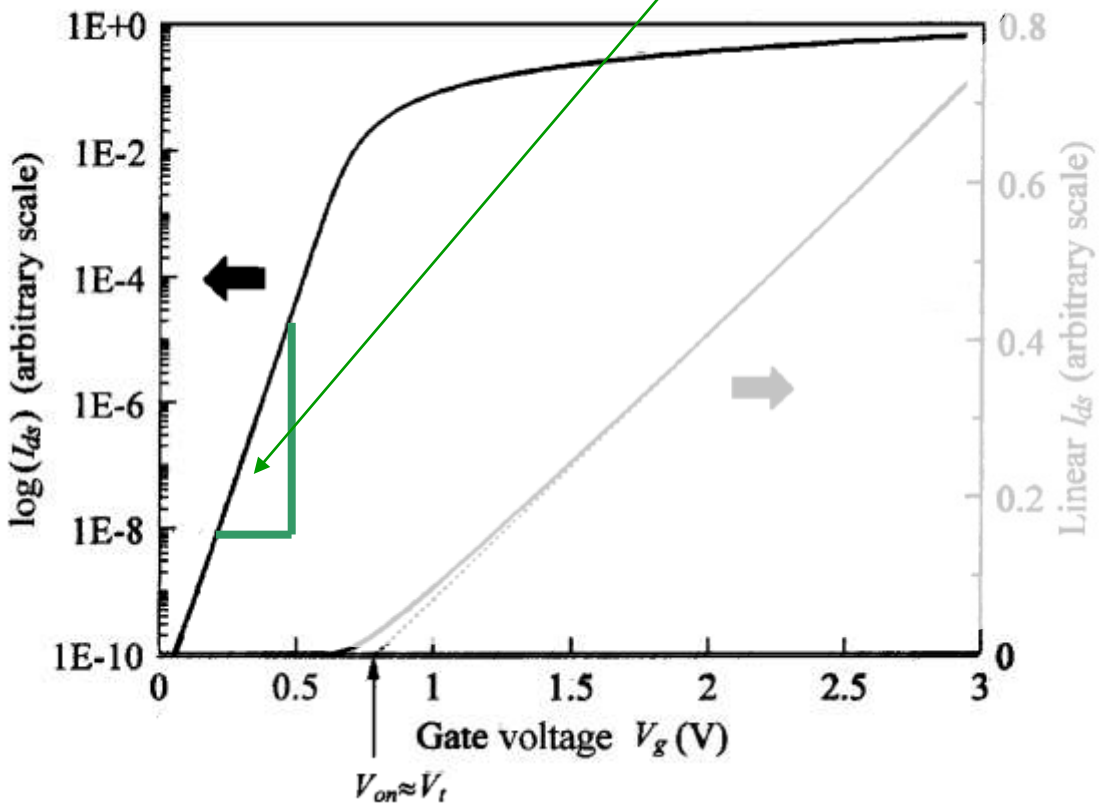
Subthreshold Current:

$I_{Dsubth} \sim e^{q_e(V_g-V_t)/kT}$



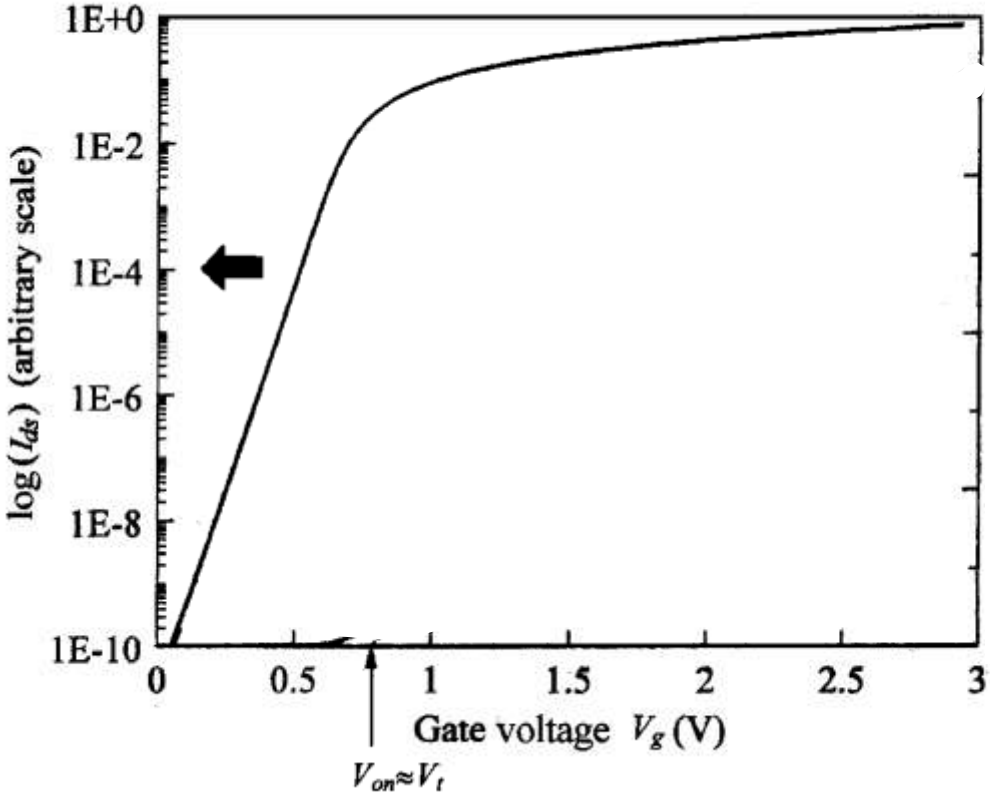
Transfer-Curve : $I_D=f(V_G)$

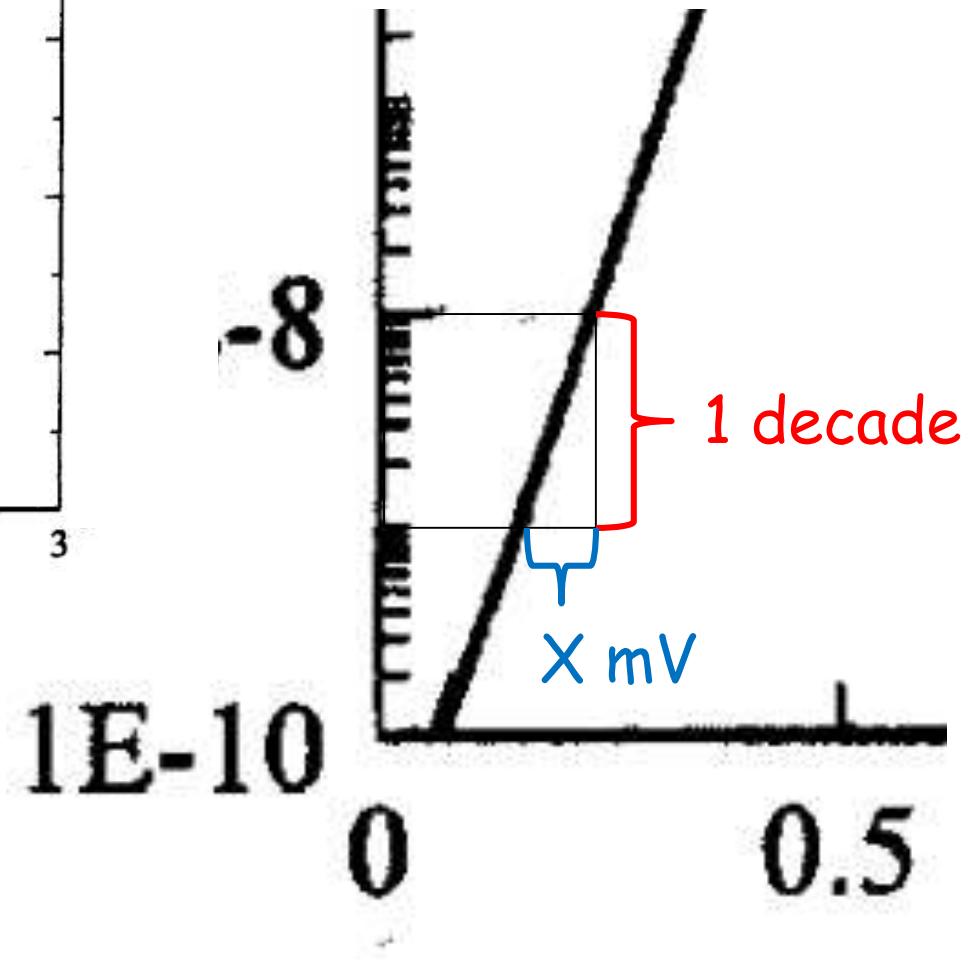
Important Parameter: subthreshold slope oder subthreshold swing



Given as change in V_G to change I_D by one order of magnitude (1 decade).
The ideal (smallest) value (at room temperature) is: 60 mV/decade.
For technology reasons, this value is higher!

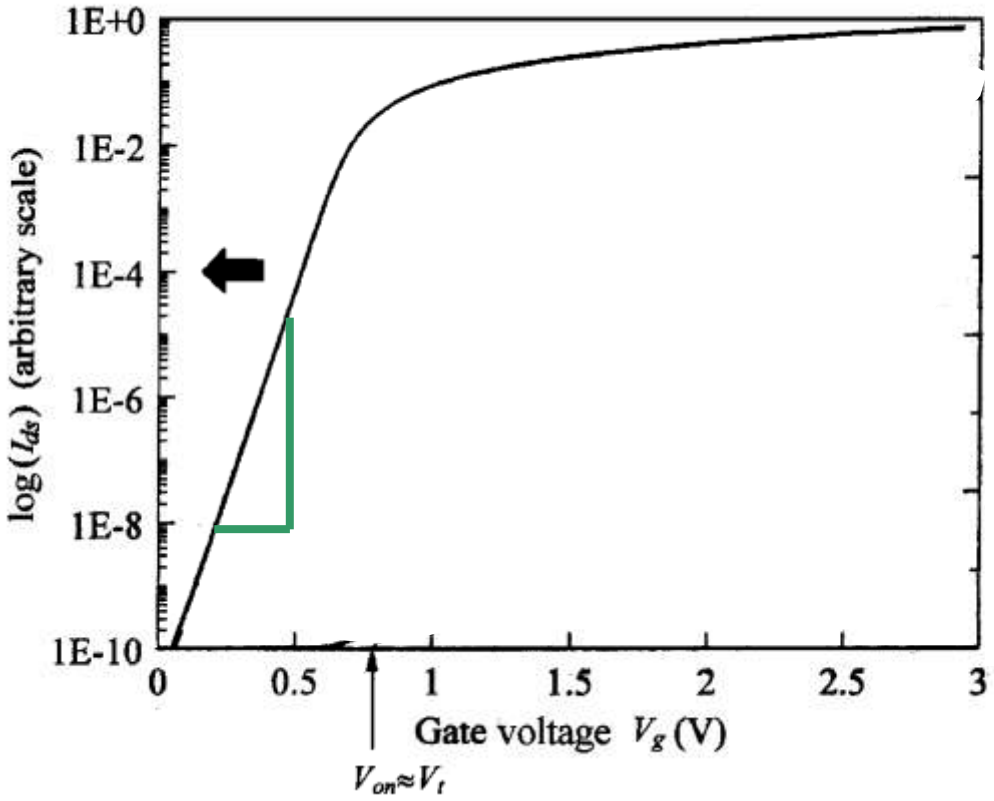
Subthreshold slope given in **mV/decade**





Transfer-curve : $I_D=f(V_G)$

The smaller this value - respectively the steeper the graph in the subthreshold range, the better is the turn off behavior of the transistor or the larger is the I_{on}/I_{off} ratio.



Lowering V_T causes implicitly a lowering of I_{on}/I_{off} !

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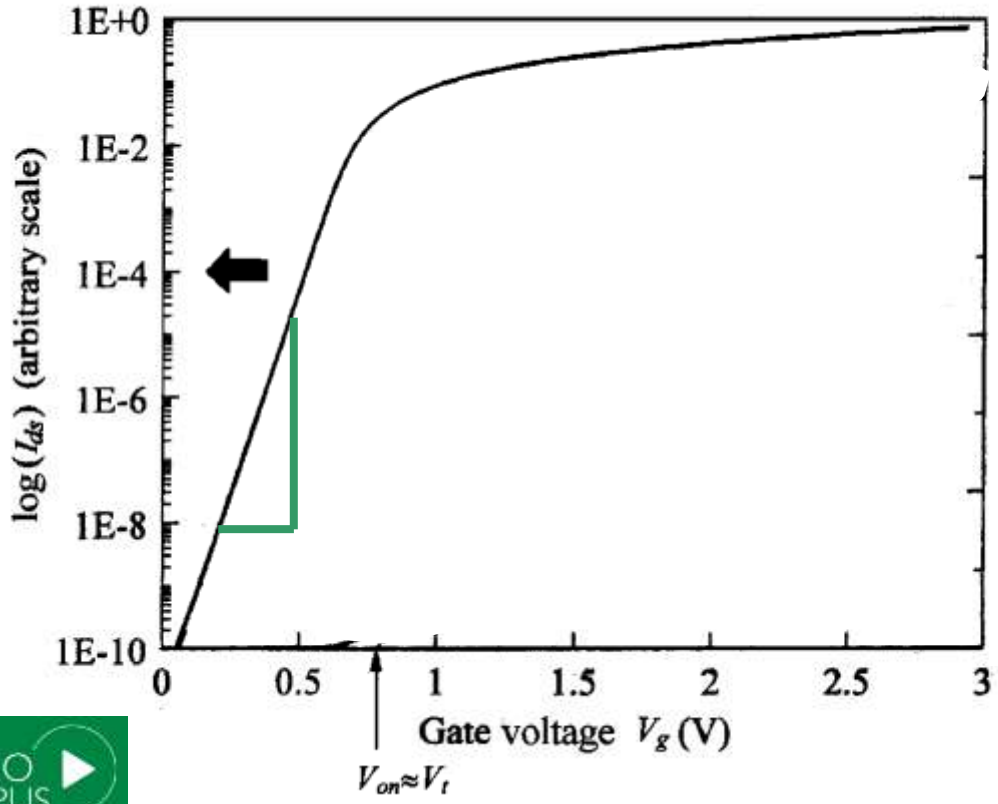

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Lowering V_T causes implicitly a lowering of I_{on}/I_{off} !

2. Circuits in Aluminum-Gate FET

2.1 Making of a simple MOSFET (Very old technology)

Process Sequence for a N-MOS FET in Metal (Aluminum) Gate Technology

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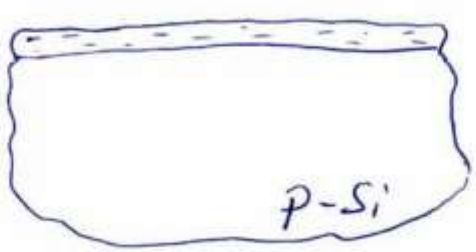
Process Sequence for a N-MOS FET in Metal (Aluminum) Gate Technology



Oxidation

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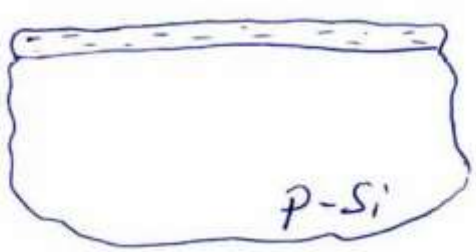
Process Sequence for a N-MOS FET in Metal (Aluminum) Gate Technology



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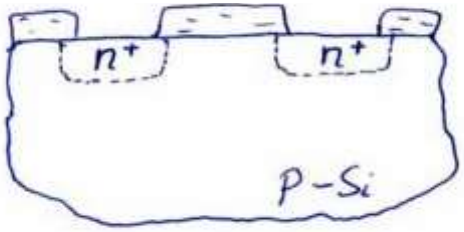

S/D Mask
Ox Etch
S/D Diffusion

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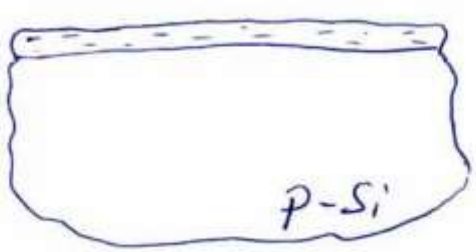

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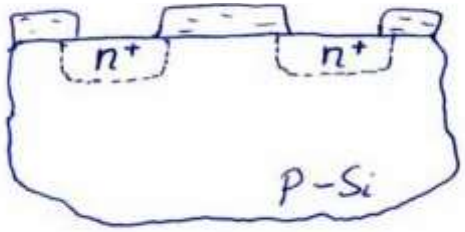
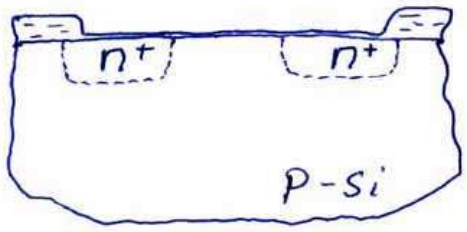


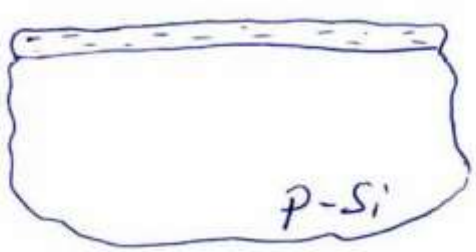
S/D Mask
Ox Etch
S/D Diffusion



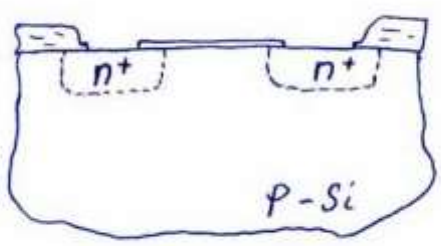
Field-Ox Mask
Ox Etch
Gate Oxidation

2.1 Making of a simple MOSFET (Very old technology)

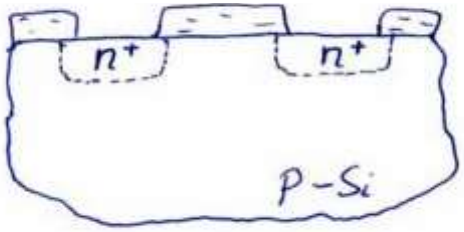
Process Sequence for a N-MOS FET in Metal (Aluminum) Gate Technology



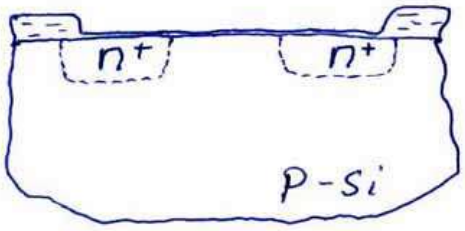
Oxidation



Contact Mask
Ox Etch
Al Depo



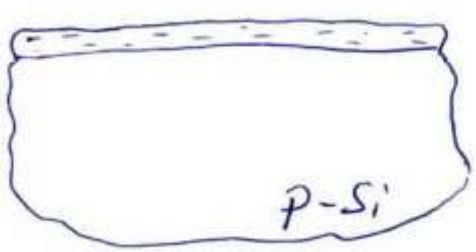
S/D Mask
Ox Etch
S/D Diffusion



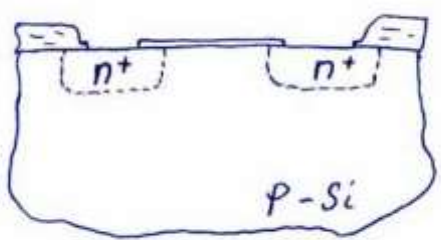
Field-Ox Mask
Ox Etch
Gate Oxidation

2.1 Making of a simple MOSFET (Very old technology)

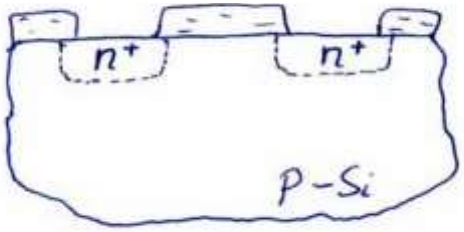
Process Sequence for a N-MOS FET in Metal (Aluminum) Gate Technology



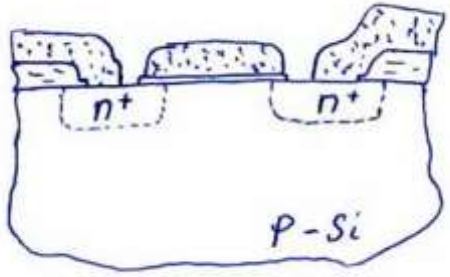
Oxidation



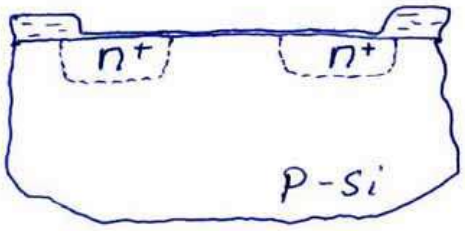
Contact Mask
Ox Etch
Al Depo



S/D Mask
Ox Etch
S/D Diffusion



Metal Mask
Metal Etch



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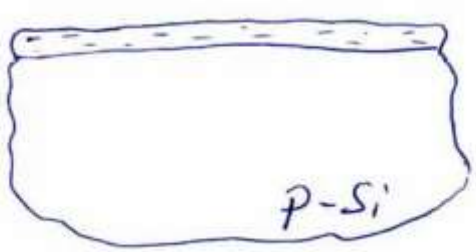
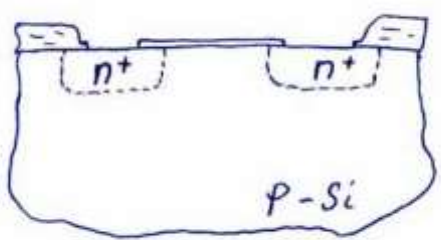


Oxidation



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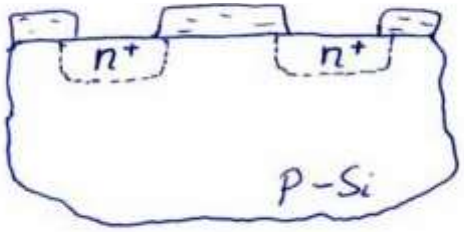

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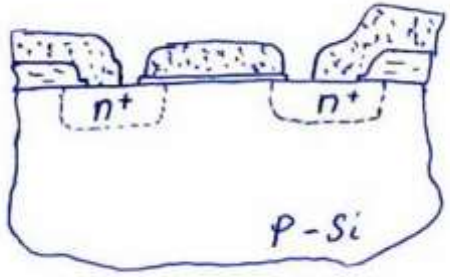
S/D Diffusion



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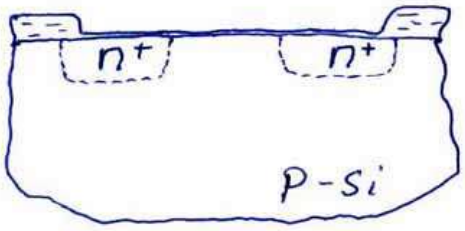

Field-Ox Mask
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Gate Oxidation

4 Mask Process
1 Metal Layer

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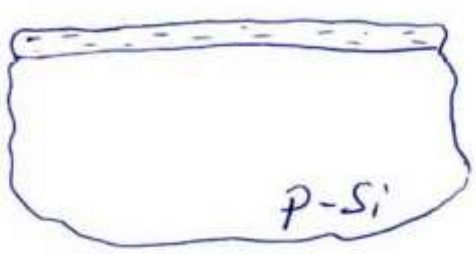
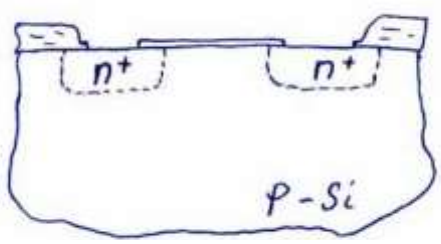


Oxidation



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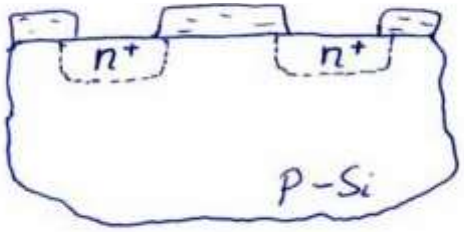

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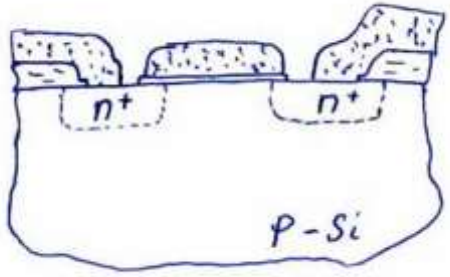

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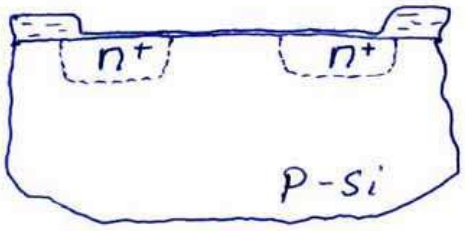

Field-Ox Mask
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Gate Oxidation

4 Mask Process
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Continue

"SCT_SS20_07.04" 50:03

2.2 From an inverter to an SRAM

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Blackboard:

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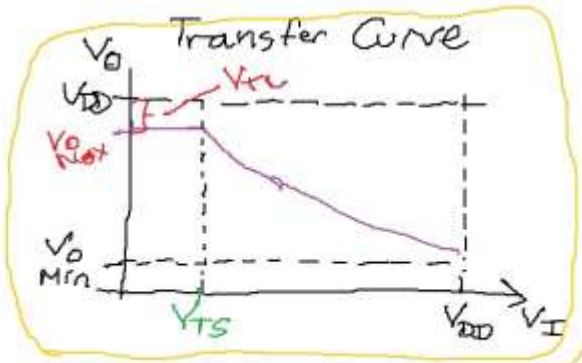
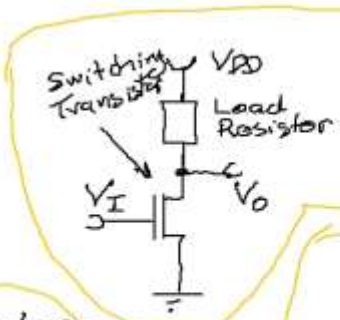
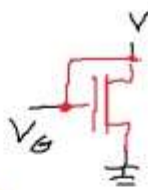
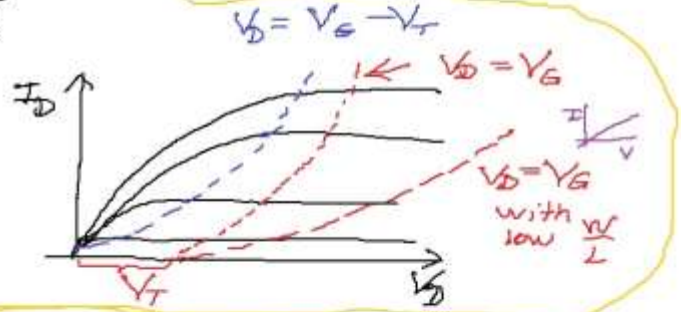




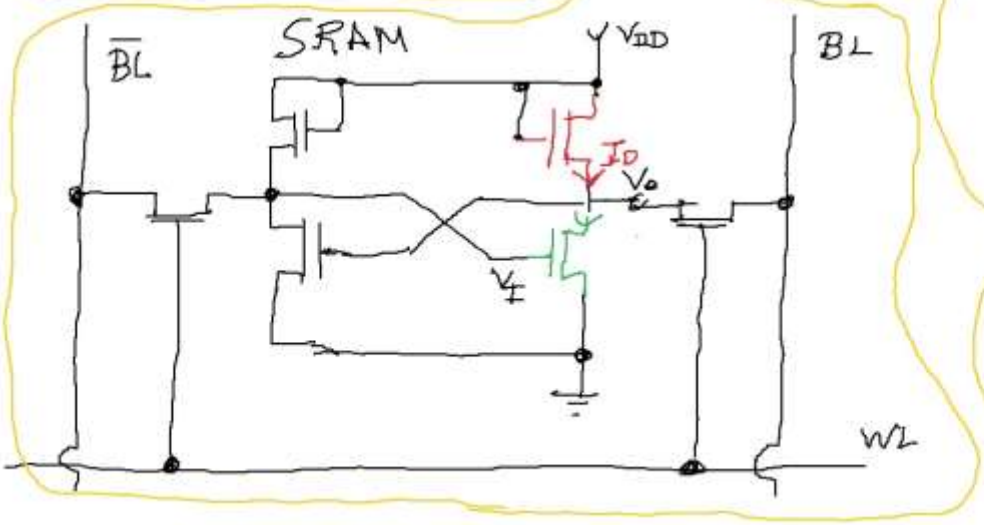
Problem
R_{Load}
difficult to integrate ⇒ more than 4 Masks!

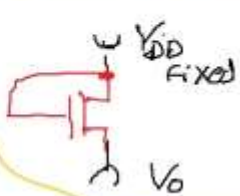
Alternative Loadresistor fabricated by a Transistor!

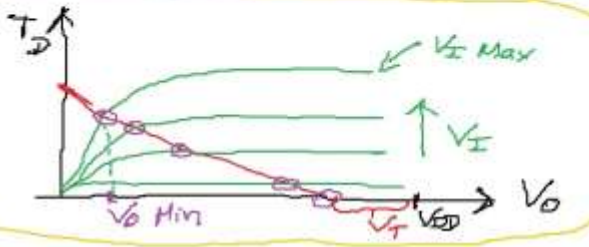




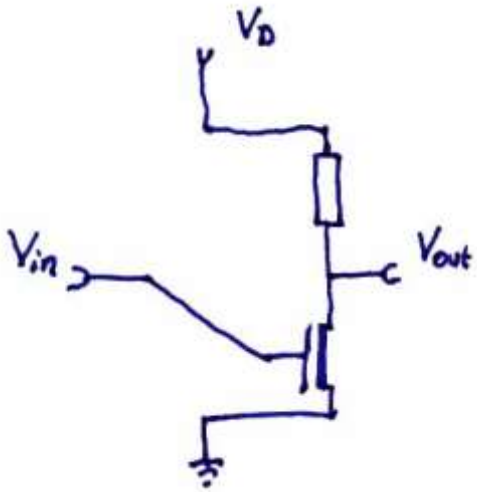
EE-Logic





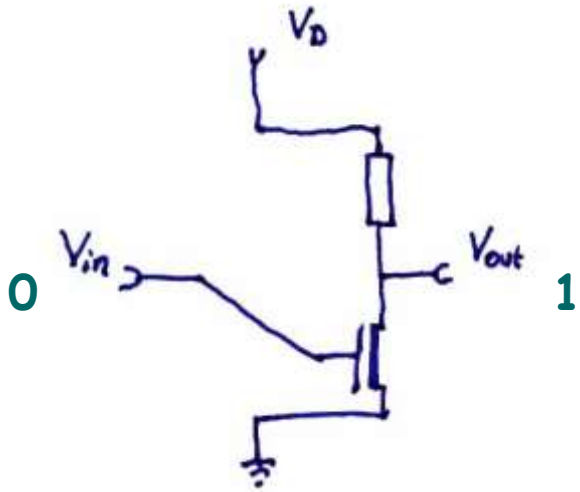


Inverter operation



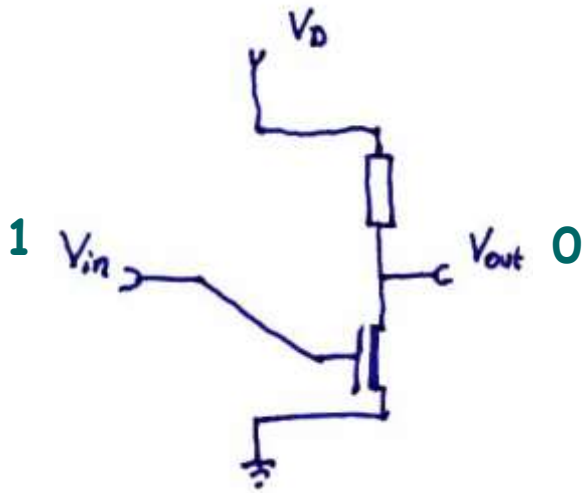
Inverter operation

V_{in} = 0 ➔
S/D of the
Enhancement Transistor
is open ➔
V_{out} = 1



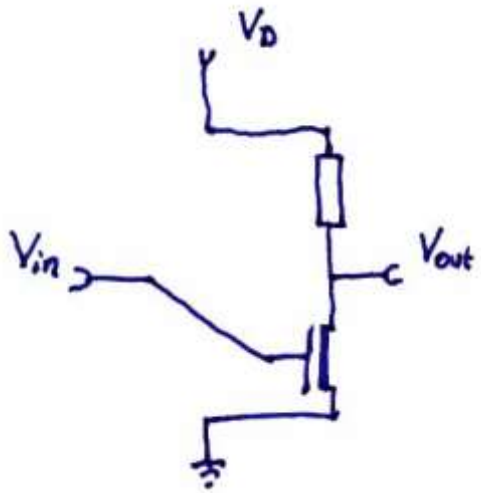
Inverter operation

V_{in} = 1 ➔
S/D of the Enhancement Transistor is switched on. ➔
Output is pulled to ground, V_{out} = 0



Inverter operation

The resistor is called "Load Resistor" and limits the current when the transistor is switched on.



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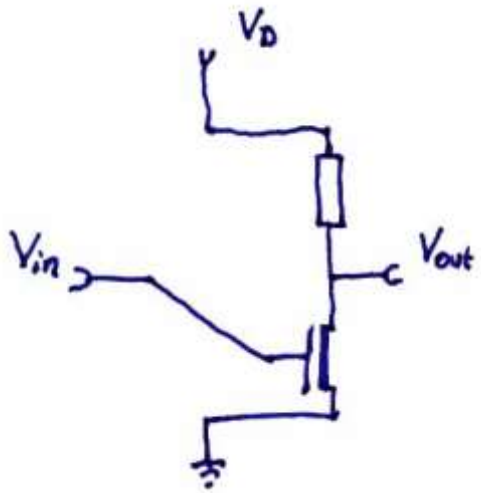

However it's much more complicated with respect to space requirements and/or process complexity to create a resistor instead of another Transistor

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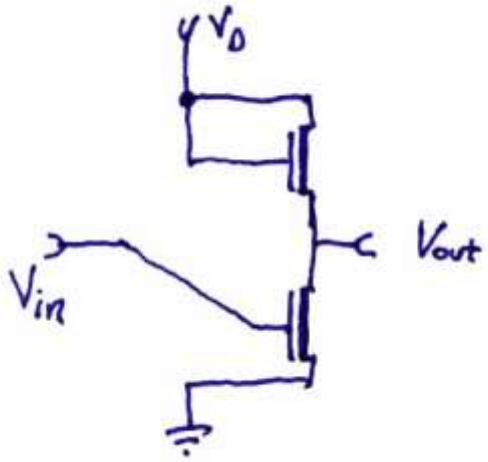

The gate of this "Load Transistor" is connected to the operating voltage

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Load Transistor function

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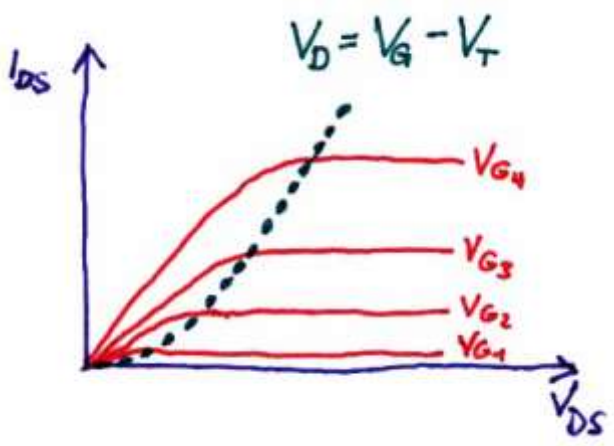

The Pinch Off condition is equivalent to the situation $V_D = V_G - V_T$

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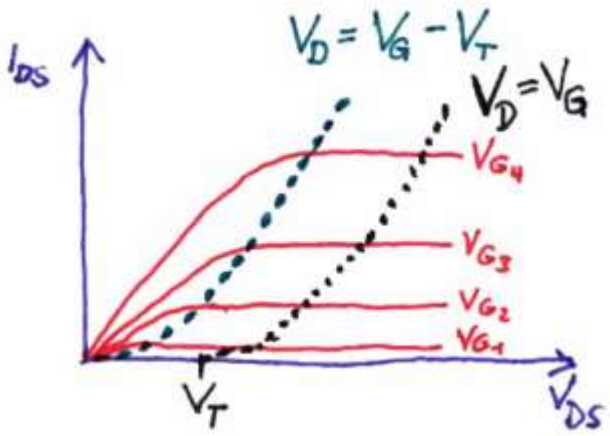
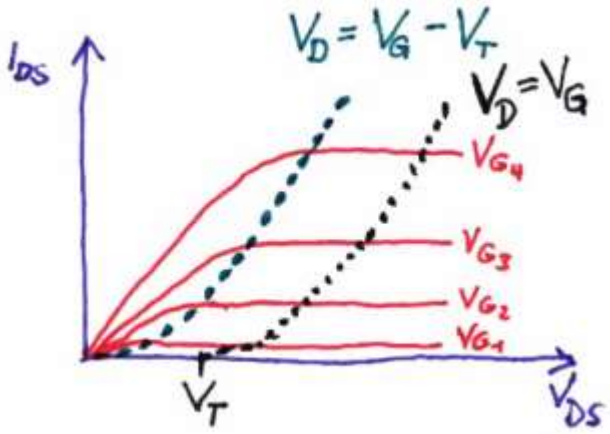
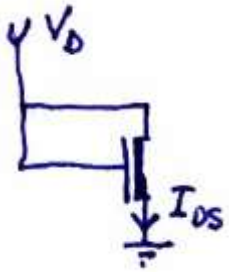


The Pinch Off condition is equivalent to the situation $V_D = V_G - V_T$

If we shift this curve by V_T to the right, we get $I_{DS} = f(V_{DS})$ for the condition $V_D = V_G$ which is the corresponding curve, when the gate is connected to the operating voltage.

Load Transistor function





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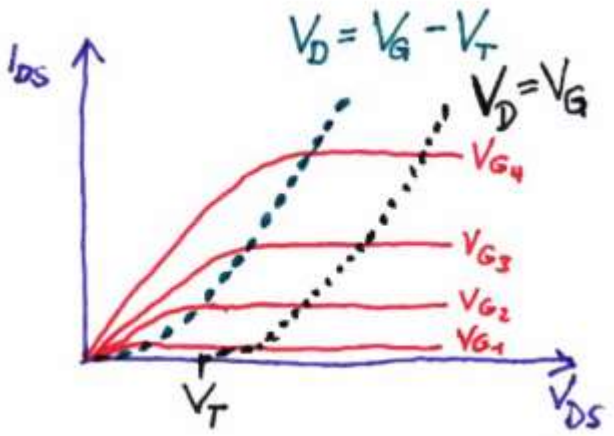

I_{DS}=

$(\mu\varepsilon_0\varepsilon_r/d_{ox}) \cdot$**(W/L)** $((V_G - V_T) - 1/2\ V_D)\cdot V_D$

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Remember: The current is proportional to W/L!

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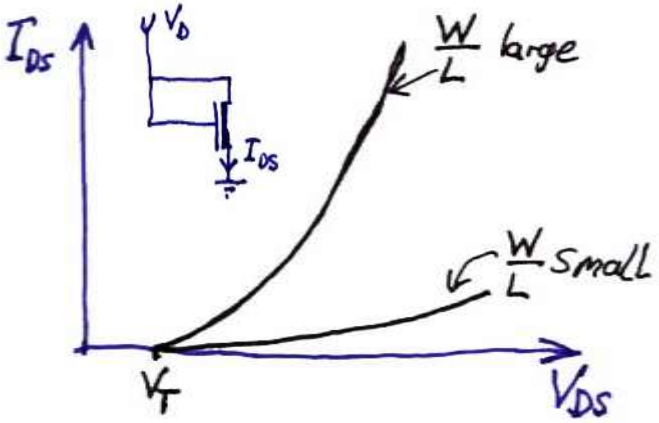

$$I_{DS} = (\mu\varepsilon_0\varepsilon_r/d_{ox}) \cdot \mathbf{(W/L)} ((V_G - V_T) - 1/2\ V_D) \cdot V_D$$

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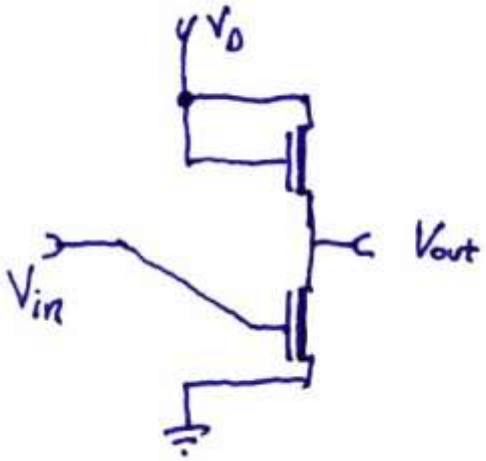
Remember: The current is proportional to W/L!

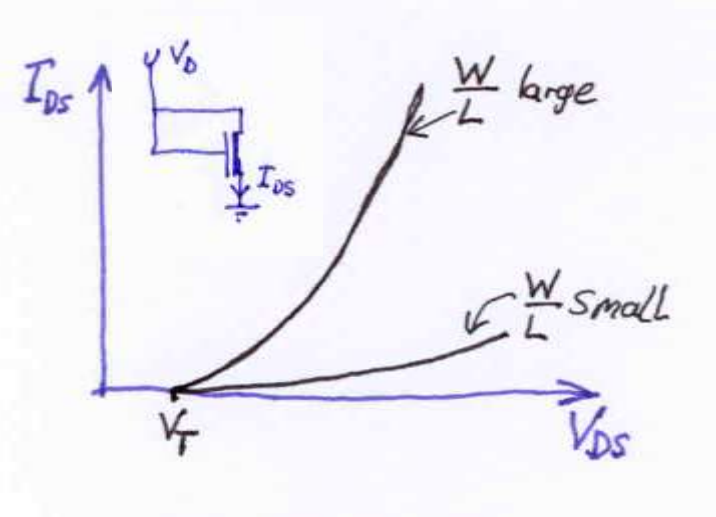
To limit the current W/L should be small !

Performance of the N MOS Inverter



At our Inverter, V_D is kept constant and the "foot-point" of the load transistor V_{out} varies between almost zero and almost V_D.

Performance of the N MOS Inverter



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Therefore the curve for the gated drain

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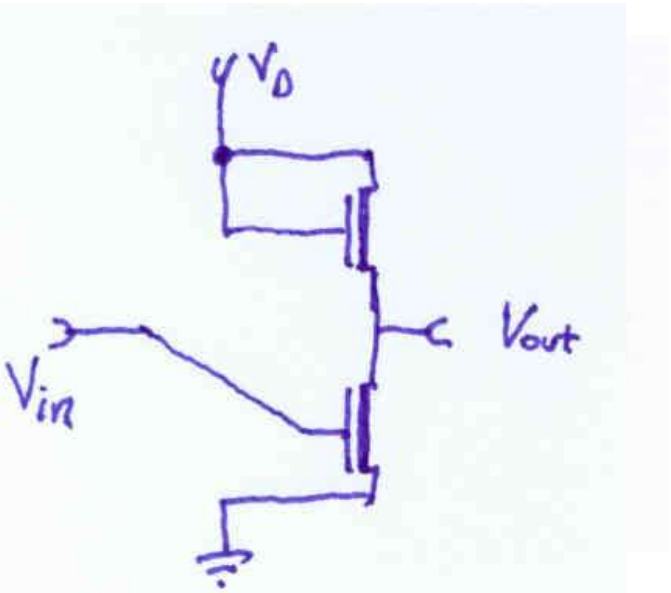

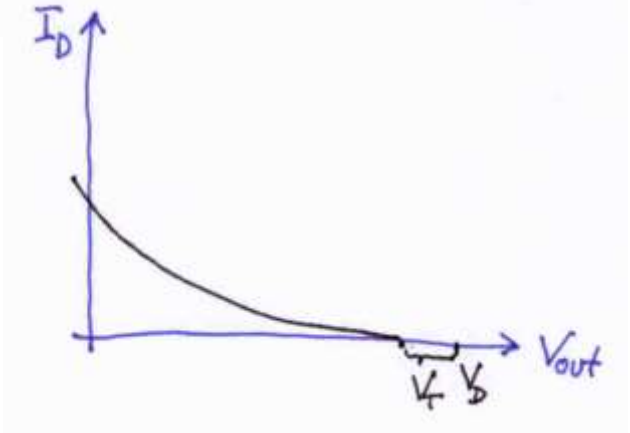

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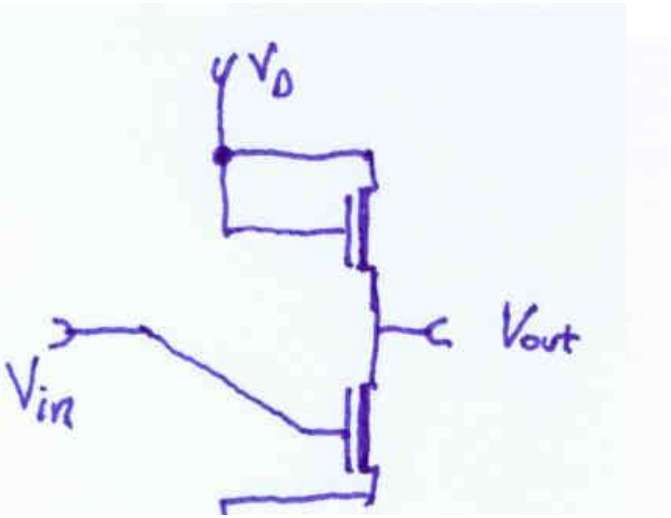

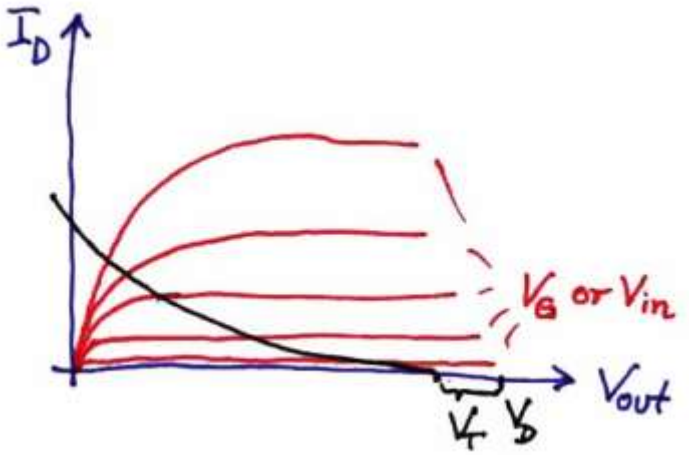

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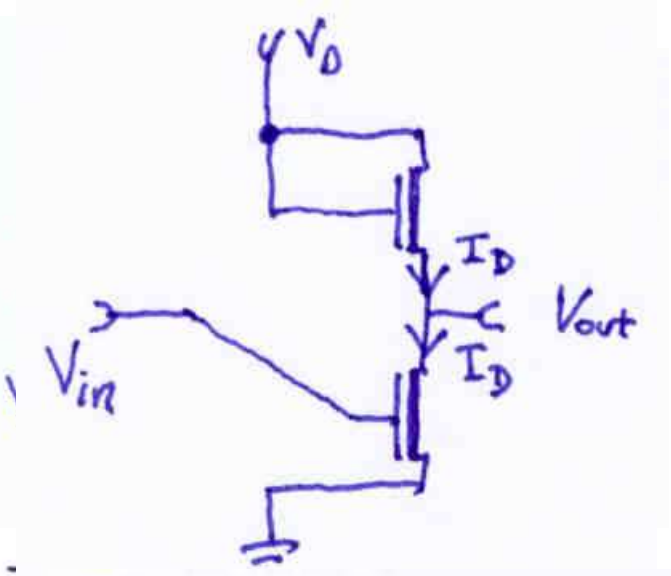
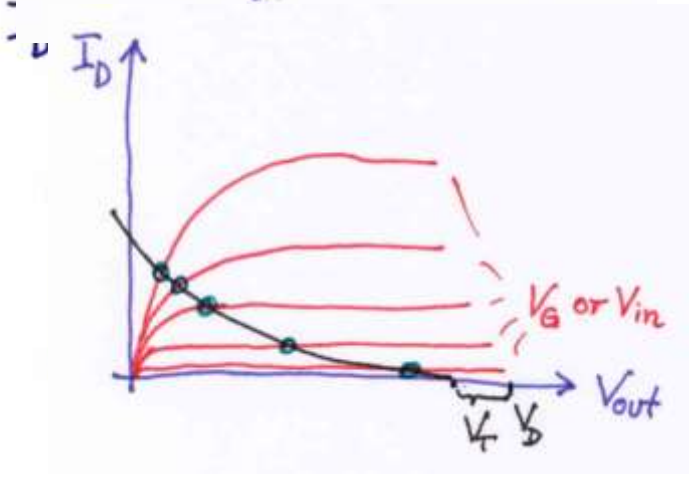
The $I_D = f(V_{out})$ behavior of the "switching transistor" (lower one) is sketched in red.

Performance of the N MOS Inverter





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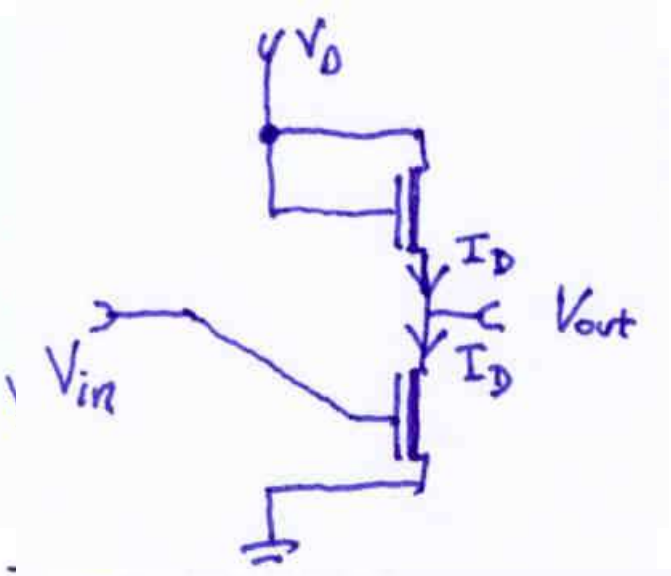
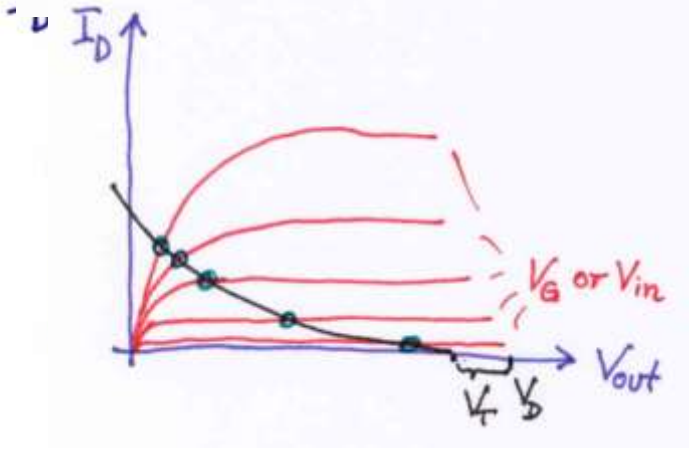
Since V_{out} is not loaded, I_D through the load transistor equals I_D through the switching transistor.

Performance of the N MOS Inverter





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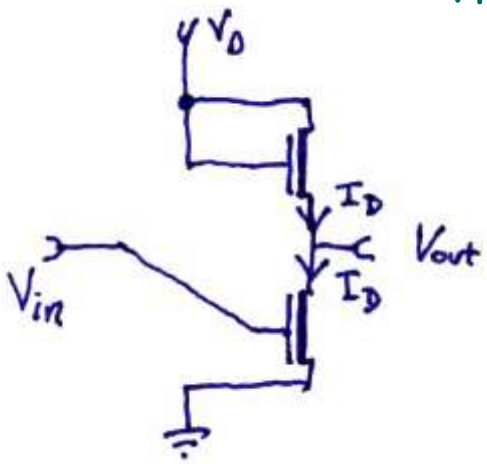
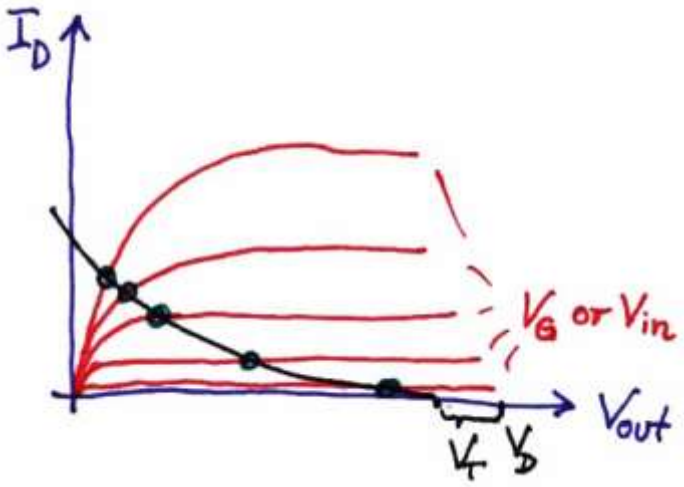
The transfer curve $V_{out} = f(V_{in})$ has the following properties: ⇨

Performance of the N MOS Inverter

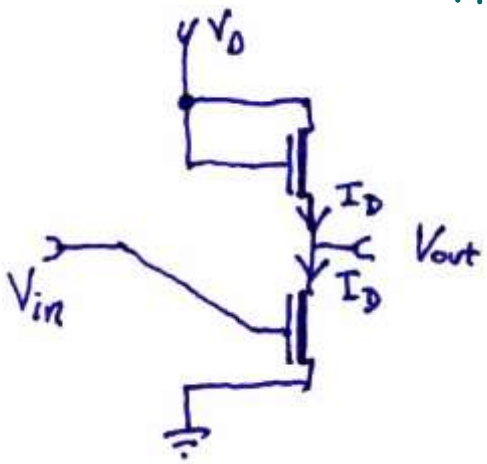
Transfer Curve for a N-MOS Enhancement Inverter



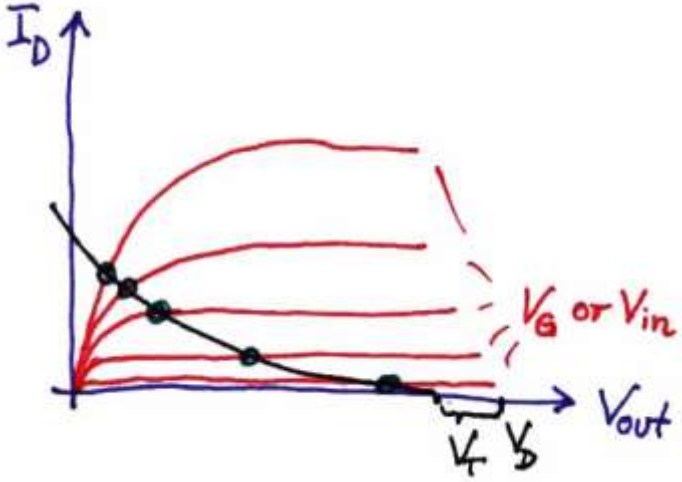


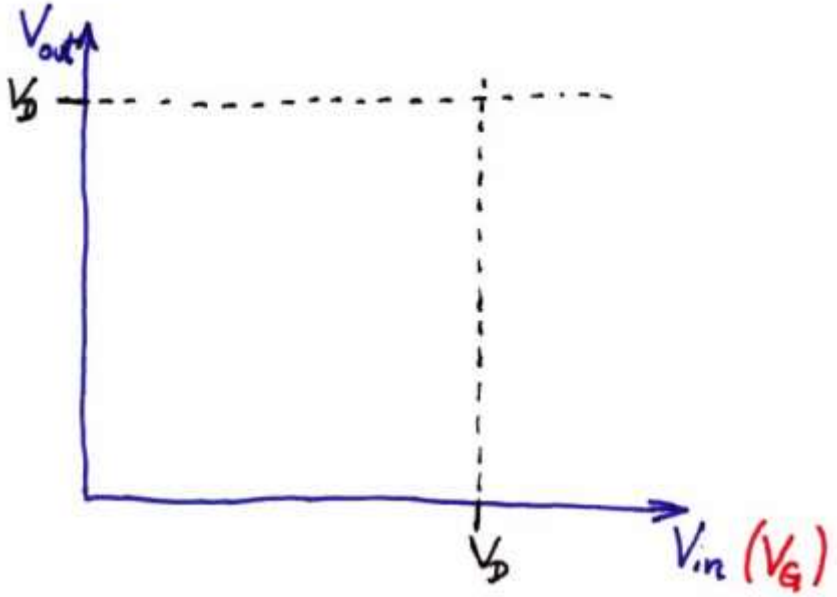
Performance of the N MOS Inverter

Transfer Curve for a N-MOS Enhancement Inverter



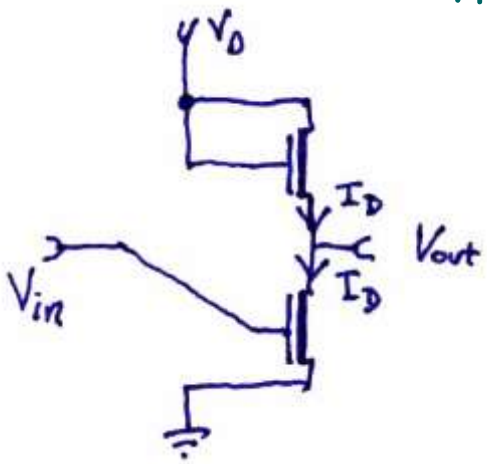
Let's call our operation voltage V_D
The maximum possible input voltage $V_{in\ max}$ is V_D
The maximum possible output voltage $V_{out\ max}$ is V_D
Raising V_{in} resp. V_G of the switching transistor.....



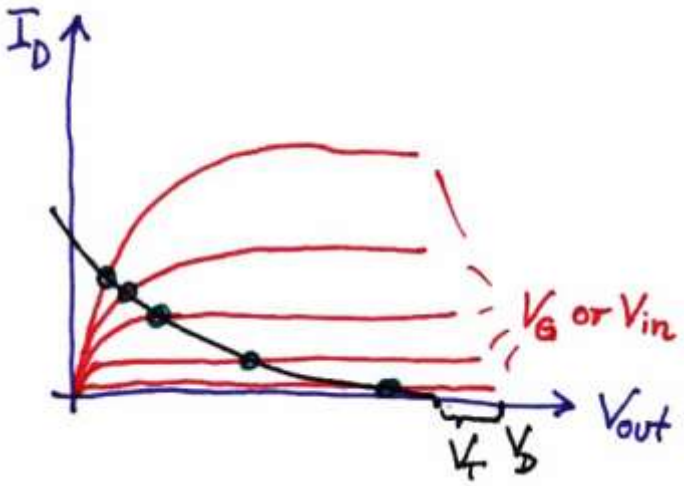


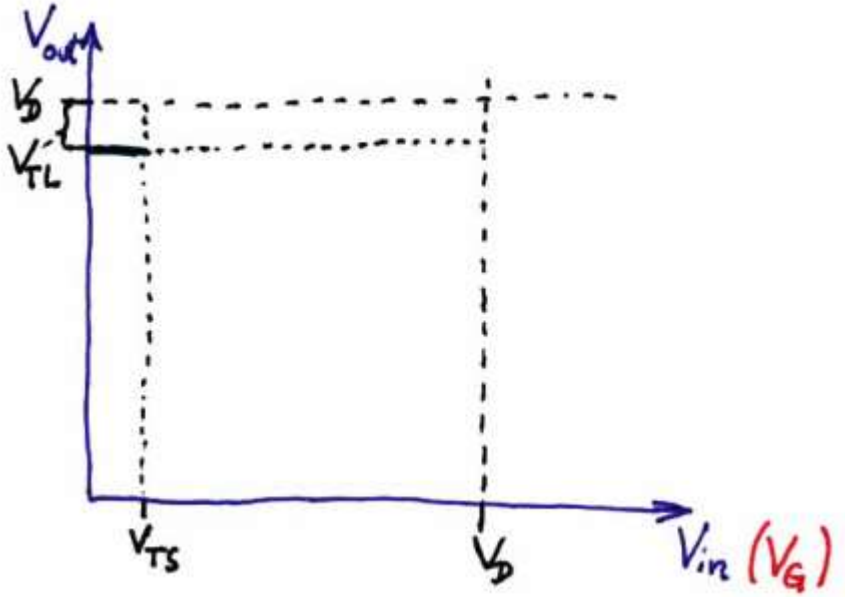
Performance of the N MOS Inverter

Transfer Curve for a N-MOS Enhancement Inverter



$V_{in} = 0 \ldots V_{TS} \Rightarrow V_{out} = V_D - V_{TL}$





Performance of the N MOS Inverter

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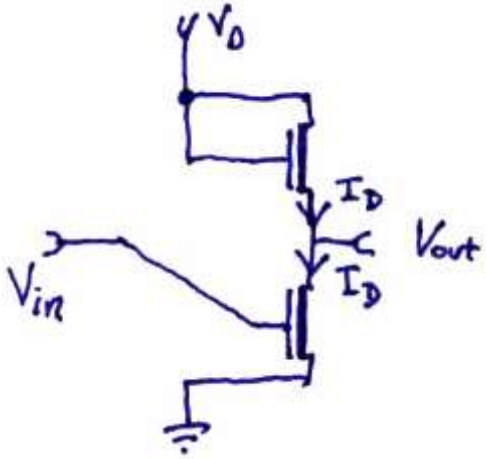
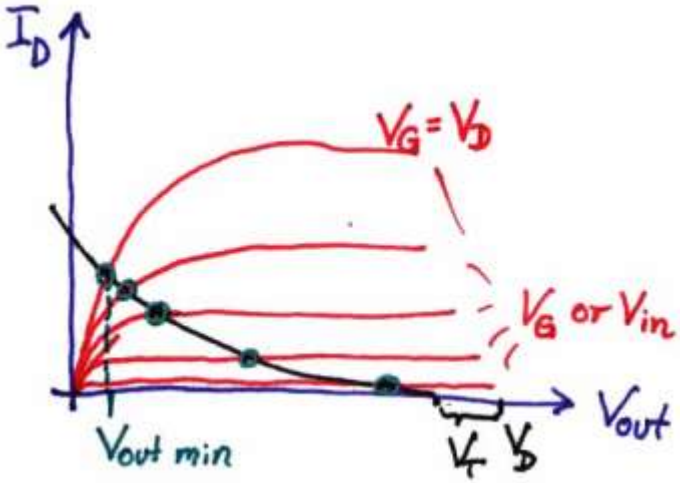
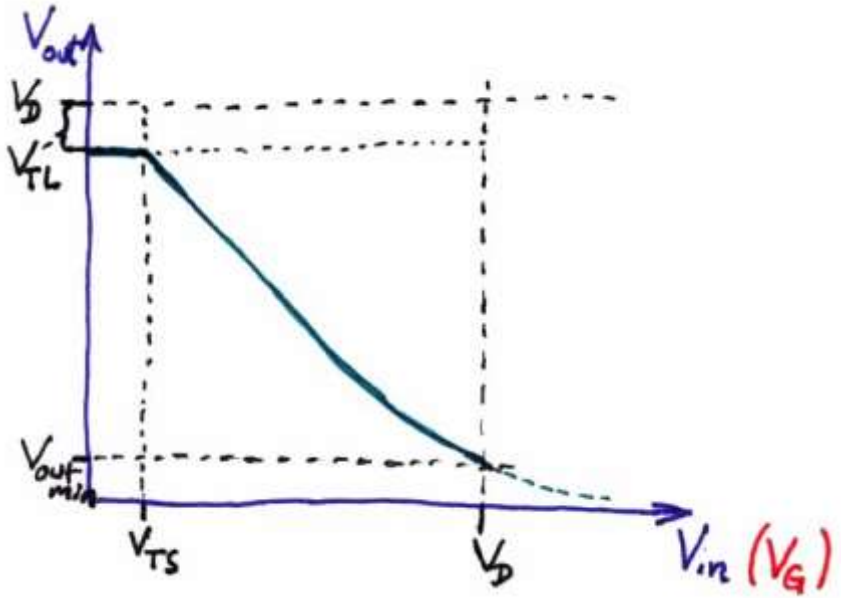


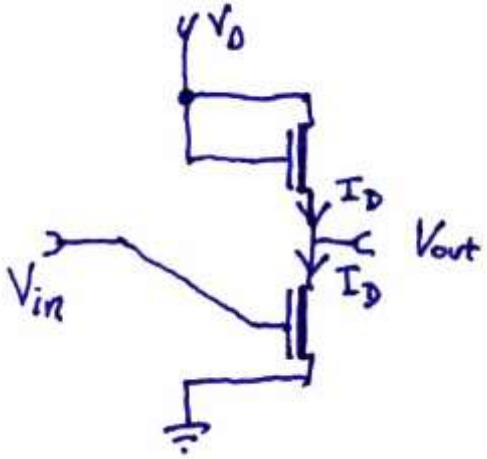
When V_{in} is further increased V_{out} drops until it reaches a minimum value.





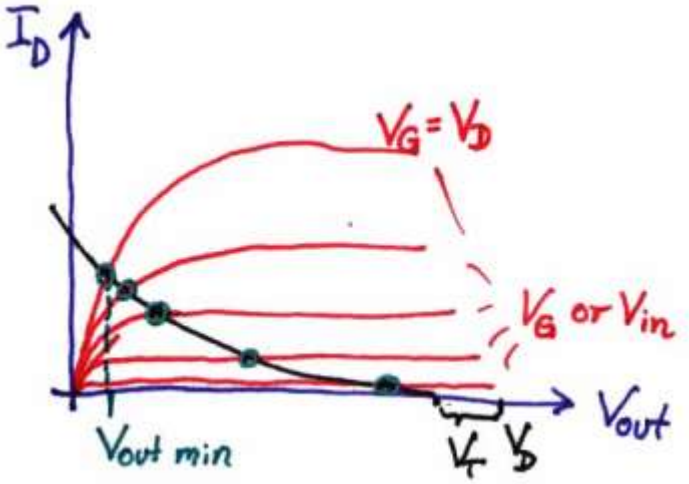
Performance of the N MOS Inverter

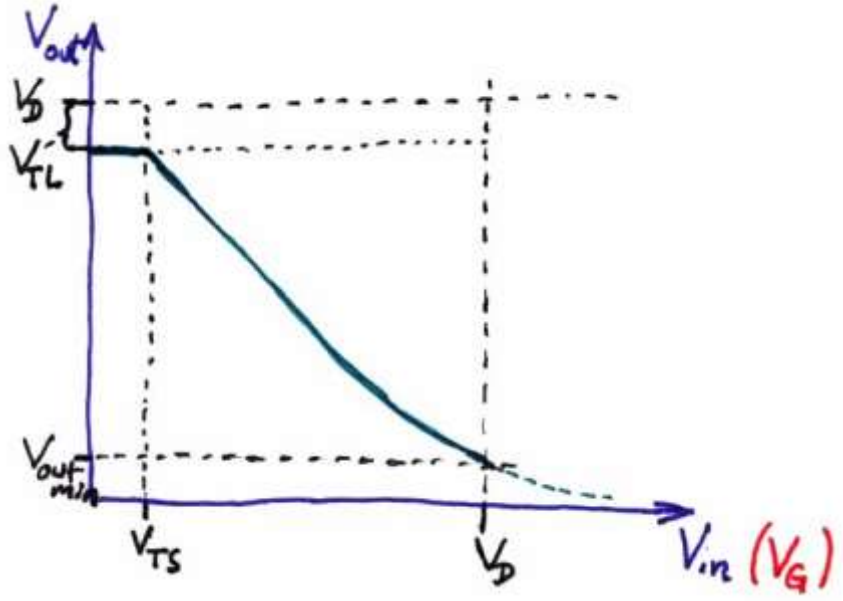
Transfer Curve for a N-MOS Enhancement Inverter



Properties of the Transfer curve:

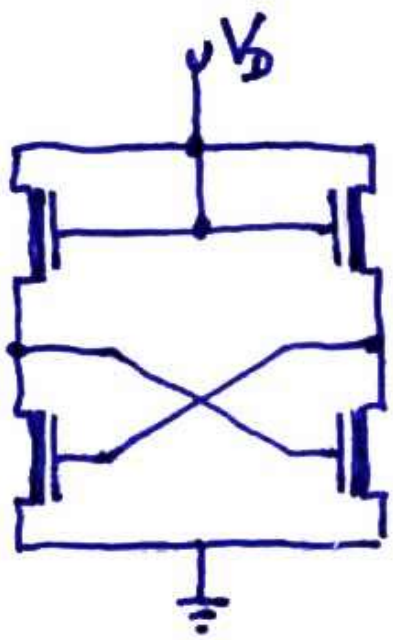
- $V_{out\ max}$ does not reach V_D
- $V_{out\ min}$ does not reach zero
- moderate steepness depending on the W/L ratio





2.3 SRAM Zelle

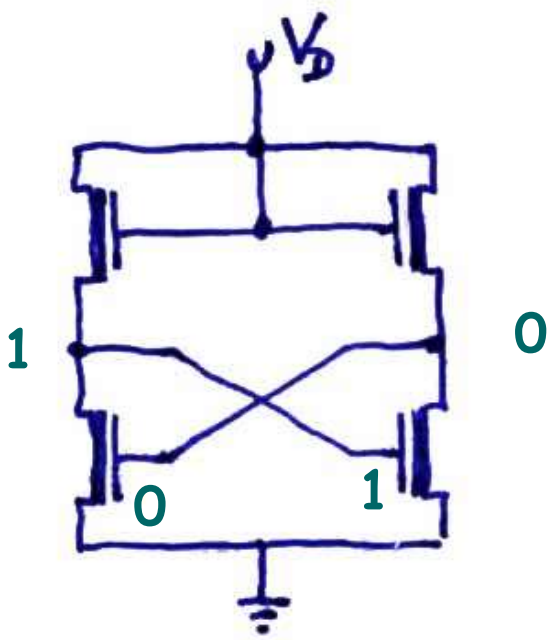
Two Inverters make a Flip-Flop



2.3 SRAM Zelle

Two Inverters make a Flip-Flop

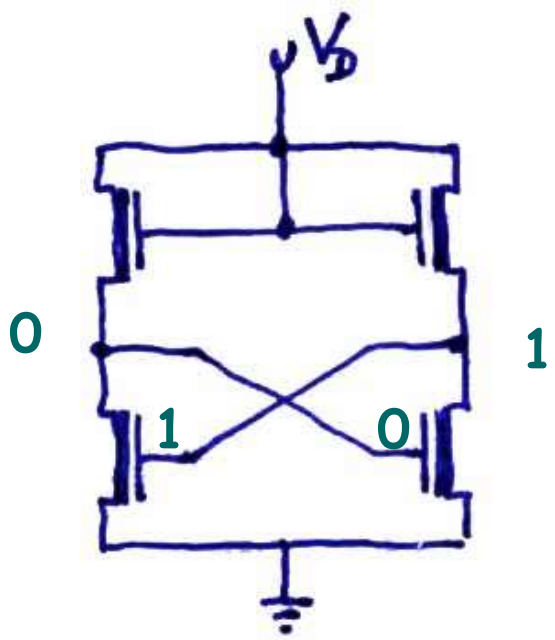
With two stable states like this one:



2.3 SRAM Zelle

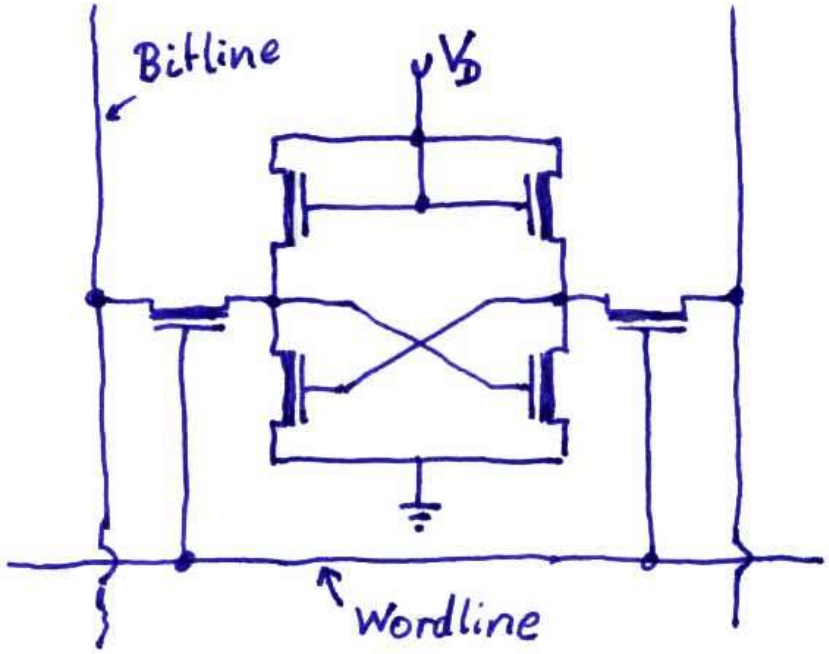
Two Inverters make a Flip-Flop

Or this one:



2.3 SRAM Zelle

Using two additional Transistors a SRAM cell is created



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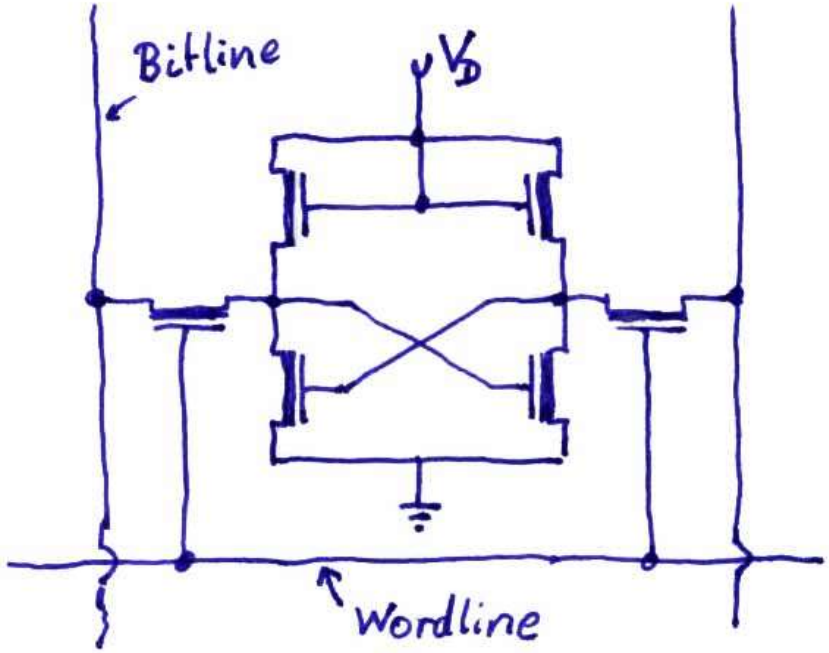


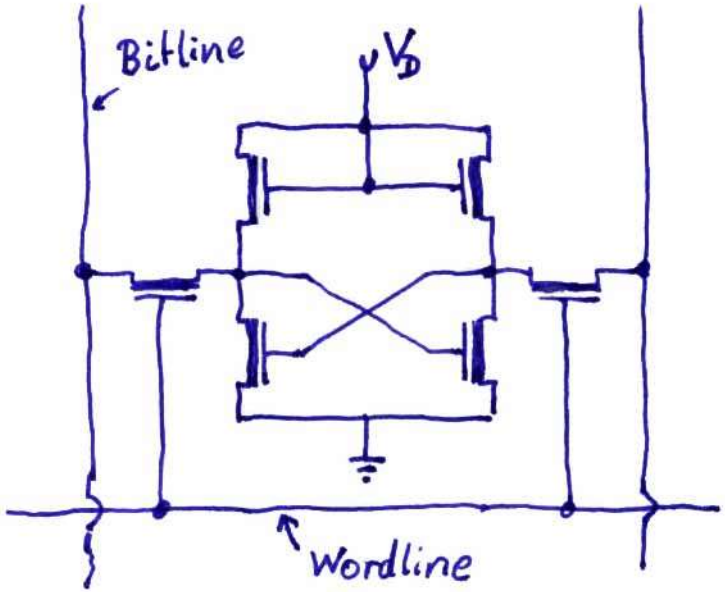
Continue

"SCT_SS20_07.05" 04:10

VIDEO CAMPUS SACHSEN

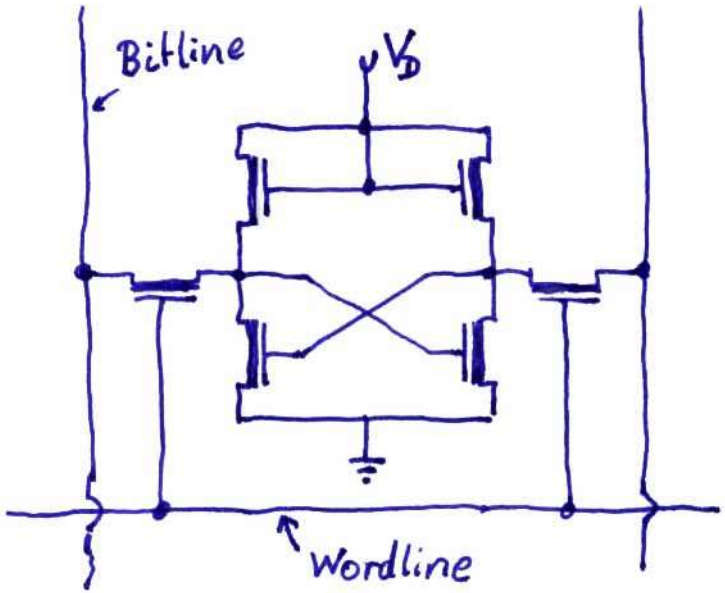
2.3 SRAM in metal gate enhancement NMOS

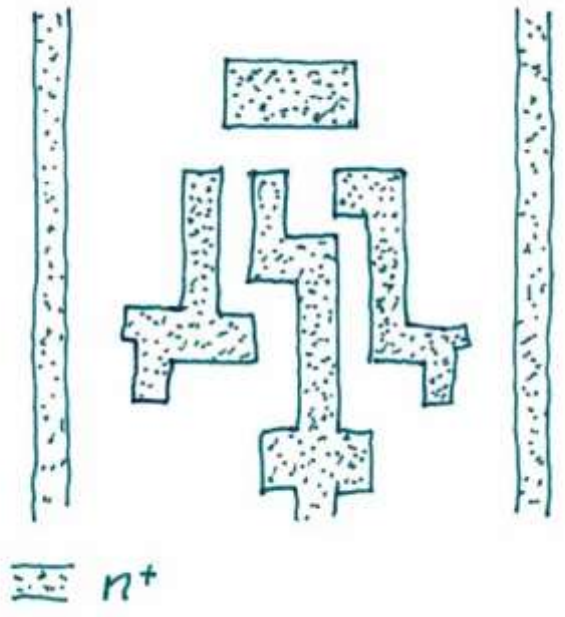
The layout consist of the 4 mask levels.



2.3 SRAM in metal gate enhancement NMOS

The layout consist of the 4 mask levels. n^+ diffusion / p substrate





2.3 SRAM in metal gate enhancement NMOS

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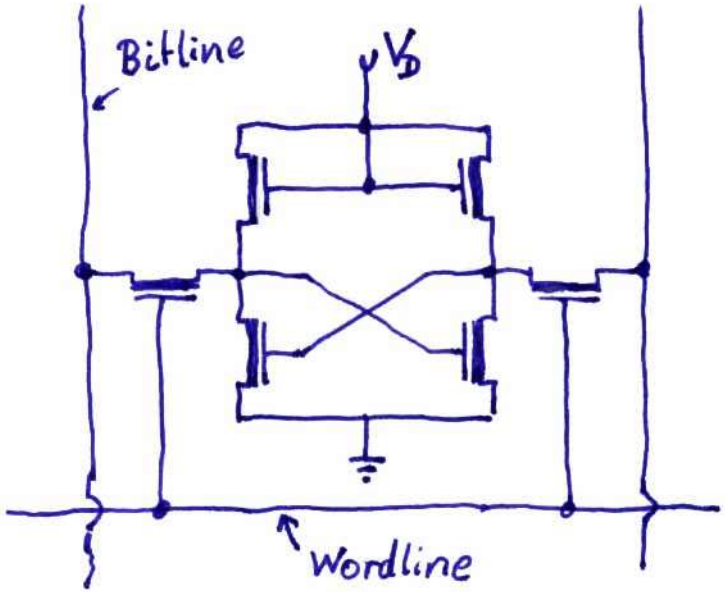
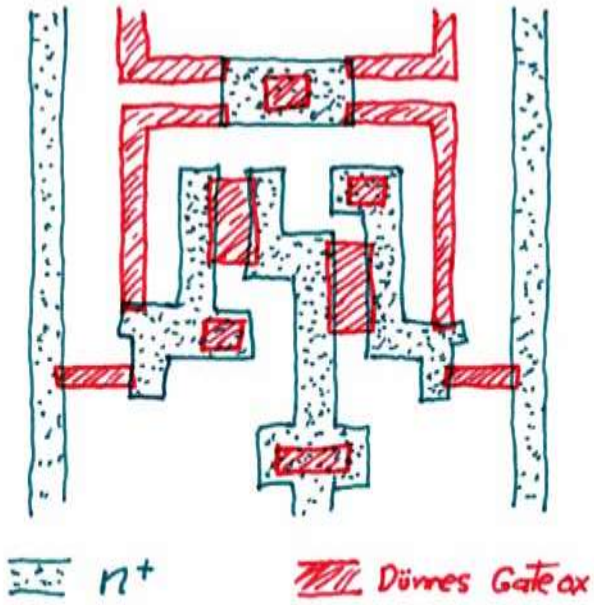


Gate Oxide



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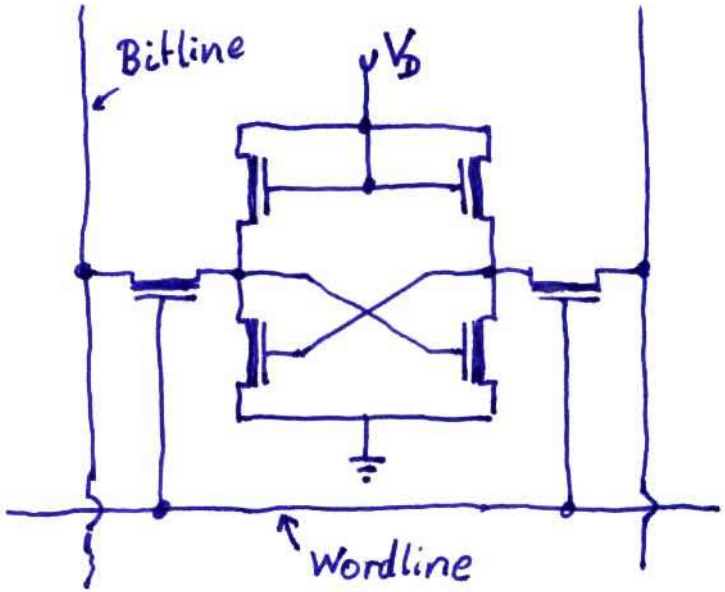
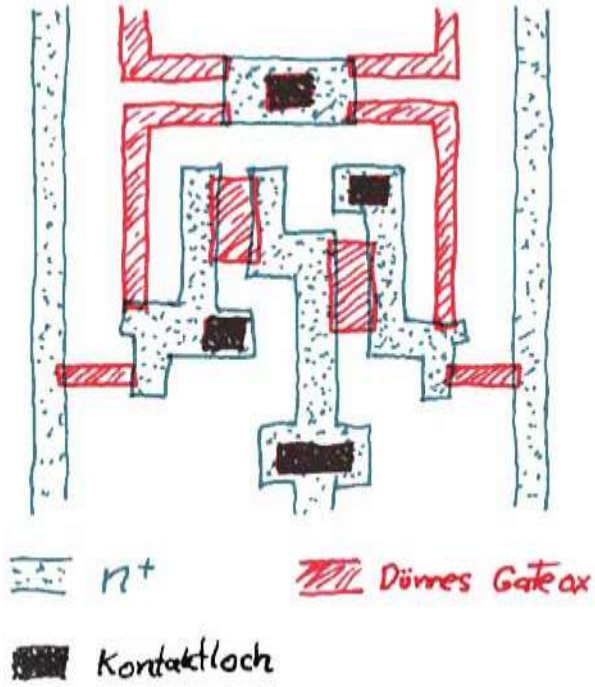


Contact open



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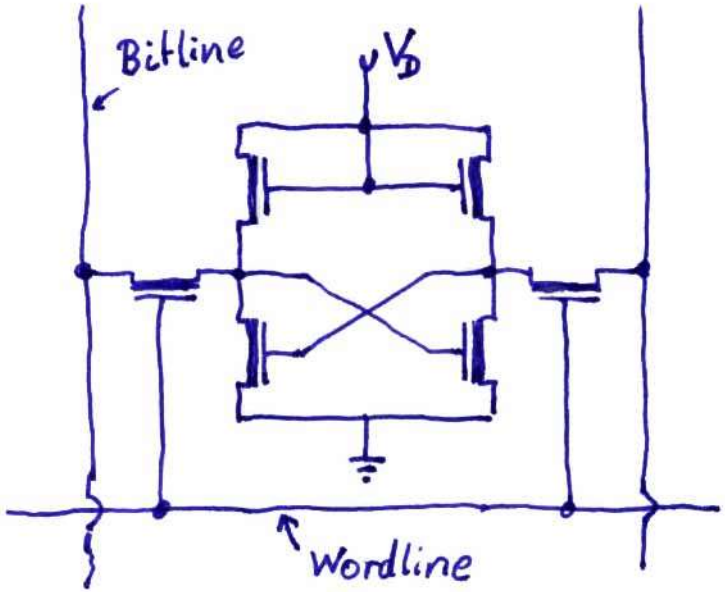
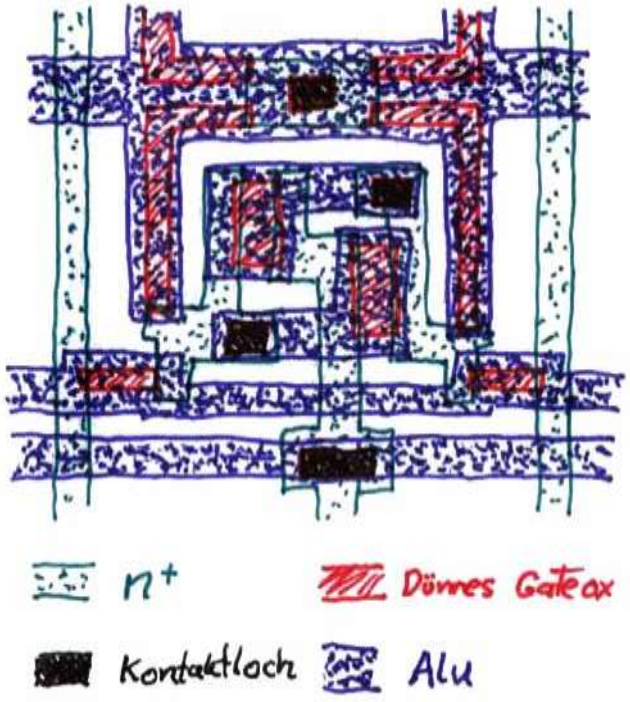


Metal Lines



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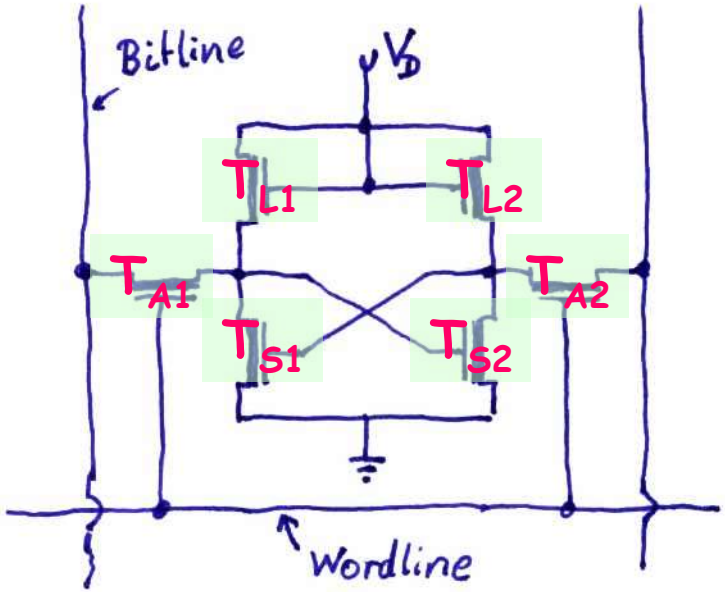
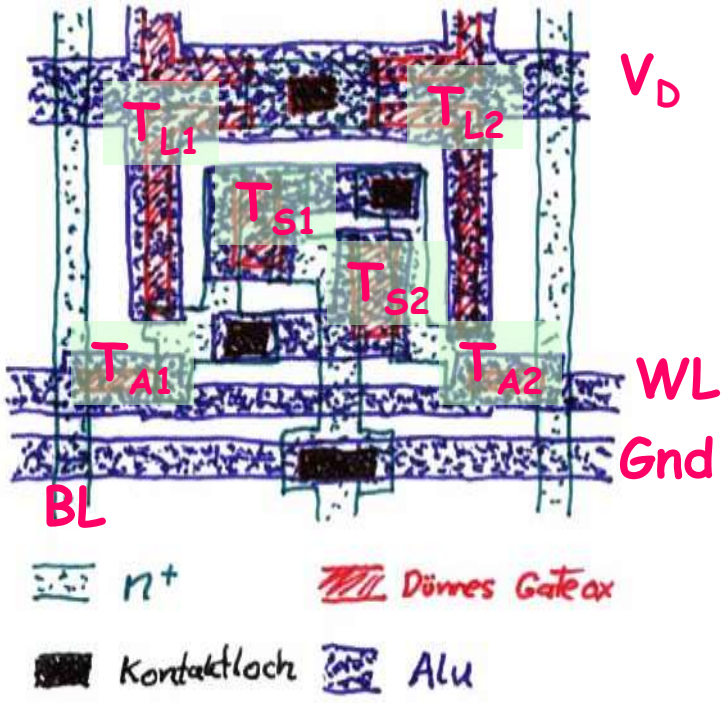
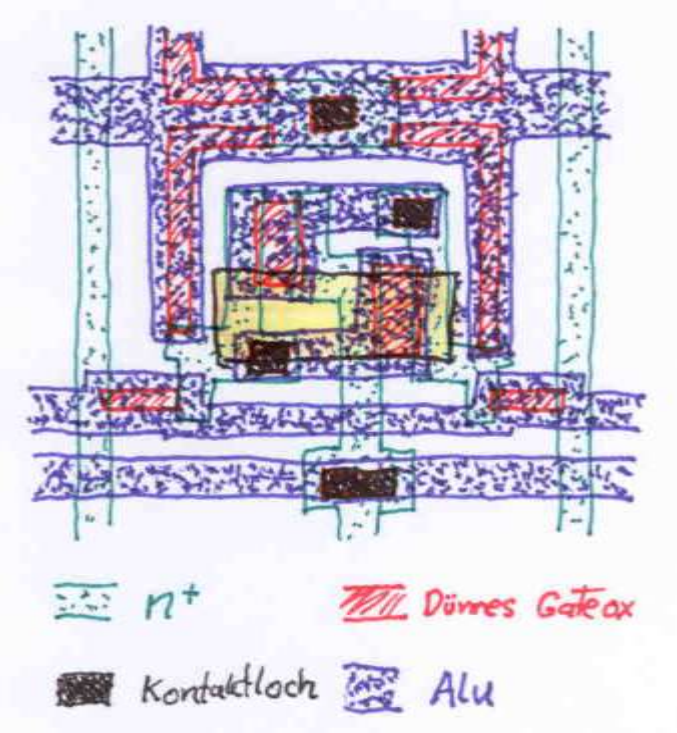
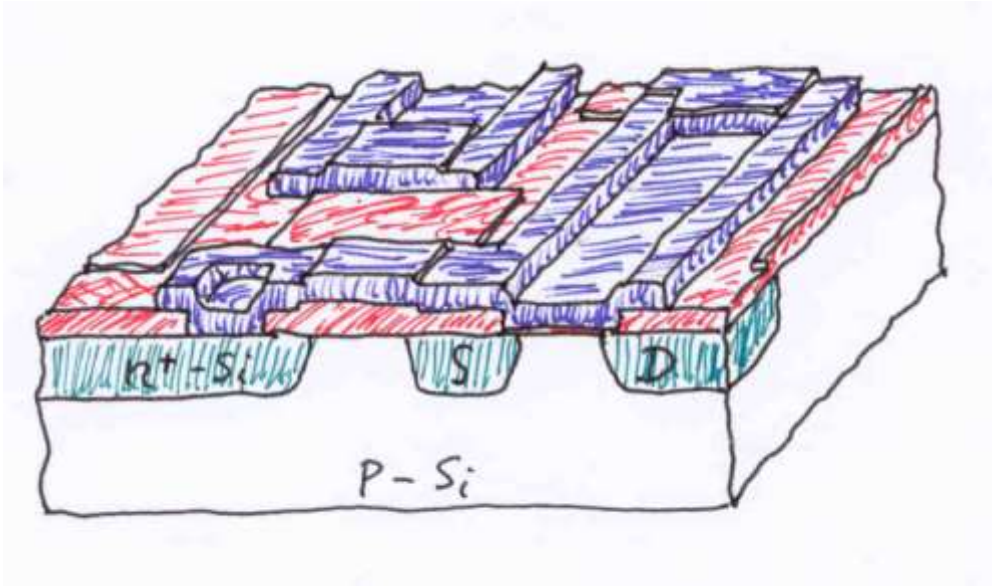


Metal Lines



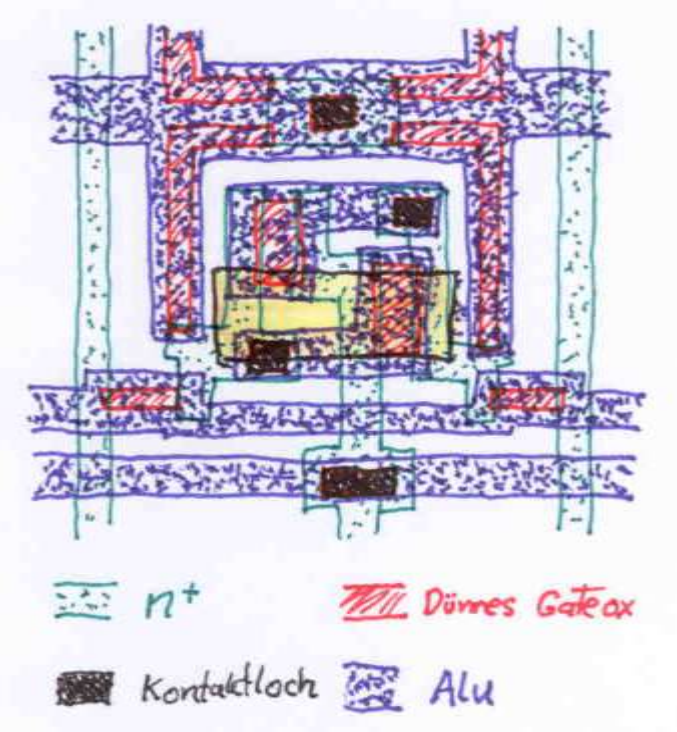
SRAM in metal gate enhancement NMOS

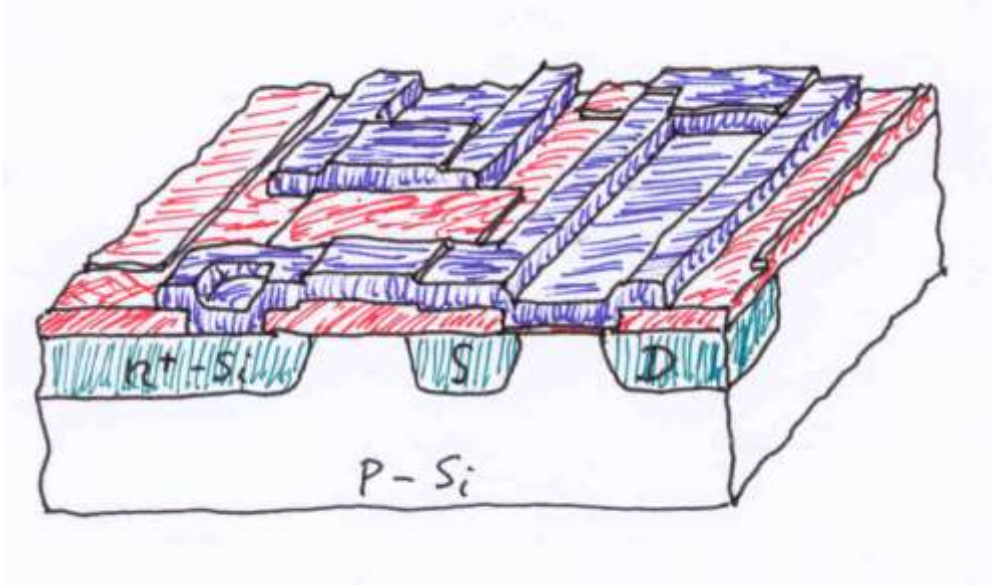




SRAM in metal gate enhancement NMOS

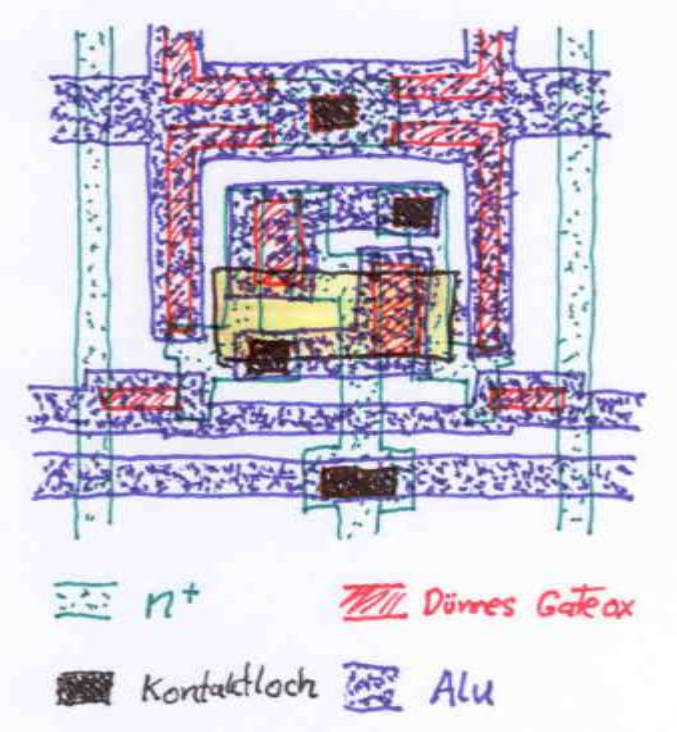
Notice the W/L Ratio of the different Transistors!

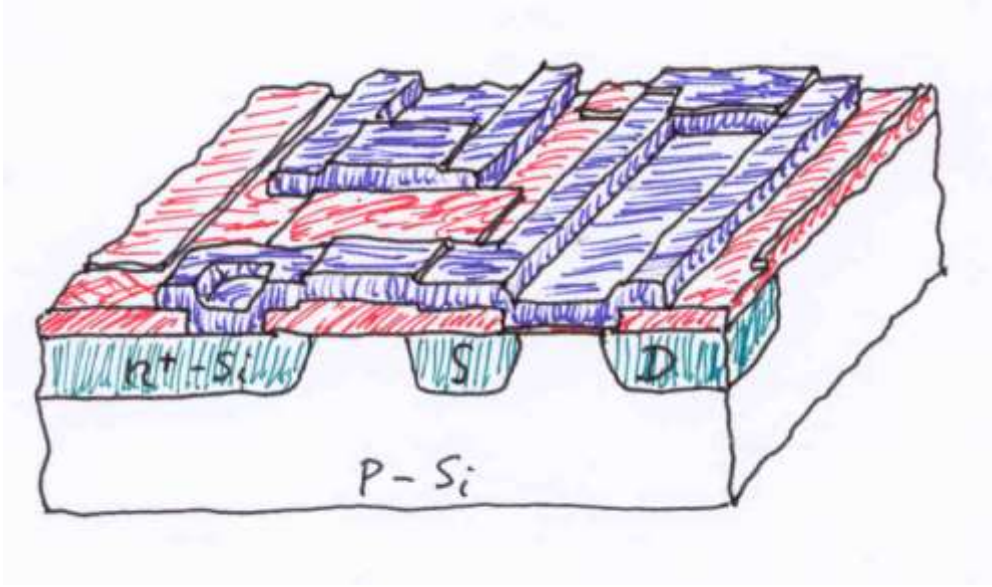




SRAM in metal gate enhancement NMOS

Notice the W/L Ratio of the different Transistors!
n^+ Diffusion not only used for Source/Drain but also as conductor line!





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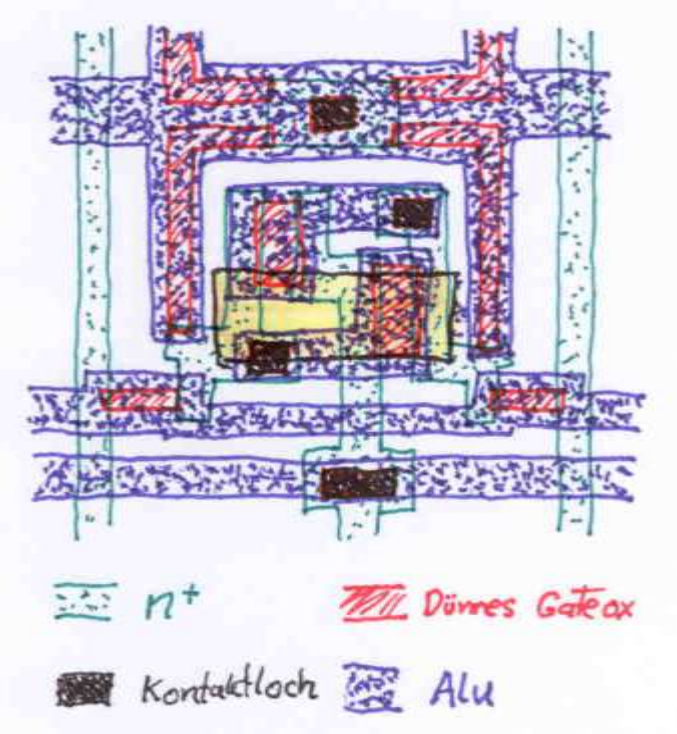

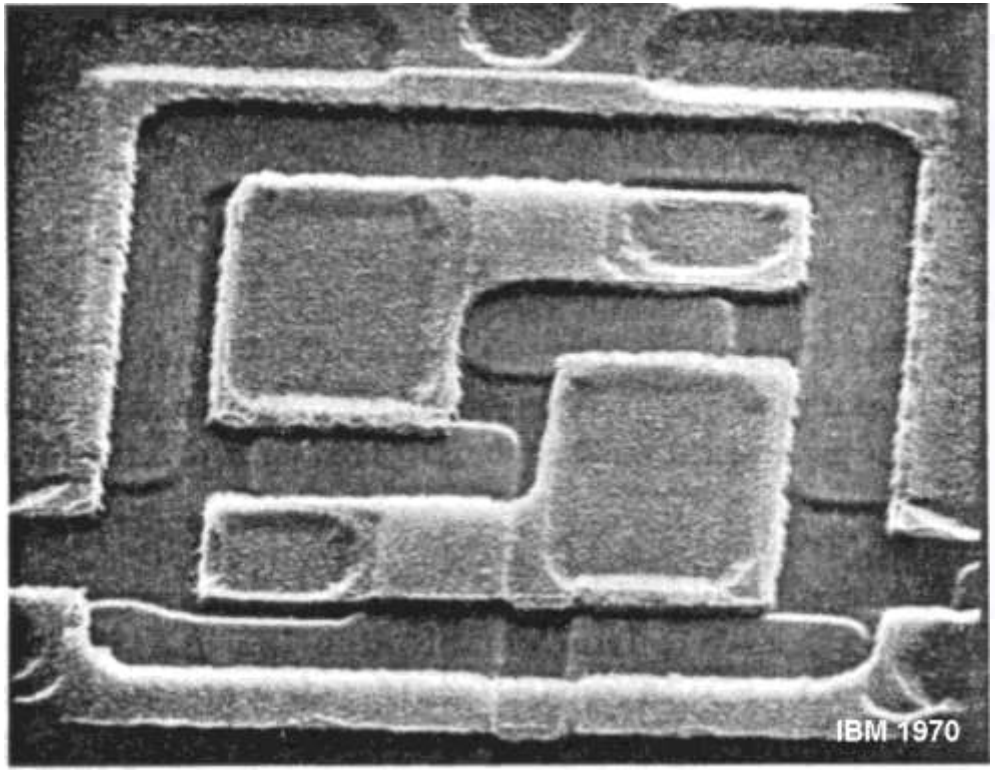

»Wissen schafft Brücken.«