TECHNISCHE UNIVERSITÄT DRESDEN

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Lecture SCT2 – Process Integration

8. Web-based virtual Lecture: June 10 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here  

"SCT_SS21_08.1" 12:31

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Outline

Review:
- SCT Basics
- MOS Capacitor
- MOS-Cap-CV
- MOS-FET
  Triode- Saturation-
  Subthreshold range
- Al-Gate FET
- Inverter to SRAM

Today:
SRAM fabrication + V_T

SC-Basics

http://www.computerhistory.org/siliconengine/timeline/

TECHNISCHE UNIVERSITÄT DRESDEN

Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

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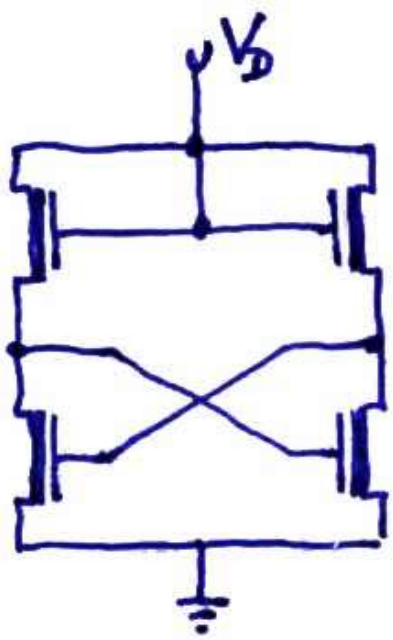
Continue ➡ VIDEO CAMPUS SACHSEN
"SCT_SS20_08.2" 15:35

http://www.computerhistory.org/siliconengine/timeline/

2.3 SRAM Cell

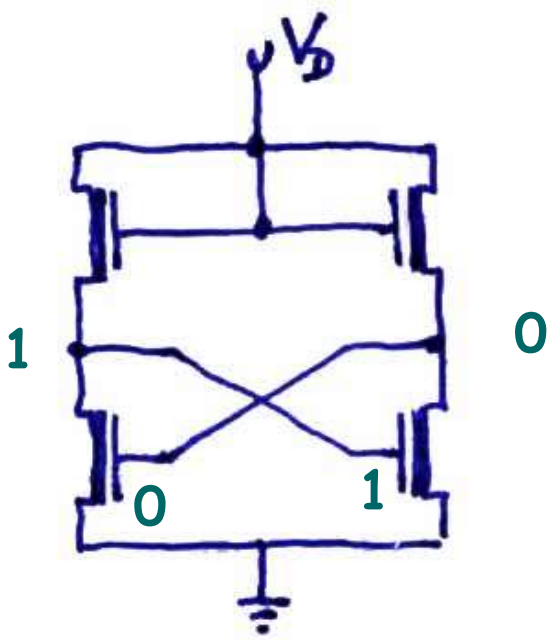
Two Inverters make a Flip-Flop



2.3 SRAM Cell

Two Inverters make a Flip-Flop

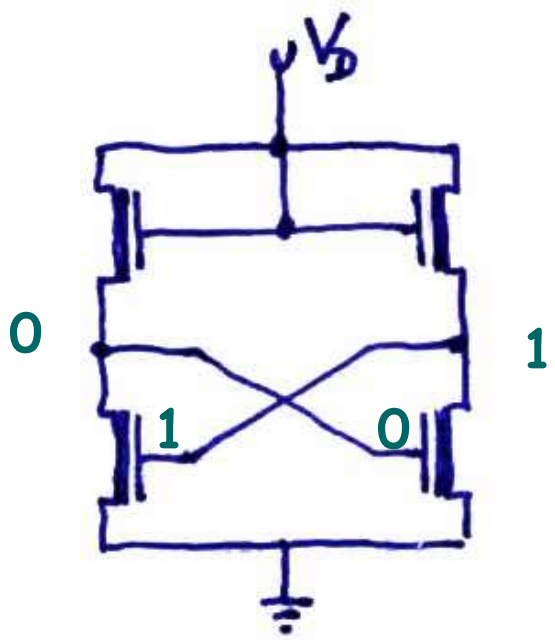
With two stable states like this one:



2.3 SRAM Cell

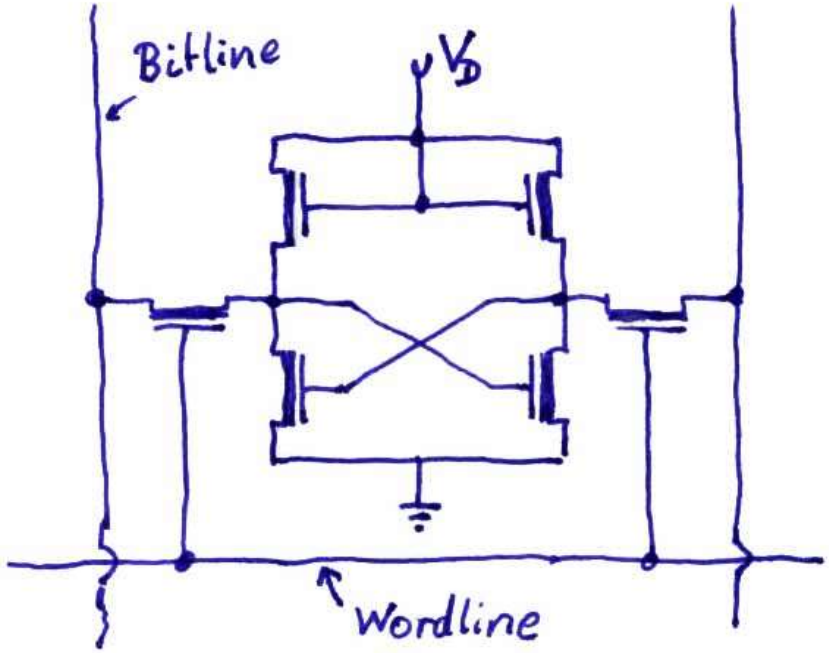
Two Inverters make a Flip-Flop

Or this one:



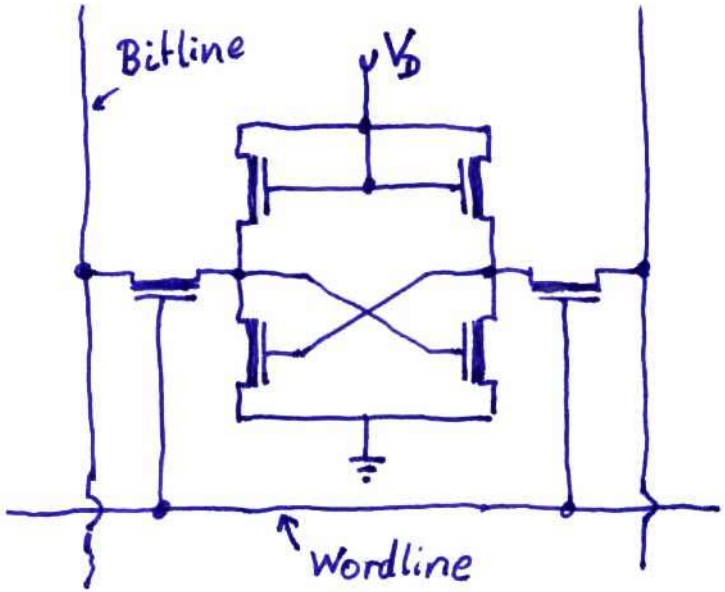
2.3 SRAM Cell

Using two additional Transistors a SRAM cell is created



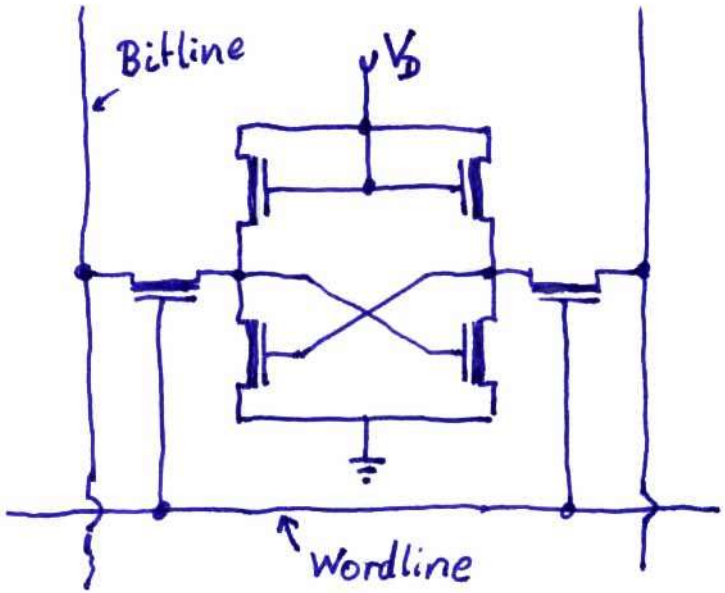
2.3 SRAM in metal gate enhancement NMOS

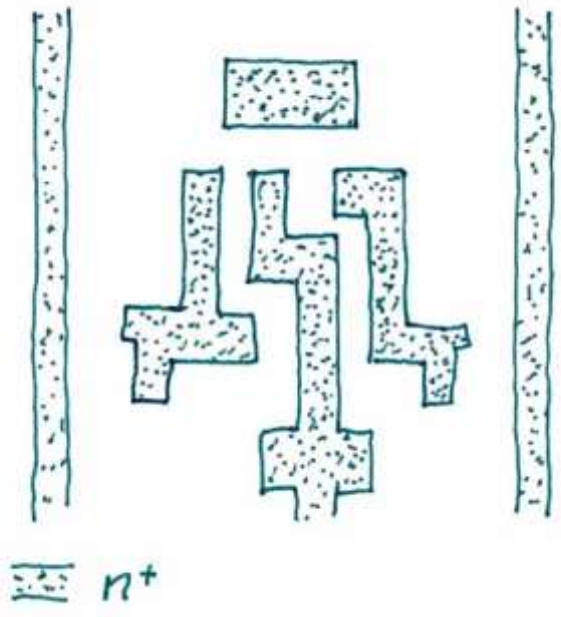
The layout consist of the 4 mask levels.



2.3 SRAM in metal gate enhancement NMOS

The layout consist of the 4 mask levels. n^+ diffusion / p substrate





2.3 SRAM in metal gate enhancement NMOS

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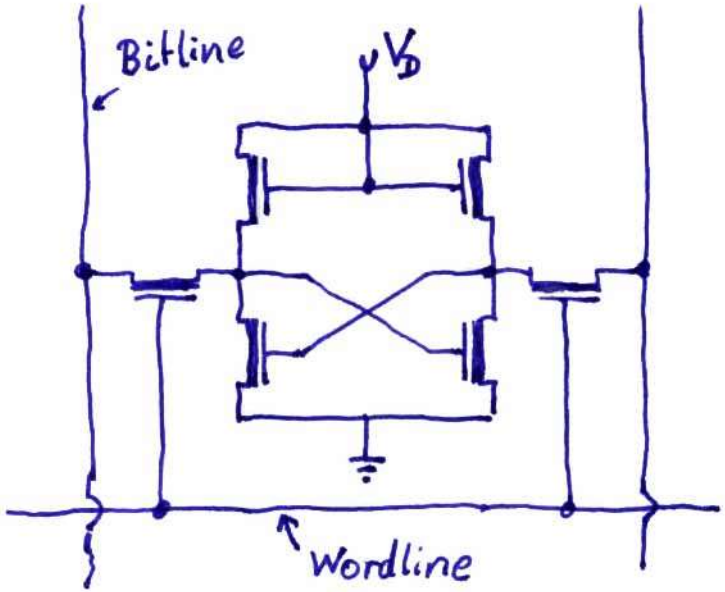
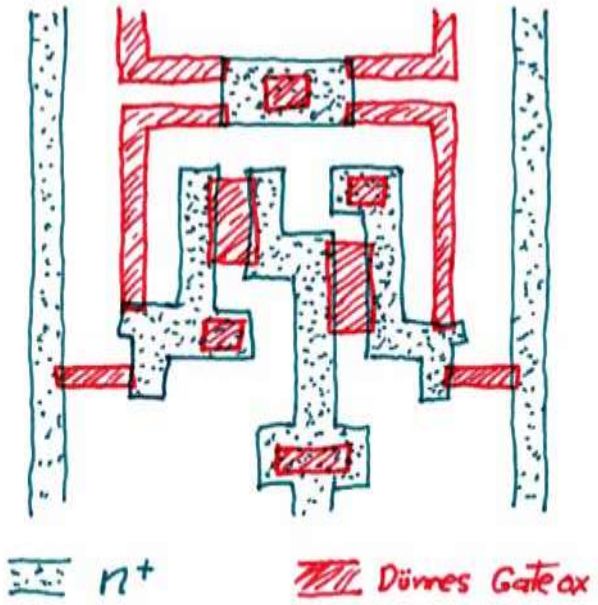


Gate Oxide



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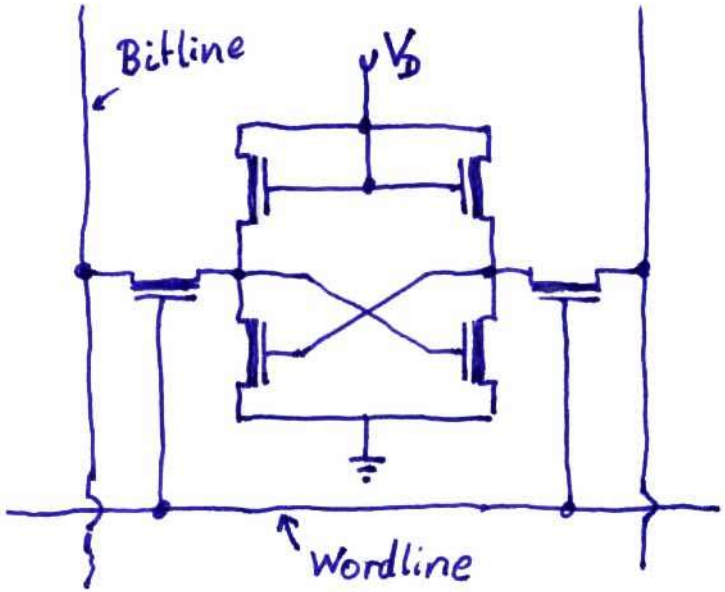
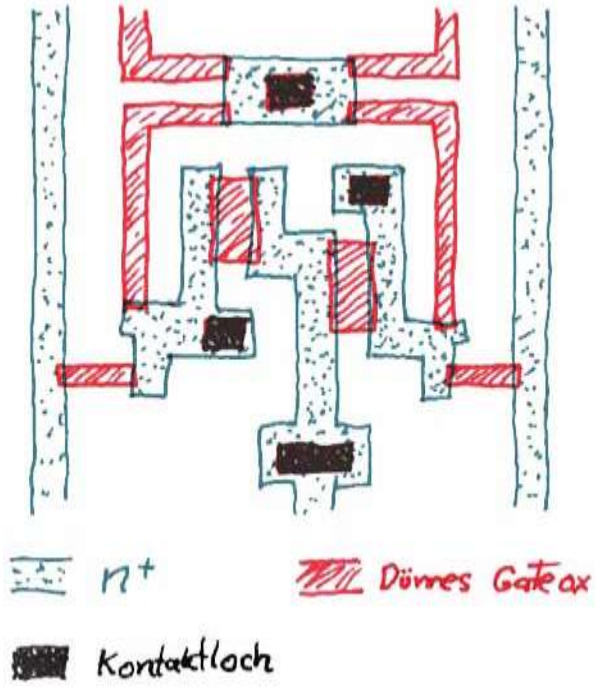


Contact open



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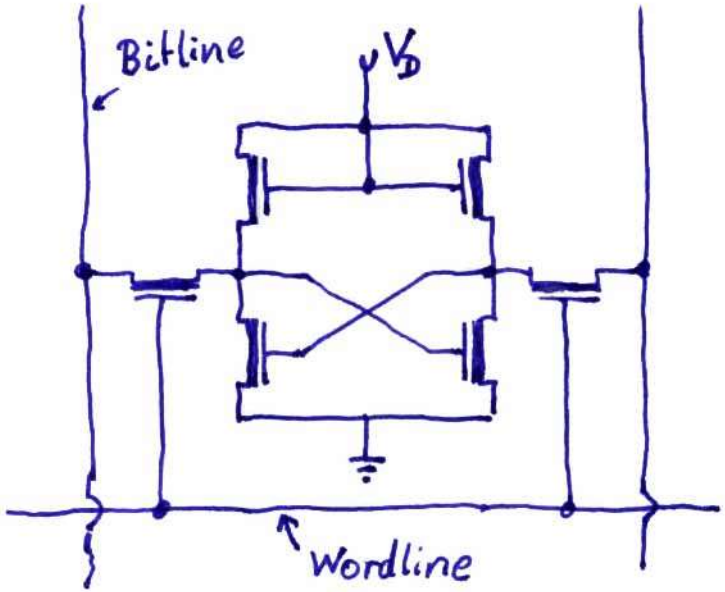
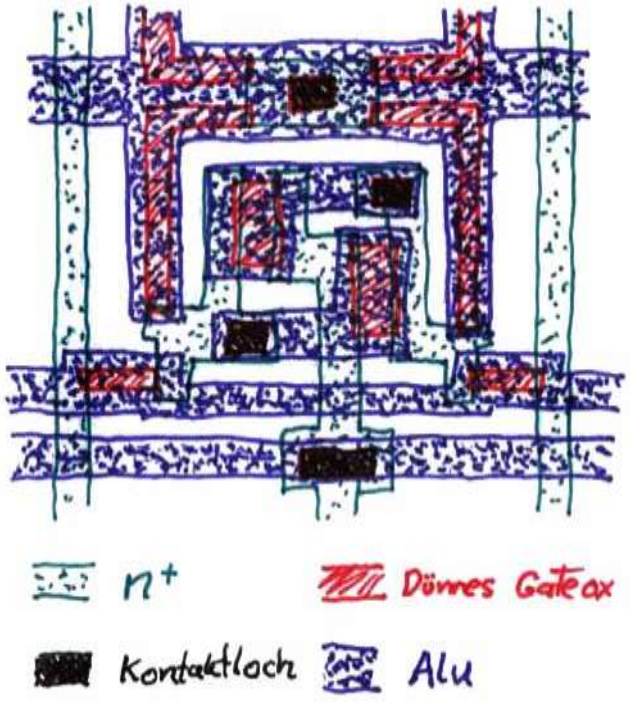


Metal Lines



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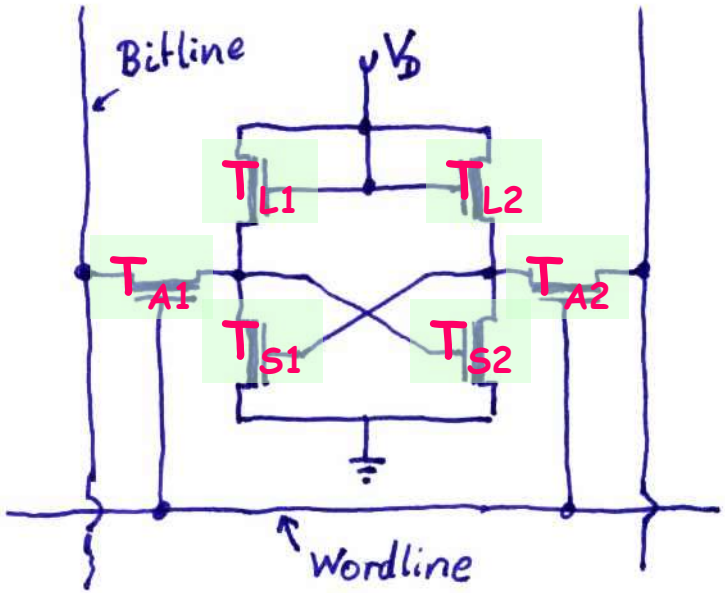
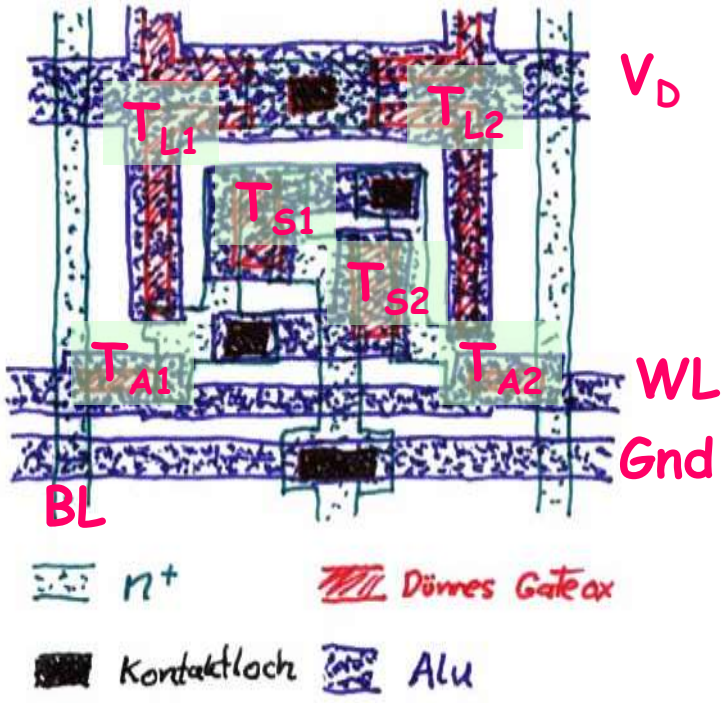
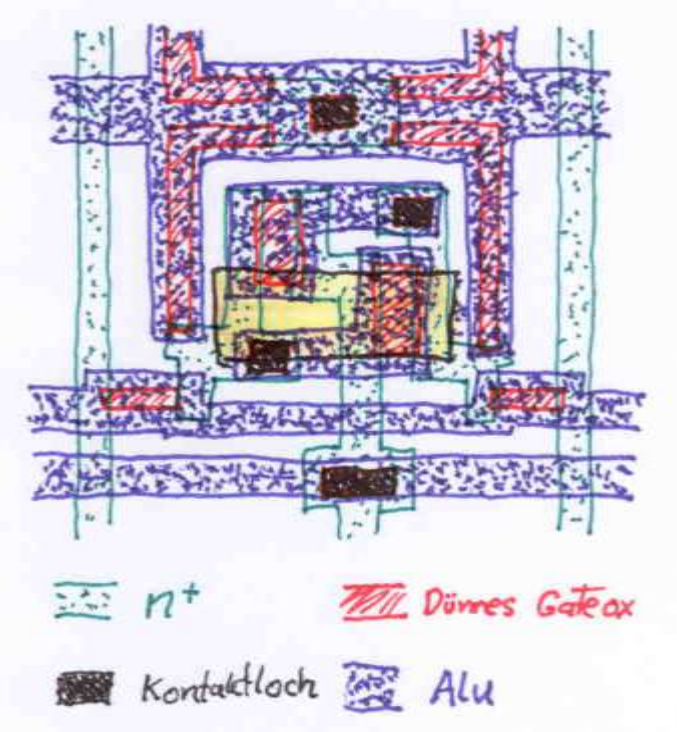
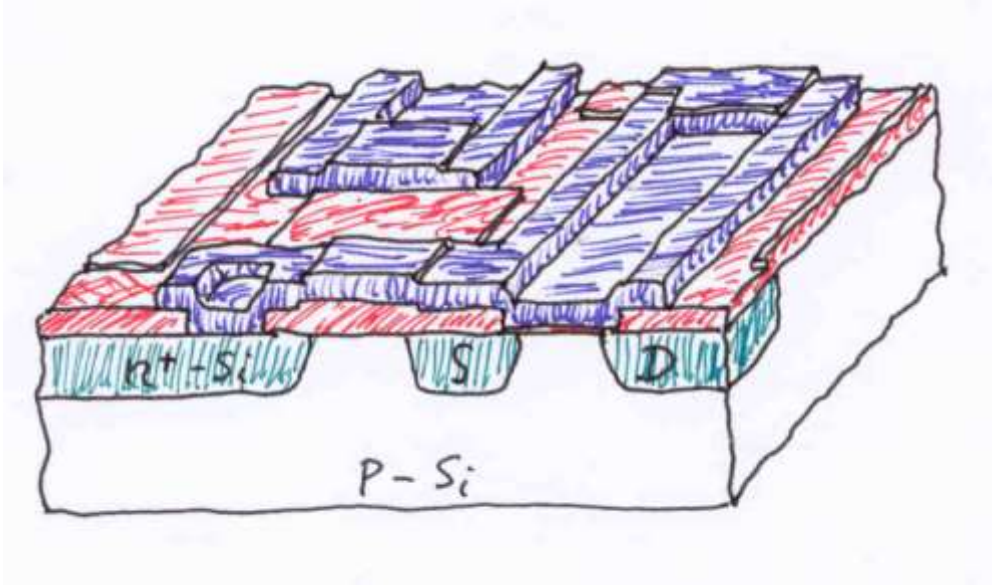


Metal Lines



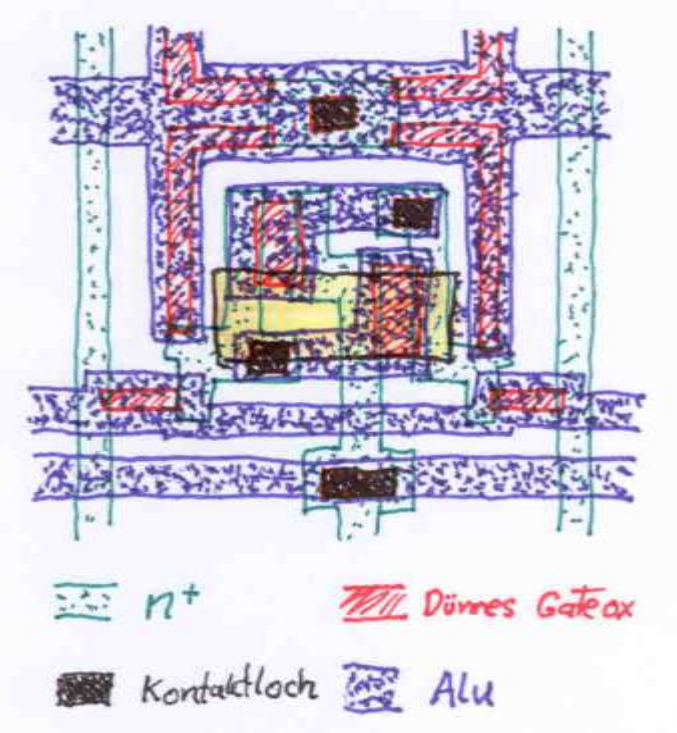
SRAM in metal gate enhancement NMOS

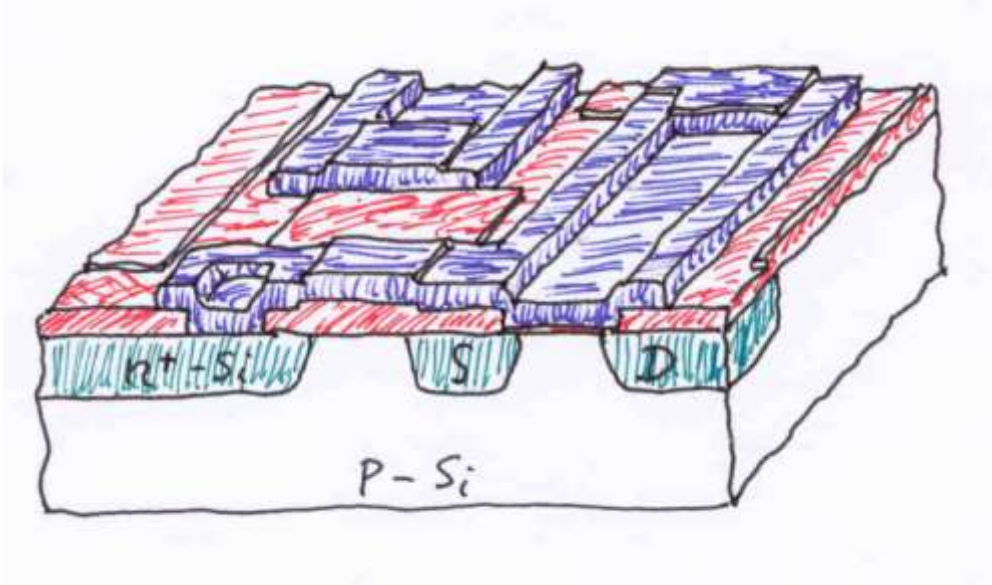




SRAM in metal gate enhancement NMOS

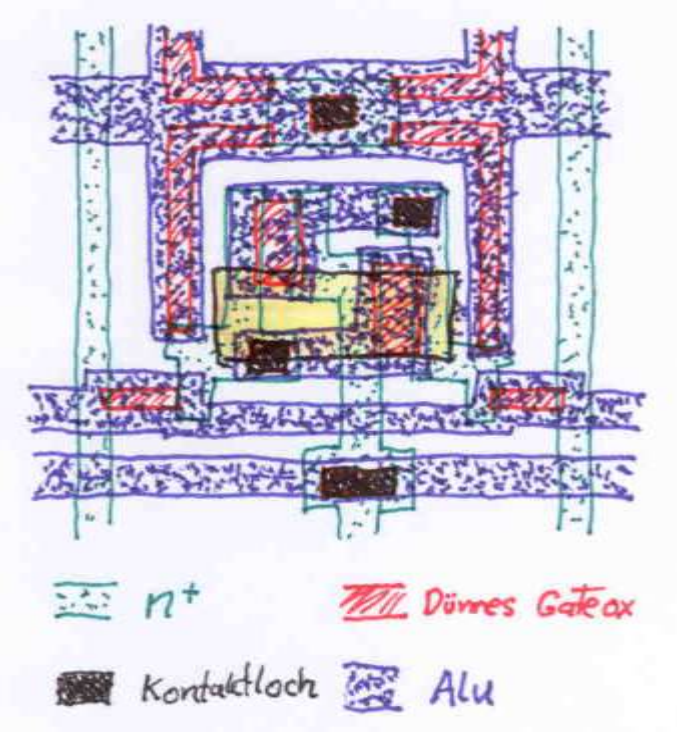
Notice the W/L Ratio of the different Transistors!

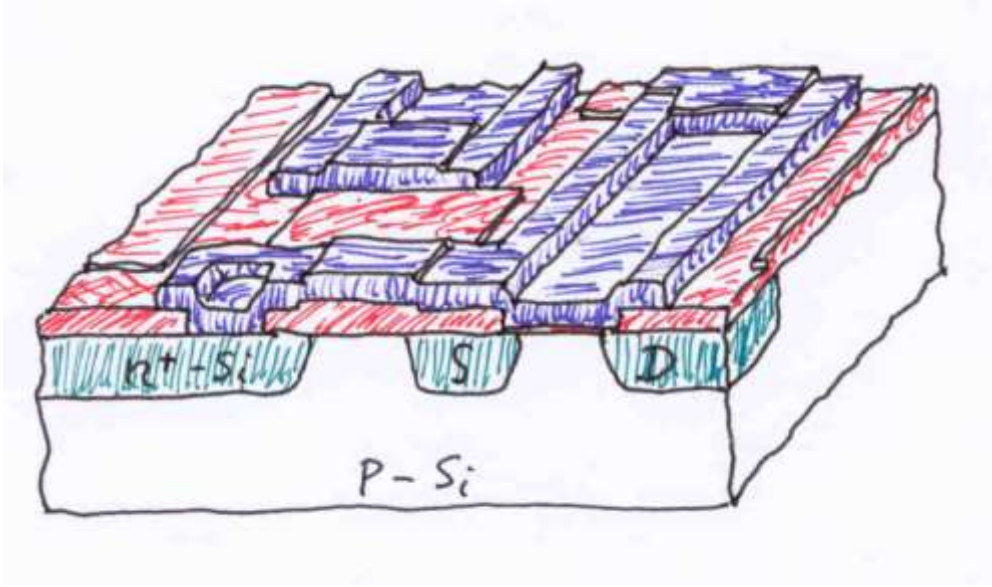




SRAM in metal gate enhancement NMOS

Notice the W/L Ratio of the different Transistors!
n^+ Diffusion not only used for Source/Drain but also as conductor line!





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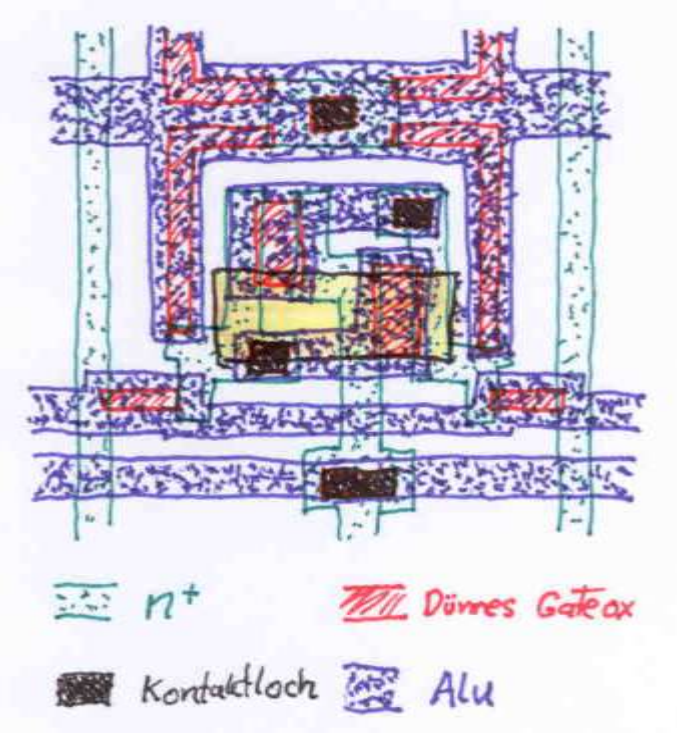
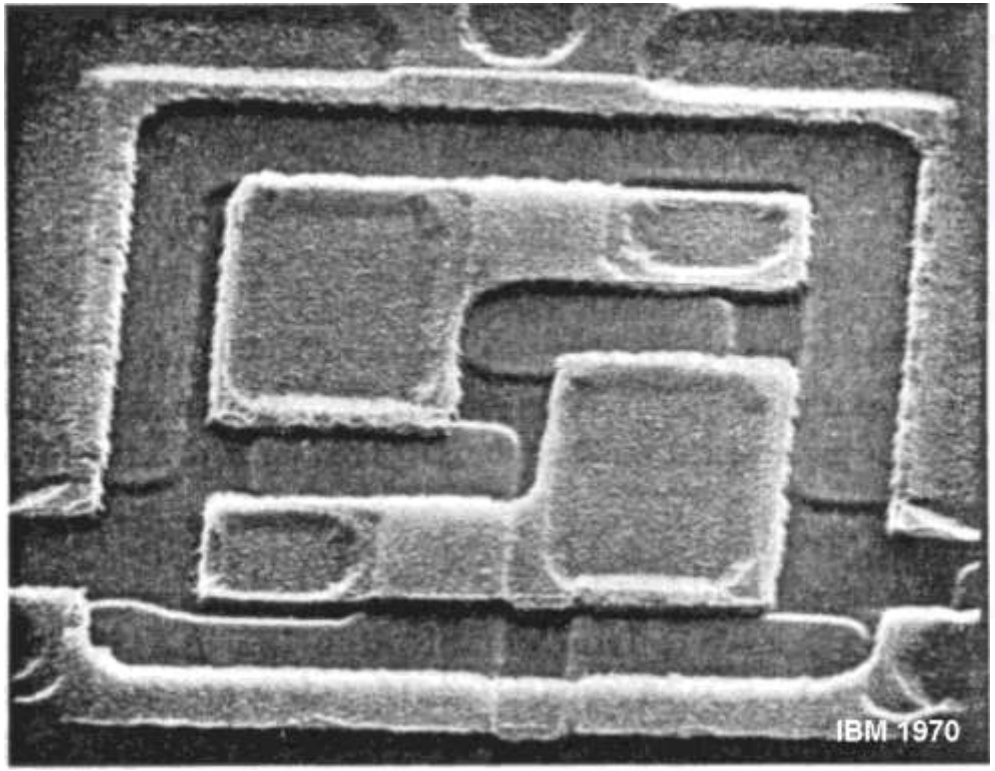
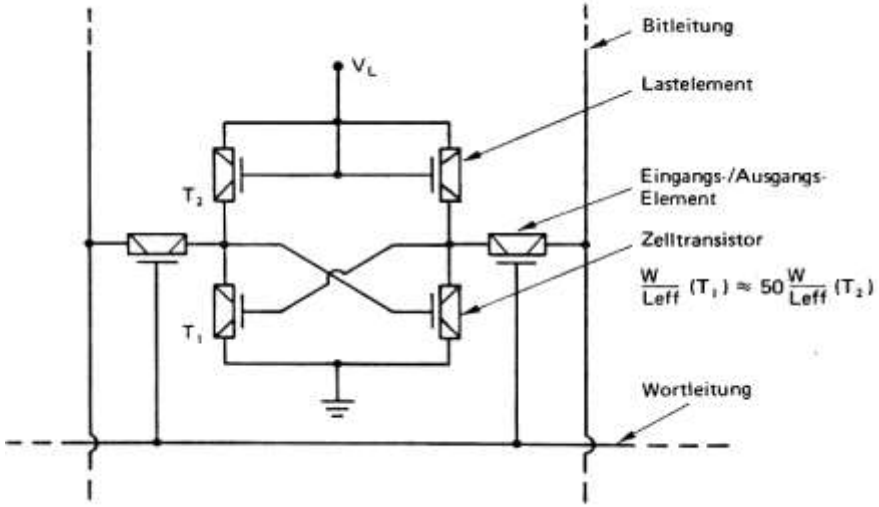
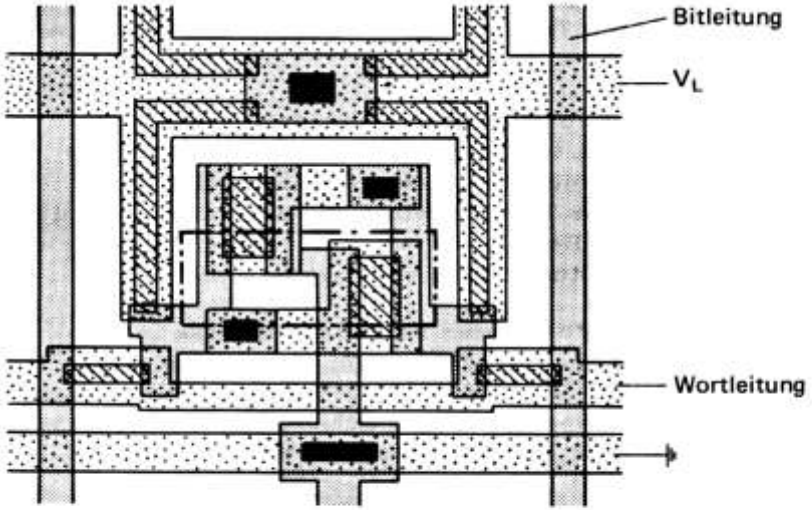
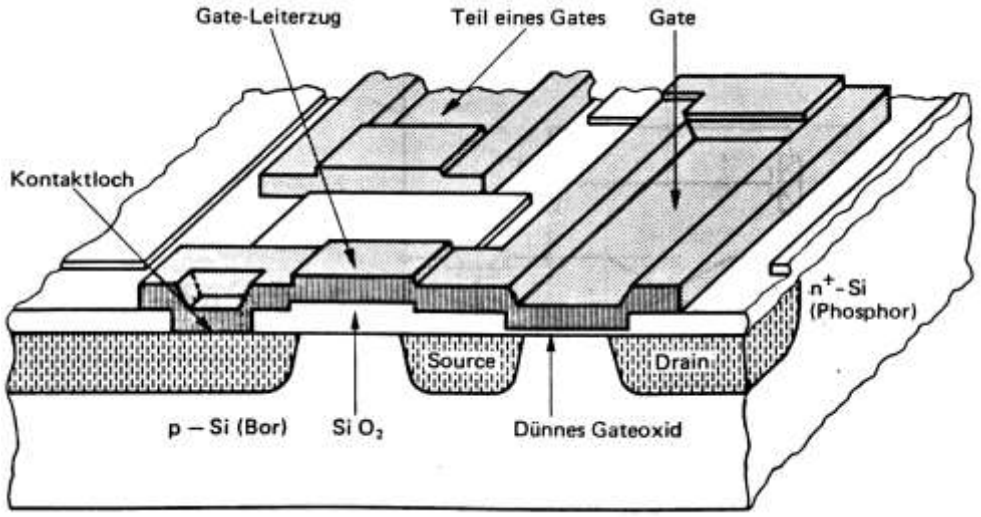










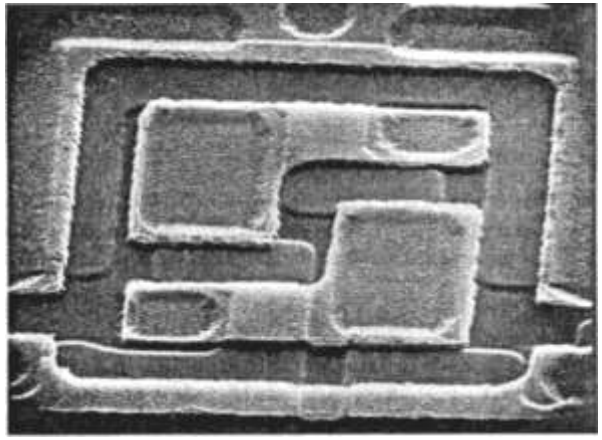
– Alu-Leiterzug

Dünnes Gateoxid

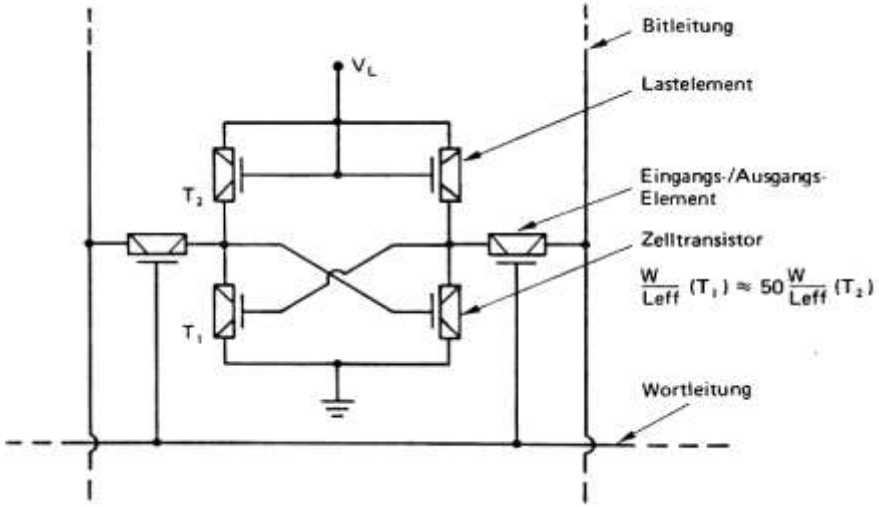
– n^+ – Diffusion

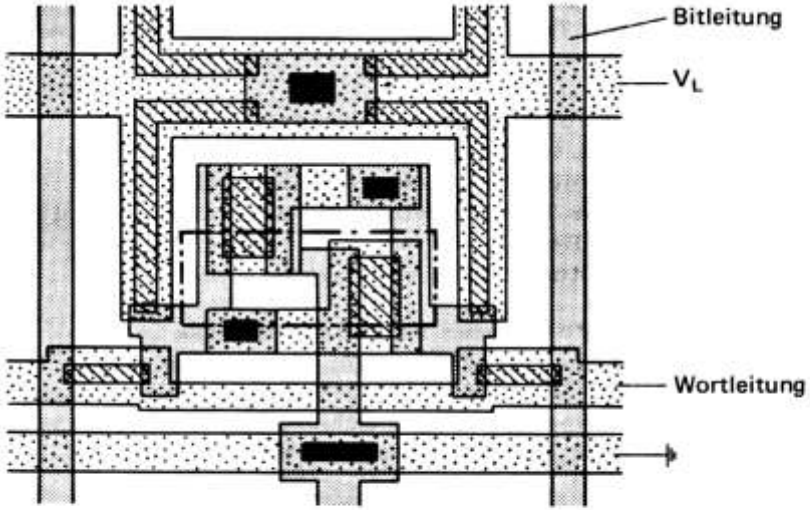
Kontaktloch

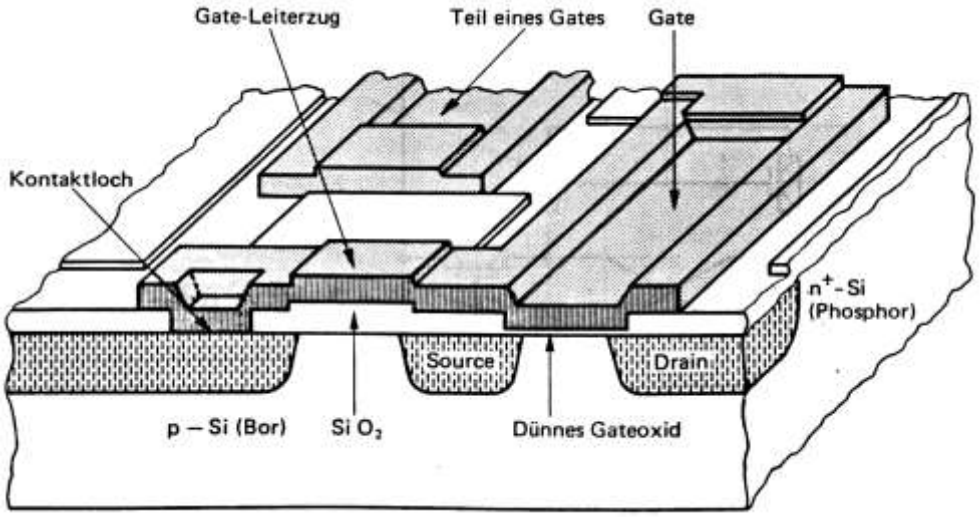
Ausschnitt, dargestellt in 41 c

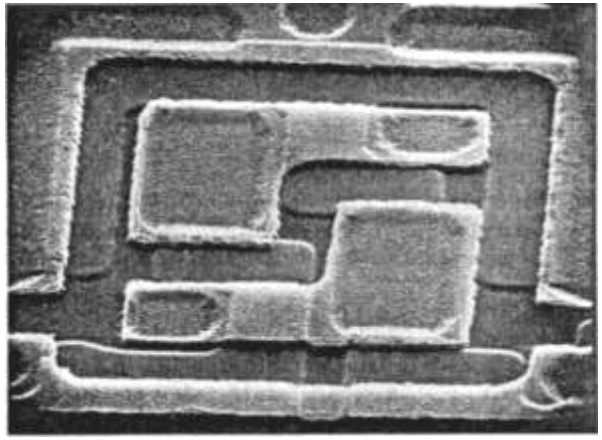


The process flow

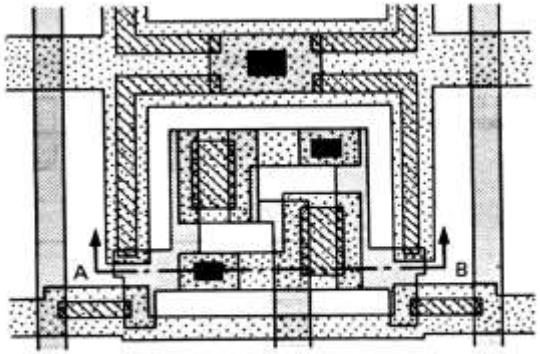






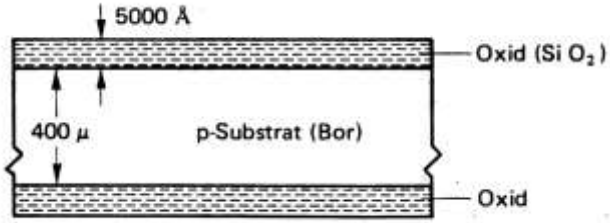


Prozeßschritt

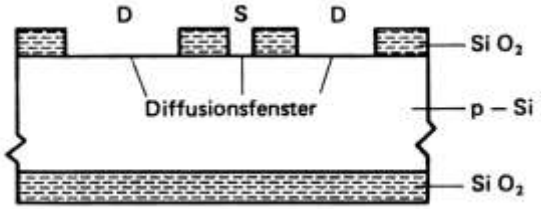


Die folgenden Querschnitte sind
Schnitte AB durch die Speicherzelle

1. Oxydation

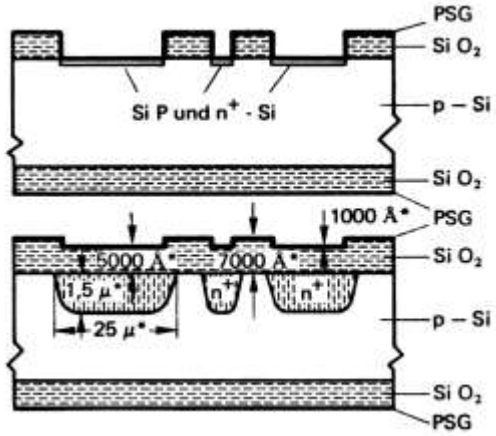


Photoprozeß (Maske 1)
Source-Drain-Diffusionsmaske

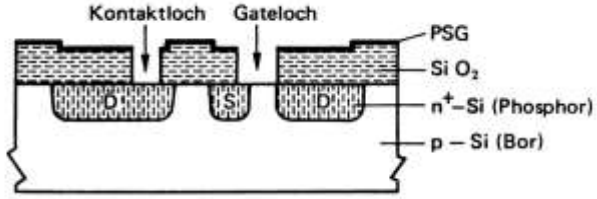


Reinigung
Source-Drain-Diffusion
a) Belegung ($POCl_3$ - Quelle)

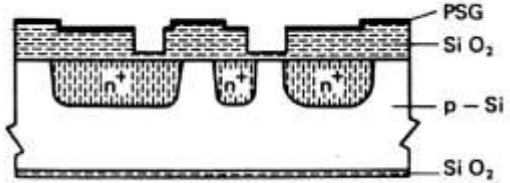
b) Eindiffusion und
Reoxidation



Photoprozeß (Maske 2)
Gate- und Kontaktlochmaske

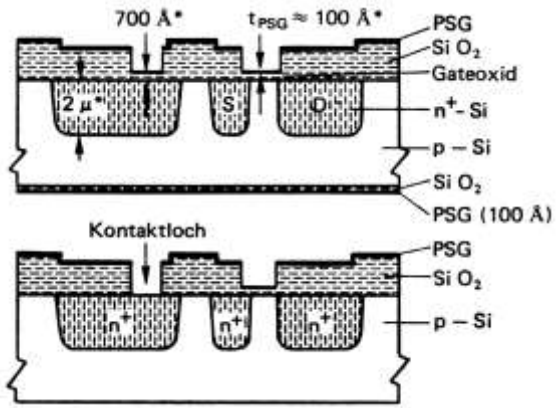


Reinigung
Gateoxydation



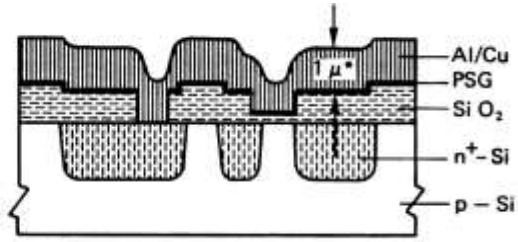
BEOL:

Stabilisierung des Gateoxids mit PSG
a) Belegung ($POCl_3$-Quelle)
b) Eindiffusion und Temperung



Photoprozeß (Maske 3)
Kontaktlochmaske

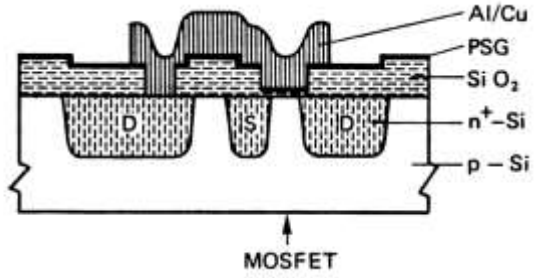
„Back door"-Ätzung
Al/Cu-Bedampfung



Photoprozeß (Maske 4)
„Alu-sub-etch"-Maske

Temperung nach Aluminium

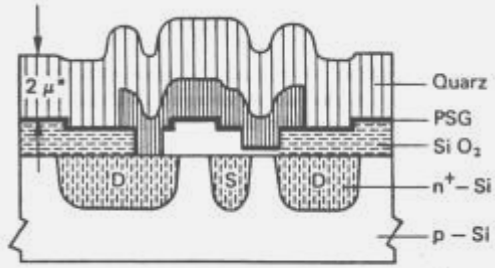
Elektrischer Test
(In Line Test post Aluminum, *Post Aluminium Probe*, PAP)



Quarz Aufstäuben (Sputtern)

Quarz Temperung

Photoprozeß (Maske 5)
Maske für Kontaktlöcher im Quarz

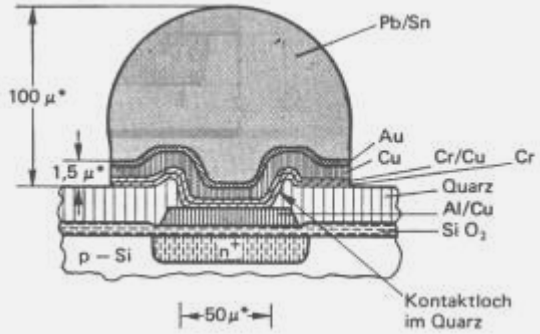


Chrom-Kupfer-Gold-Bedampfung

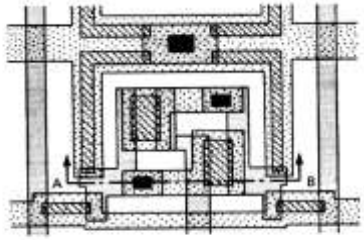
Blei/Zinn-Bedampfung

Pad Reflow

In Line Test post Pad Reflow



Prozeßschritt



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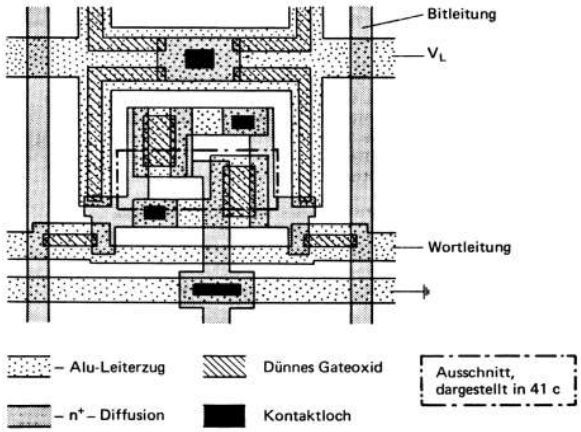
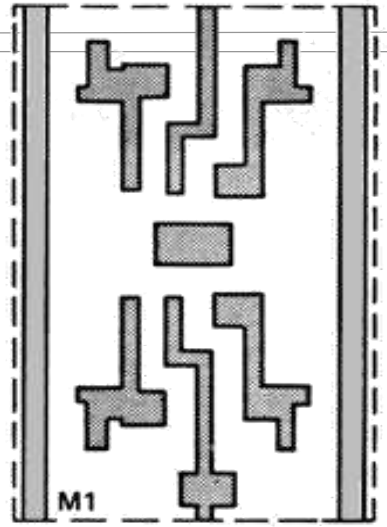
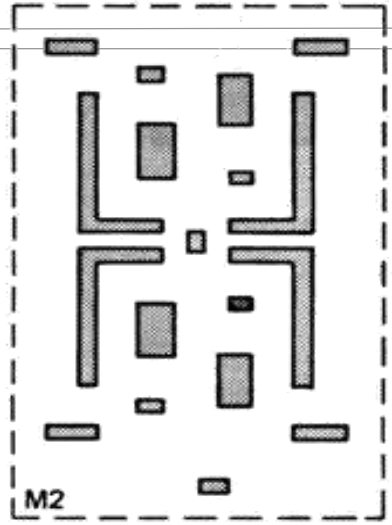
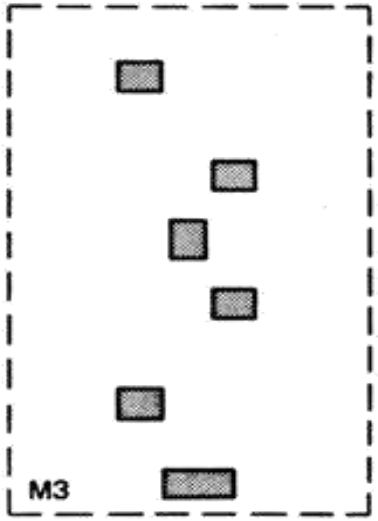
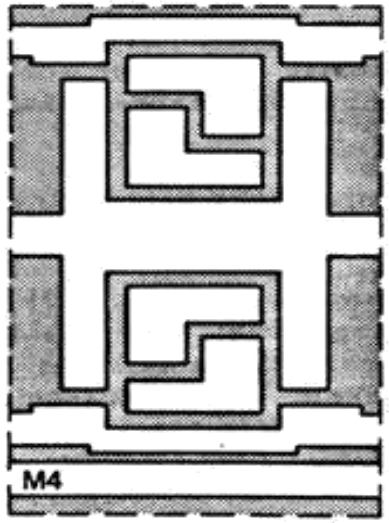

Bitleitung
V_L
Wortleitung
– Alu-Leiterzug
Dünnes Gateoxid
Ausschnitt, dargestellt in 41 c
– n⁺ – Diffusion
Kontaktloch


M1


M2


M3


M4

Prozess - Integration

Metal Gate N-MOS Enhancement Process:

☺ simple (only 4 Mask Levels)
☺ conductor level in the substrate (through n^+ region)

Prozess - Integration

Metal Gate N-MOS Enhancement Process:

☺ simple (only 4 Mask Levels)
☺ conductor level in the substrate (through n^+ region)

☹ requires much space
☹ limitations of the transfer curve
☹ slow

Prozess - Integration

Metal Gate N-MOS Enhancement Process:

☺ simple (only 4 Mask Levels)
☺ conductor level in the substrate (through n^+ region)

☹ requires much space
☹ limitations of the transfer curve
☹ slow

Continue "SCT_SS20_08.04" 36:10 VIDEO CAMPUS SACHSEN

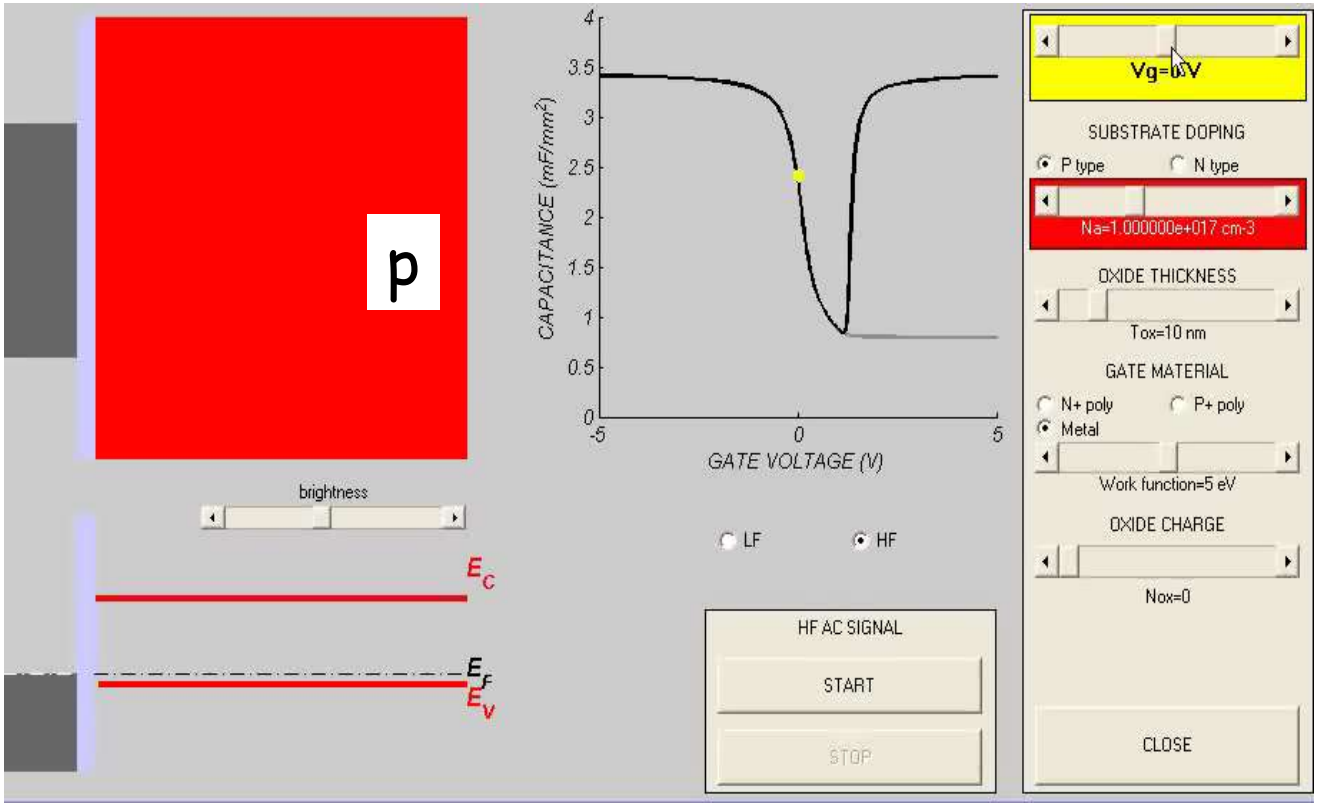
The threshold voltage

2.4 The threshold voltage at MOSFET

Parameters to turn knobs:

- Oxide Thickness
- Substrate Doping
- Oxide Charges
- Work function difference
- Substrate Bias

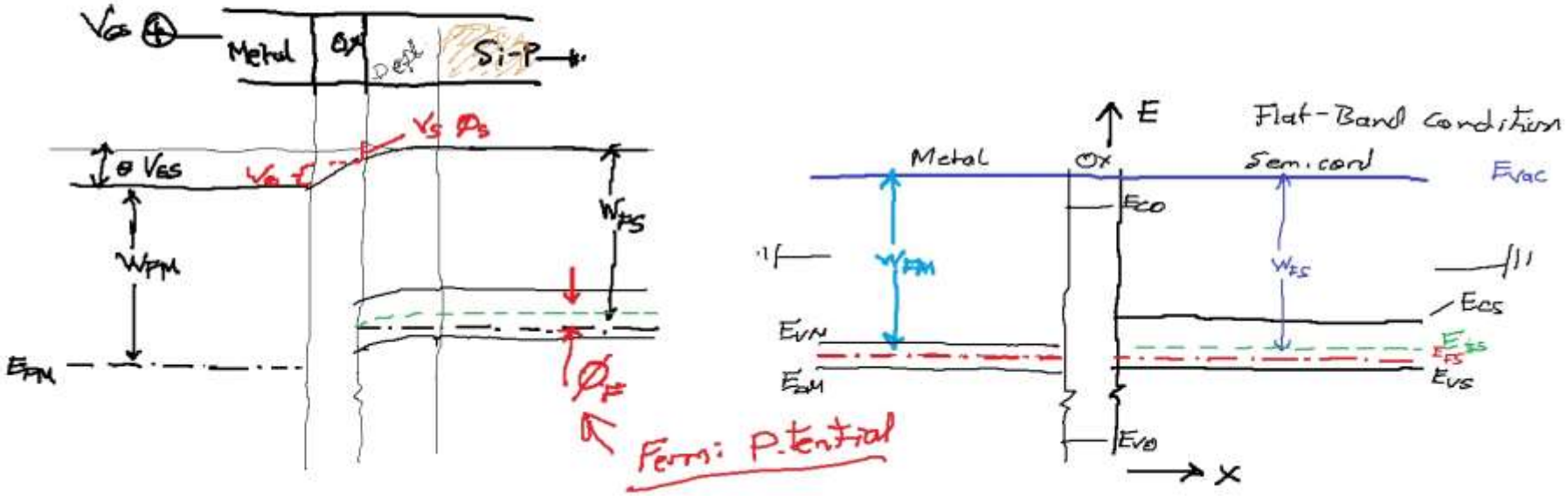
Meaning of the Threshold Voltage V_T



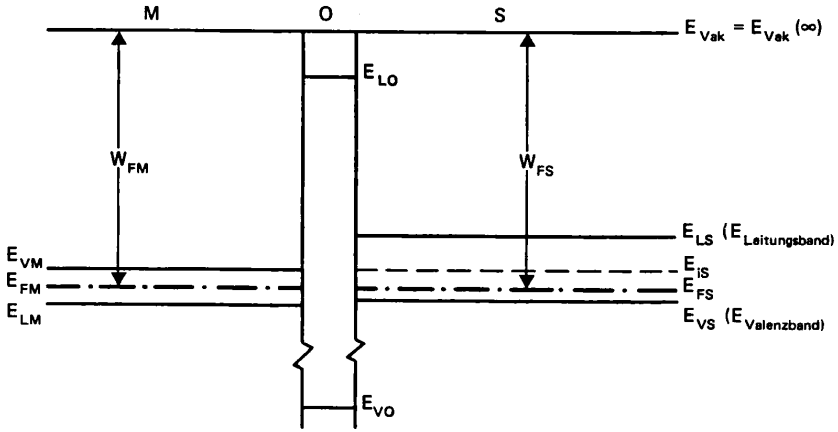
Terms:
- accumulation
- depletion
- inversion

Try also pdf file "MOScapAnim" in OPAL folder

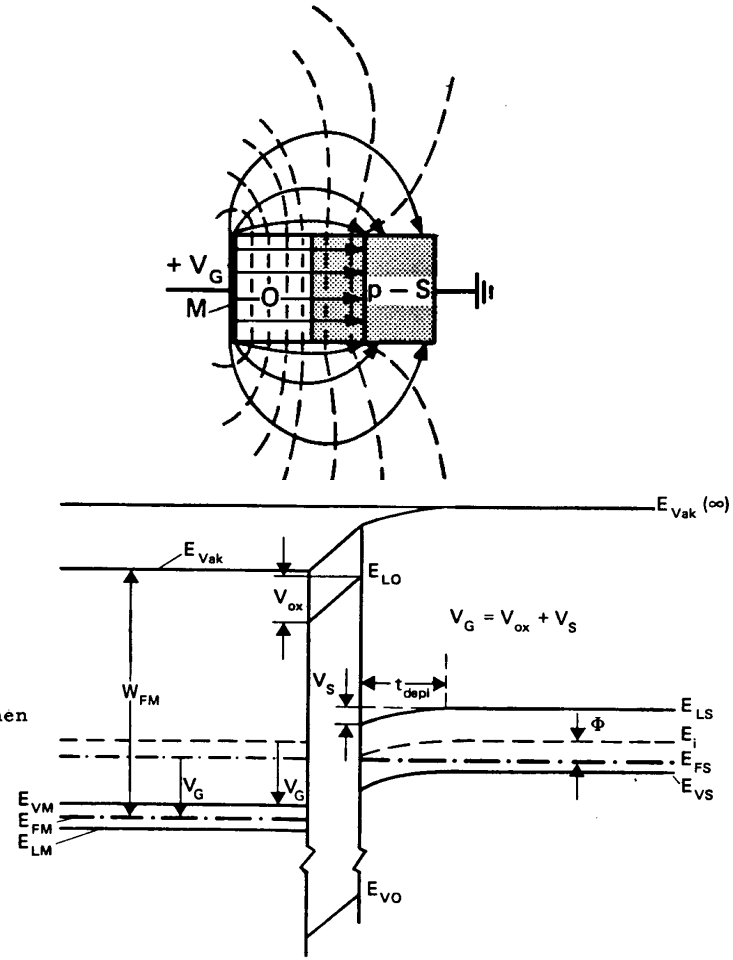
Blackboard 8.1



Situation at band diagrams

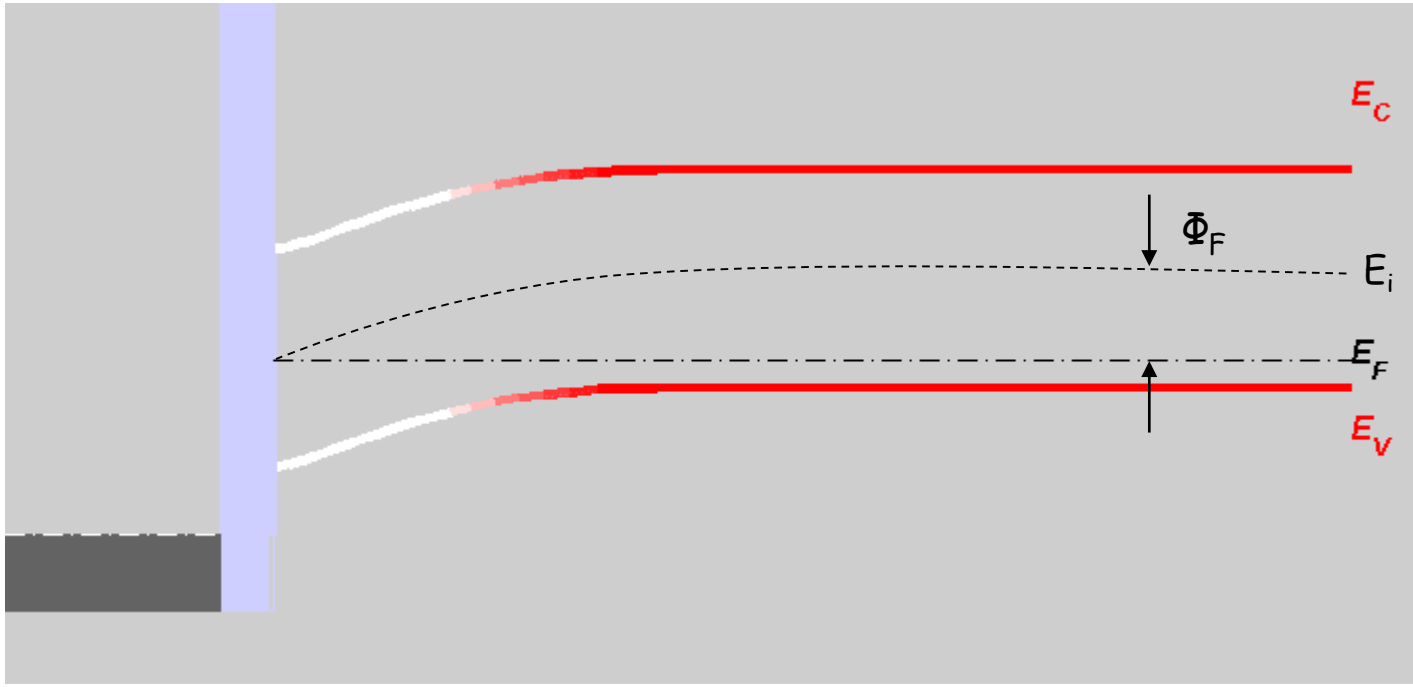


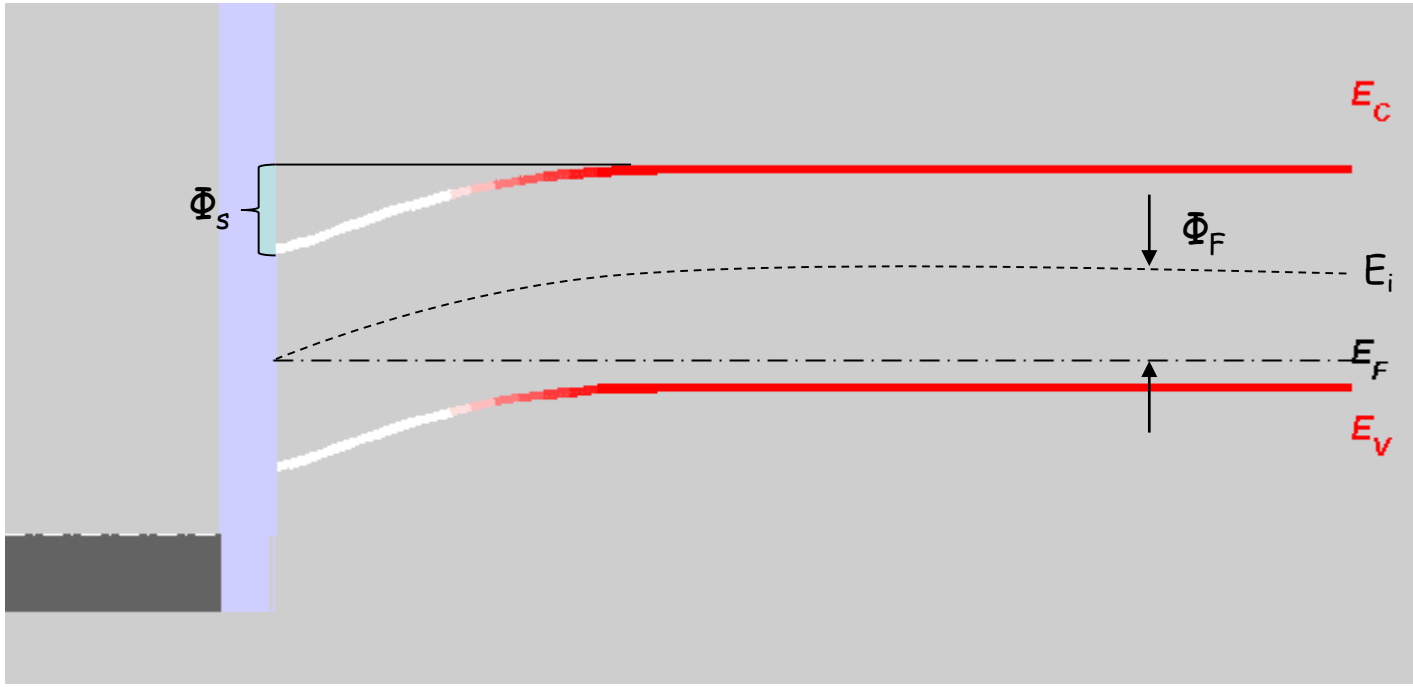
Bändermodell einer idealisierten MOS-Struktur im thermodynamischen Gleichgewicht

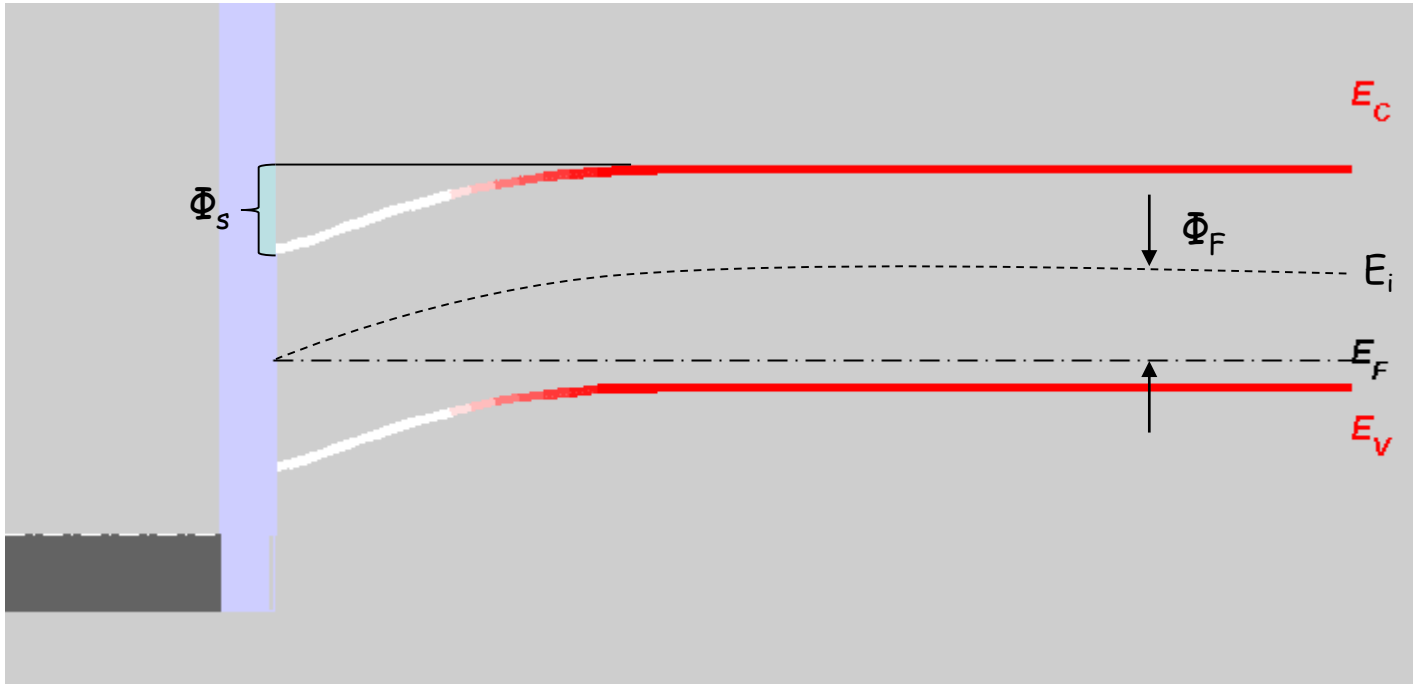


Idealisierte MOS-Struktur bei $0 < V_G < V_T$

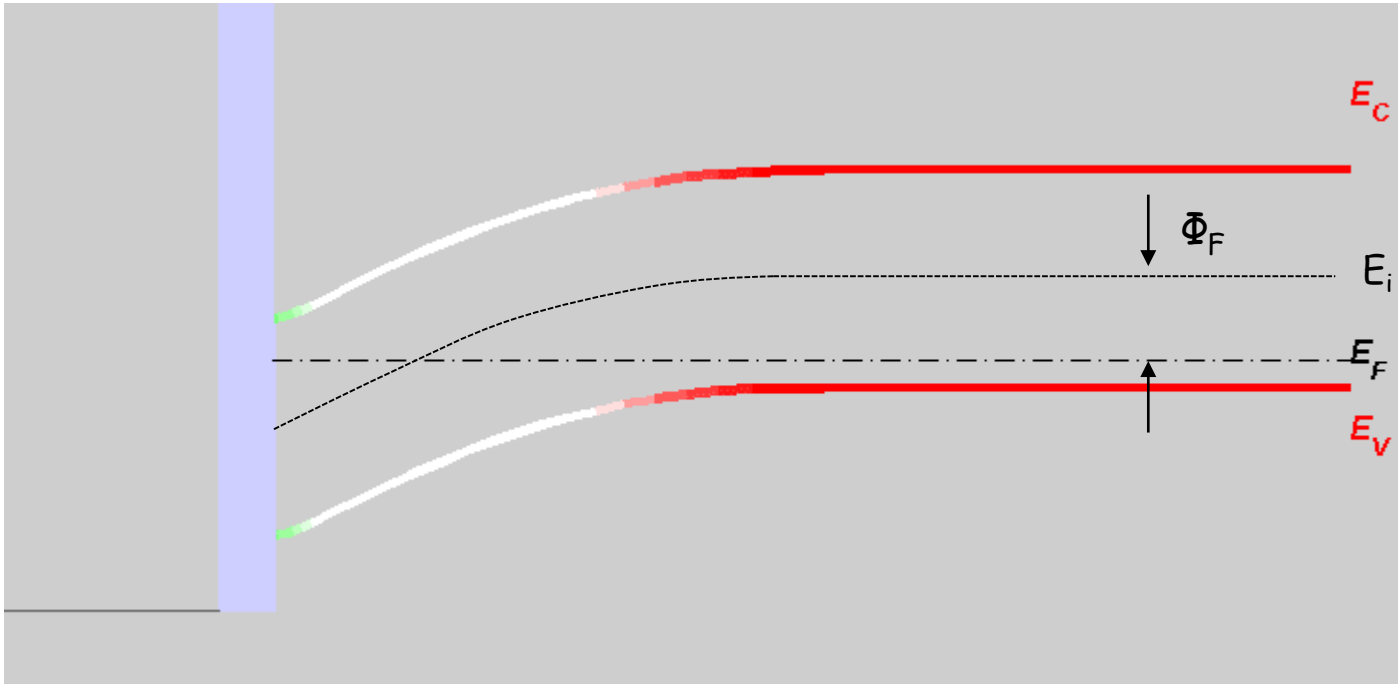

E_C
Φ_F
E_i
E_F
E_V

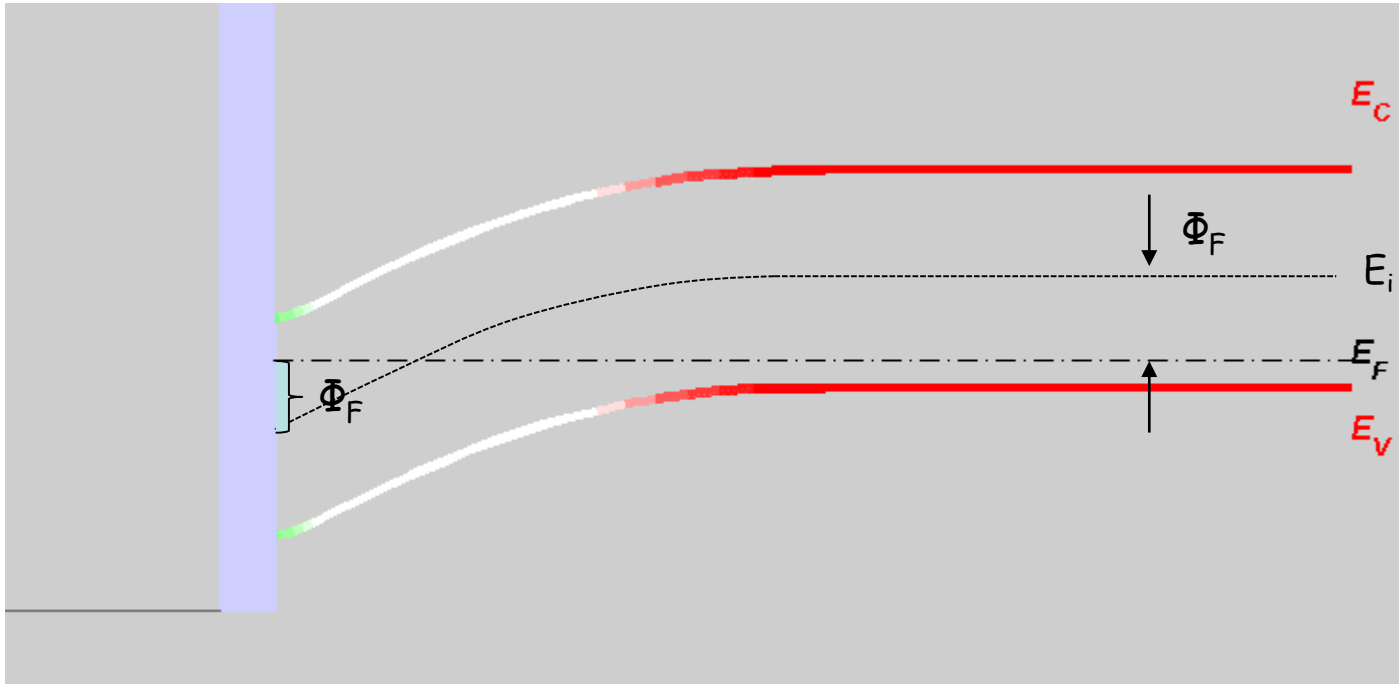

E_C
Φ_F
E_i
E_F
E_V

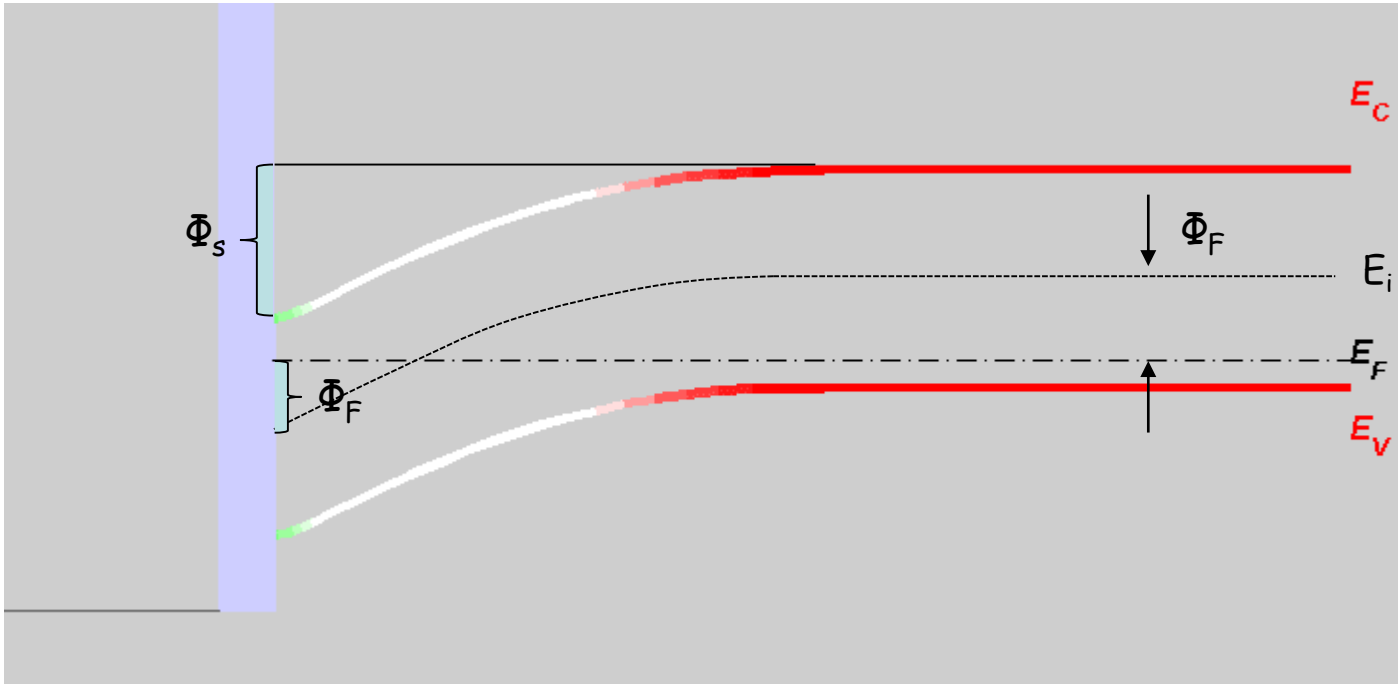

E_C
Φ_s
Φ_F
E_i
E_F
E_V

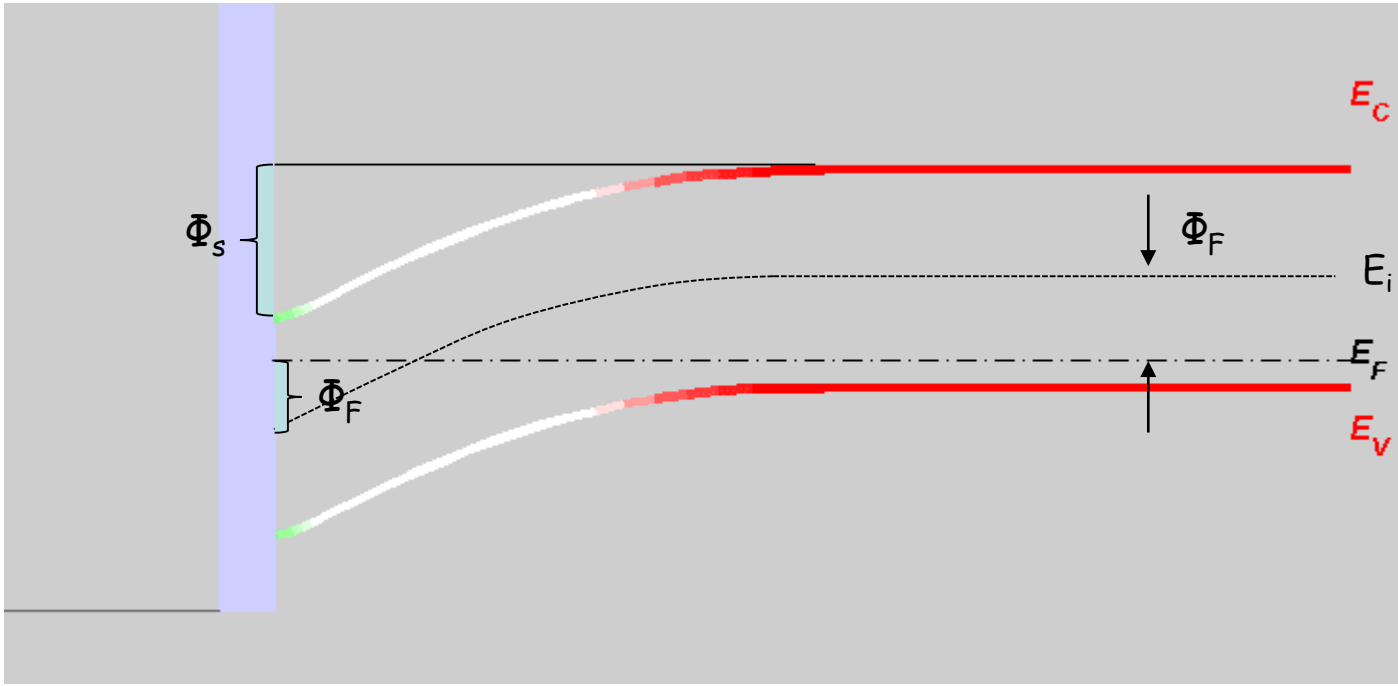


$$\Phi_s = \Phi_F$$


E_C
Φ_F
E_i
E_F
E_V

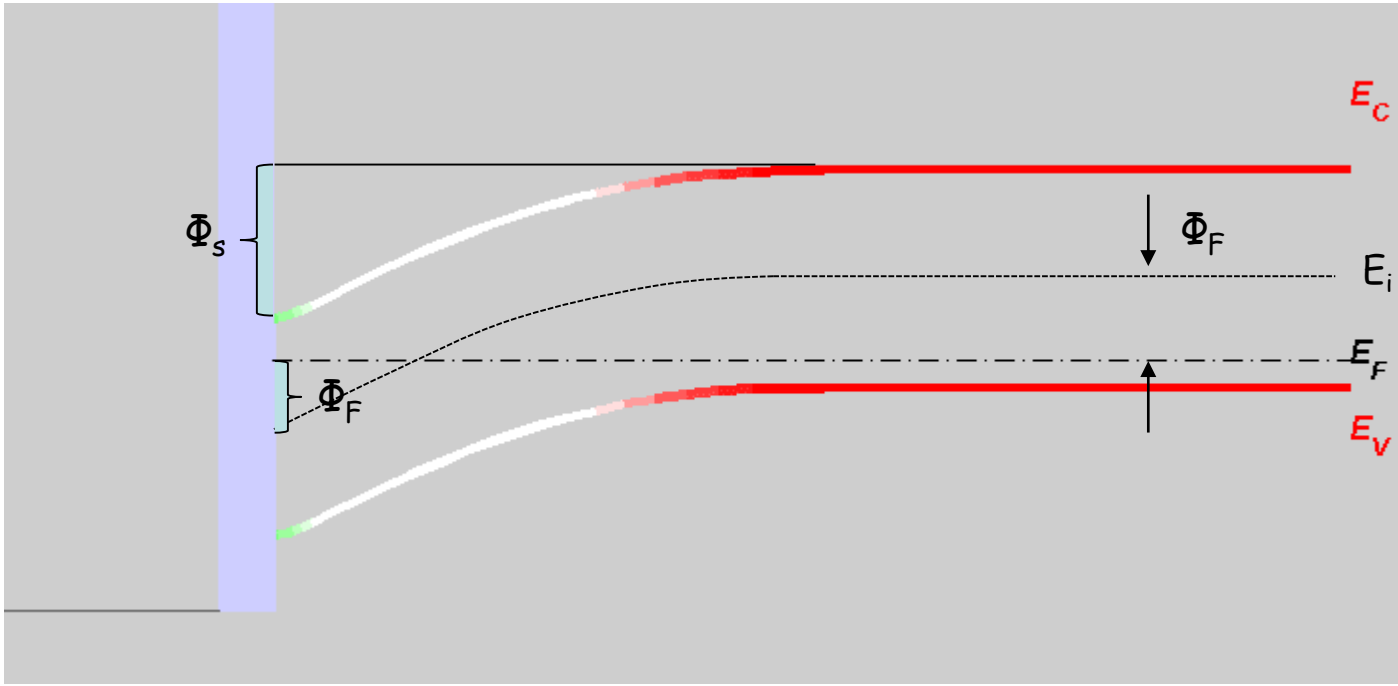

E_C
Φ_F
E_i
E_F
Φ_F
E_V


E_C
Φ_s
Φ_F
E_i
E_F
Φ_F
E_V



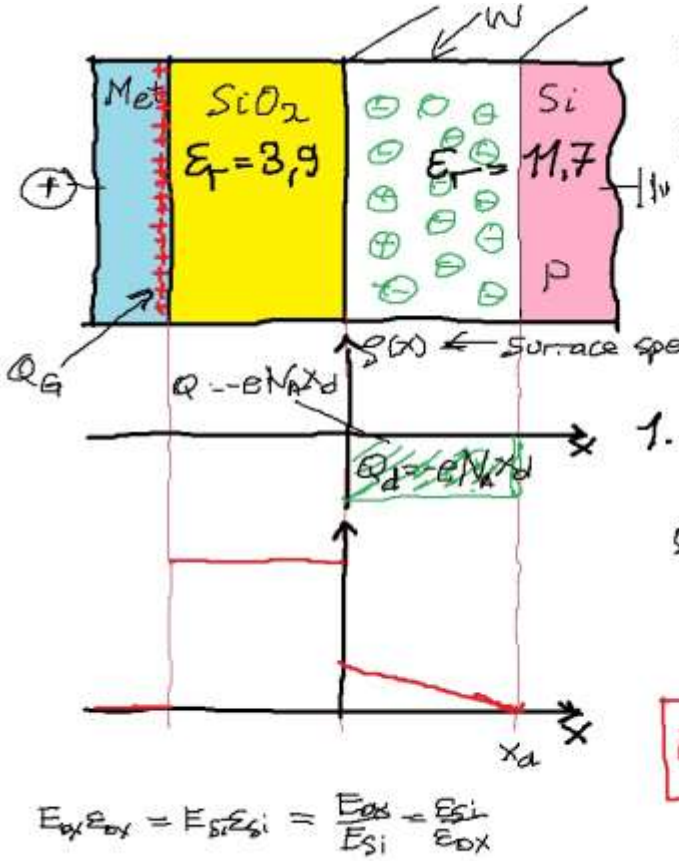
$\Phi_s = 2\Phi_F$:Strong inversion or threshold V_t

Derivation of V_t



$\Phi_s = 2\Phi_F$:Strong inversion or threshold V_t

Blackboard 8.2



Relation between El.potential Φ in V and carrier density ϱ →
Poisson Equation

$$\frac{\partial^2 \Phi}{\partial x^2} = -\frac{\varrho}{\varepsilon}$$ consists of 2 parts:

$$\frac{\partial E}{\partial x} = \frac{\varrho}{\varepsilon} \quad \text{and} \quad \frac{\partial \Phi}{\partial x} = -E$$

1. Integration

$$E \text{ in } \frac{V}{m} = \int \frac{\varrho}{\varepsilon} dx$$

Boundary Cond.
$E(x_d) = 0$

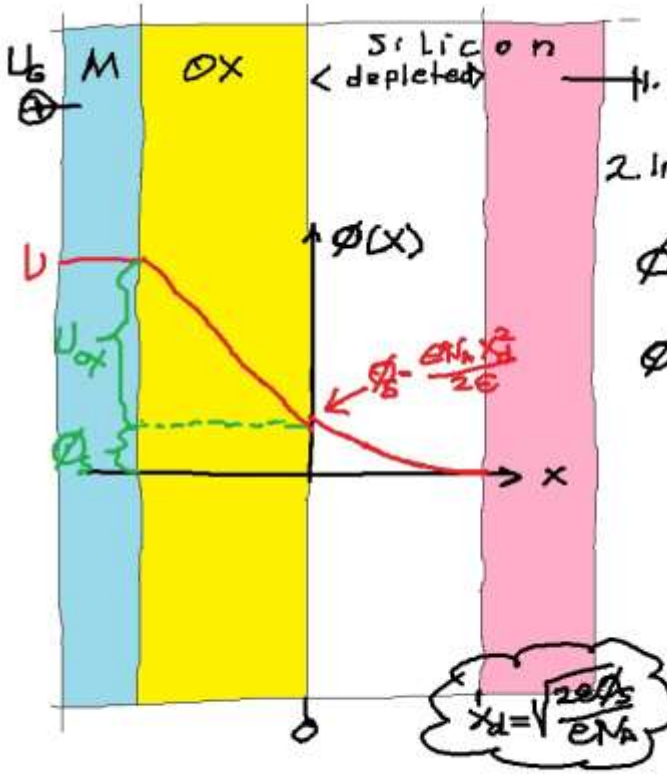
$\varrho = -eN_A$ $\quad E_{Si}(x) = E_{Si}(0) - \frac{eN_A}{\varepsilon} x$

$$E_{Si}(0) = \frac{eN_A}{\varepsilon} x_d$$

$$E_{Si}(x) = \frac{eN_A}{\varepsilon}(x_d - x)$$

$$E_{ox}\varepsilon_{ox} = E_{Si}\varepsilon_{Si} = \frac{E_{ox}}{E_{Si}} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}}$$

Blackoard 8.3



$$E_{Si}(x) = \frac{eN_A}{\varepsilon}(x_d - x)$$

2. Integration delivers ϕ in V $= \int -E\,dx$

$$\phi(x) = -\frac{eN_A}{\varepsilon}\left(x_d x - \frac{1}{2}x^2\right) + \phi_0$$

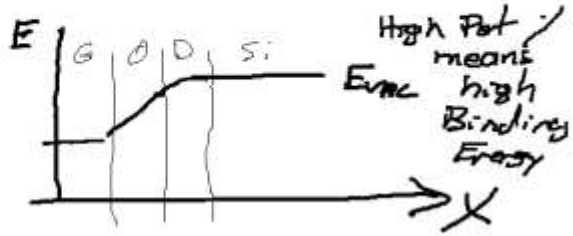
Boundary condition $\phi(x_d) = \Theta$

$$\phi_0 = \frac{eN_A}{\varepsilon}\frac{1}{2}x_d^2 = \phi_s$$

$$\phi(x) = -\frac{eN_A}{\varepsilon}\left(-\frac{1}{2}x_d^2 + x_d x - \frac{1}{2}x^2\right)$$

$$\phi(x) = \frac{eN_A}{2\varepsilon}\left(x_d^2 - 2x_d x + x^2\right) = \frac{eN_A x_d^2}{2\varepsilon}\left(1 - 2\frac{x}{x_d} + \frac{x^2}{x_d^2}\right)$$

$$\phi(x) = \frac{eN_A x_d^2}{2\varepsilon}\left(1 - \frac{x}{x_d}\right)^2$$



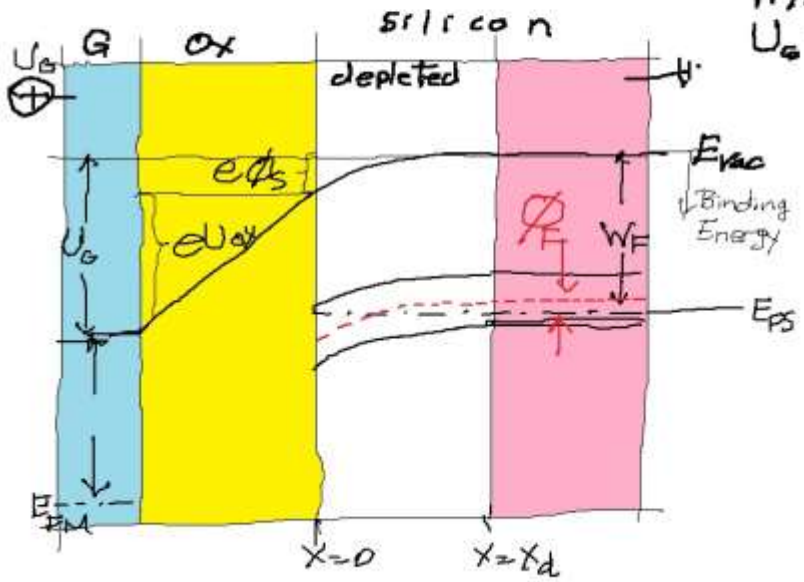
Blackboard 8.4

$$Q_G = (U_G - \phi_S) C_{ox} = -Q_d$$

$$Q_d = -eN_A \cdot x_d = -eN_A \sqrt{\frac{2\varepsilon\phi_S}{eN_A}}$$

$$Q_d = -\sqrt{2eN_A\varepsilon \cdot \phi_S}$$

Threshold voltage condition:
$U_G = U_T$ when $\phi_S = 2\phi_F$



$$-Q_{d\max} = \sqrt{2eN_A\varepsilon(2\phi_F)} = (U_G - \phi_S) C_{ox}$$

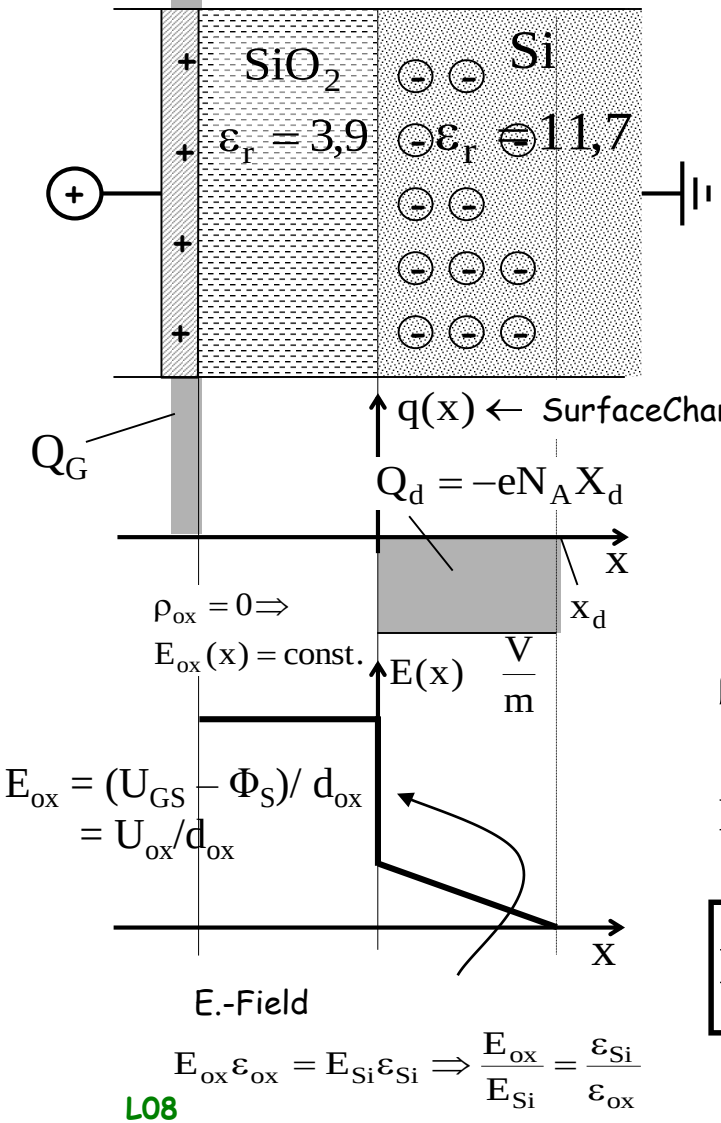
$U_G = U_T$; $\phi = 2\phi_F$

solve for U_T

$$U_T = \frac{1}{C_{ox}} \sqrt{2eN_A\varepsilon(2\phi_F)} + 2\phi_F$$

$C_{ox} = \frac{\varepsilon}{d_{ox}}$ surface specific capacity

Threshold voltage at MOS-FET /1
Idealized!



Relation between El. Potential $\Phi(V)$ and carrier density $\rho \rightarrow$ Poisson equation

$$\frac{\partial^2\Phi}{\partial x^2} = -\frac{\rho}{\varepsilon}$$ Consist of 2 parts:

$$\frac{\partial E}{\partial x} = \frac{\rho}{\varepsilon} \quad \text{und} \quad \frac{\partial\Phi}{\partial x} = -E$$

1. Integration delivers $E\left(\frac{V}{m}\right) = \int \frac{\rho}{\varepsilon}\,dx$

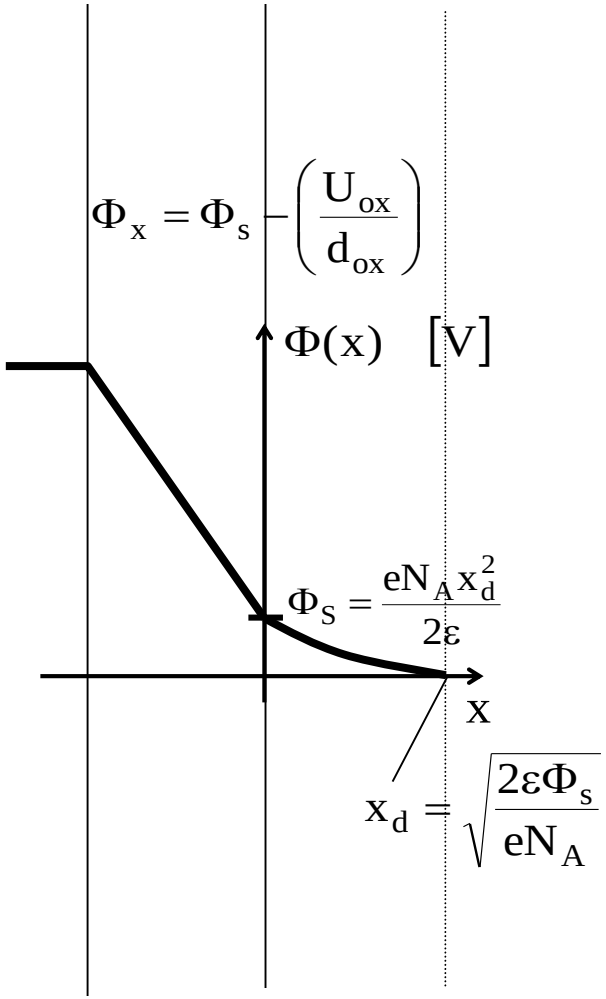
$$\rho = -eN_A \qquad E_{Si}(x) = E_{SI}(0) - \frac{eN_A}{\varepsilon}x$$

Boundary cond. $E(x_d) = 0$

$$E_{Si}(0) = \frac{eN_A}{\varepsilon}x_d$$

$$\boxed{E_{Si}(x) = \frac{eN_A}{\varepsilon}(x_d - x)\Rightarrow} \qquad E_{Si} = \frac{eN_A x_d}{\varepsilon}\left(1 - \frac{x}{x_d}\right)$$

Threshold voltage at MOS-FET /2



2.Integration delivers $\Phi(V) = \int -E dx$

$$\Phi(x) = -\frac{eN_A}{\varepsilon}\left(x_d x - \tfrac{1}{2}x^2\right) + \Phi_0$$

Boundary cond.

$$\Phi(x_d) = 0$$

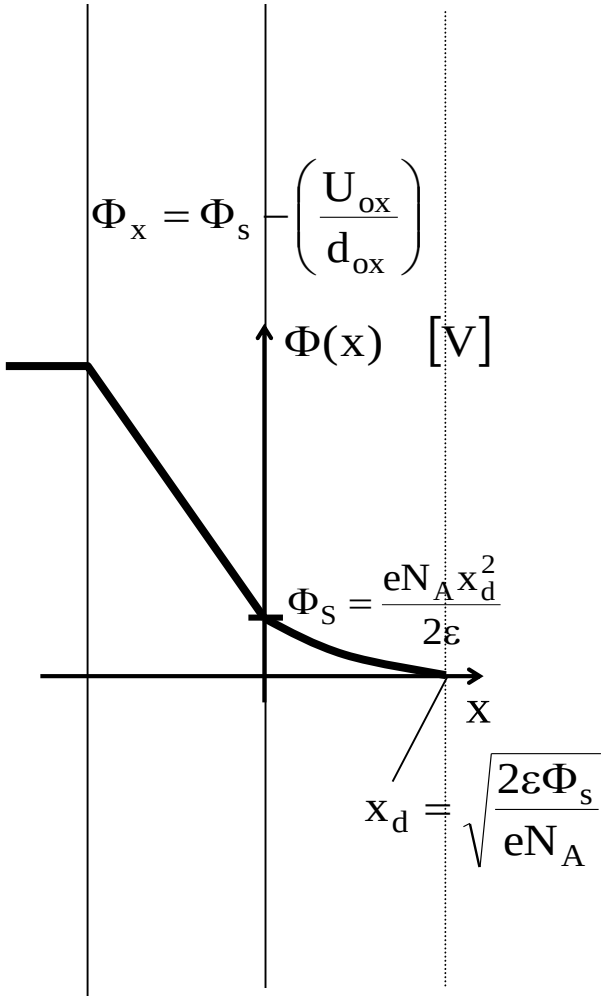
$$\Phi_0 = \frac{eN_A}{\varepsilon}\tfrac{1}{2}x_d^2$$

$$\Phi(x) = -\frac{eN_A}{\varepsilon}\left(-\tfrac{1}{2}x_d^2 + x_d x - \tfrac{1}{2}x^2\right)$$

$$\frac{eN_A}{2\varepsilon}\left(x_d^2 - 2xx_d + x^2\right) = \frac{eN_A x_d^2}{2\varepsilon}\left(1 - 2\frac{x}{x_d} + x_d^2\right)$$

$$\Phi(x) = \frac{eN_A x_d^2}{2\varepsilon}\left(1 - \frac{x}{x_d}\right)^2$$

Threshold voltage at MOS-FET /2



2.Integration delivers $\Phi(V) = \int -E dx$

$$\Phi(x) = -\frac{eN_A}{\varepsilon}\left(x_d x - \tfrac{1}{2}x^2\right) + \Phi_0$$

Boundary cond.

$$\Phi(x_d) = 0$$

$$\Phi_0 = \frac{eN_A}{\varepsilon}\tfrac{1}{2}x_d^2$$

$$\Phi(x) = -\frac{eN_A}{\varepsilon}\left(-\tfrac{1}{2}x_d^2 + x_d x - \tfrac{1}{2}x^2\right)$$

$$\frac{eN_A}{2\varepsilon}\left(x_d^2 - 2xx_d + x^2\right) = \frac{eN_A x_d^2}{2\varepsilon}\left(1 - 2\frac{x}{x_d} + x_d^2\right)$$

$$\Phi(x) = \frac{eN_A x_d^2}{2\varepsilon}\left(1 - \frac{x}{x_d}\right)^2$$

! High potential means high binding energy !

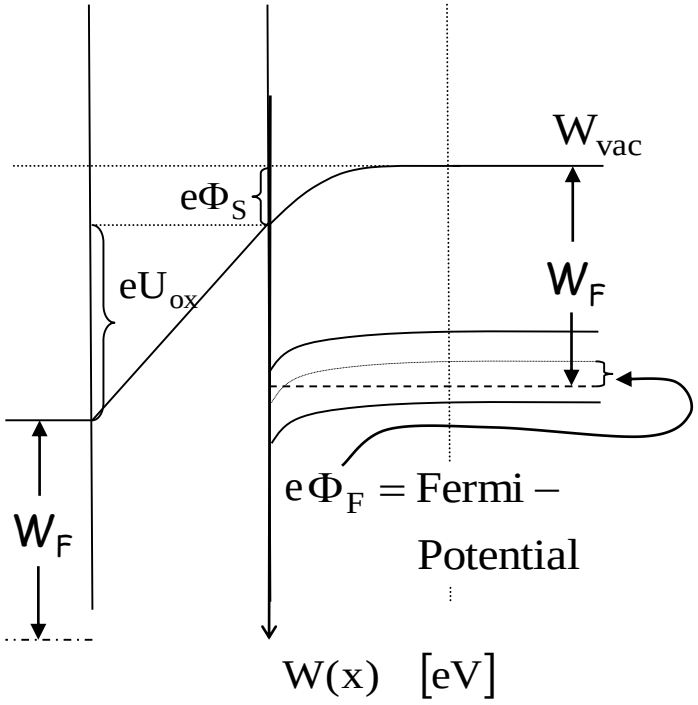
Threshold voltage at MOS-FET /3

$$Q_G = (U_{GS} - \Phi_S) C_{ox} = -Q_d$$

$$Q_d = -eN_A \cdot x_d = -eN_A \sqrt{\frac{2\varepsilon \Phi s}{eN_A}}$$

$$Q_d = -\sqrt{2eN_A \varepsilon \cdot \Phi_S}$$

Condition for threshold: $U_{GS}=U_T$ when



Threshold voltage at MOS-FET /3

$$Q_G = (U_{GS} - \Phi_S) C_{ox} = -Q_d$$

$$Q_d = -eN_A \cdot x_d = -eN_A \sqrt{\frac{2\varepsilon \Phi s}{eN_A}}$$

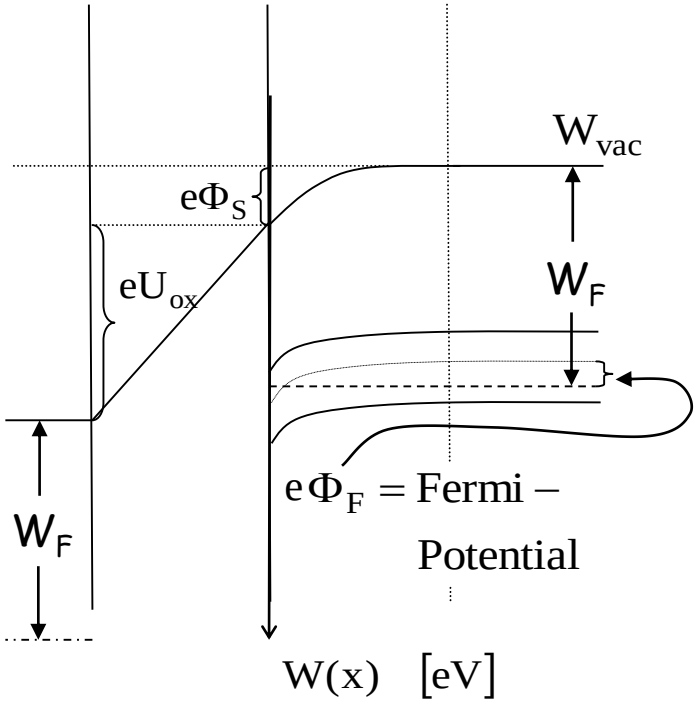
$$Q_d = -\sqrt{2eN_A \varepsilon \cdot \Phi_S}$$

Condition for threshold: $U_{GS}=U_T$ when $\Phi_S = 2\Phi_F$

$$-Q_{d_{max}} = \sqrt{2eN_A \varepsilon (2\Phi_F)} = (U_{GS} - \Phi_S) C_{ox}$$

$U_{GS} \equiv U_T$

$\Phi_S = 2\Phi_F$



Threshold voltage at MOS-FET /3

$$Q_G = (U_{GS} - \Phi_S) C_{ox} = -Q_d$$

$$Q_d = -eN_A \cdot x_d = -eN_A \sqrt{\frac{2\varepsilon \Phi s}{eN_A}}$$

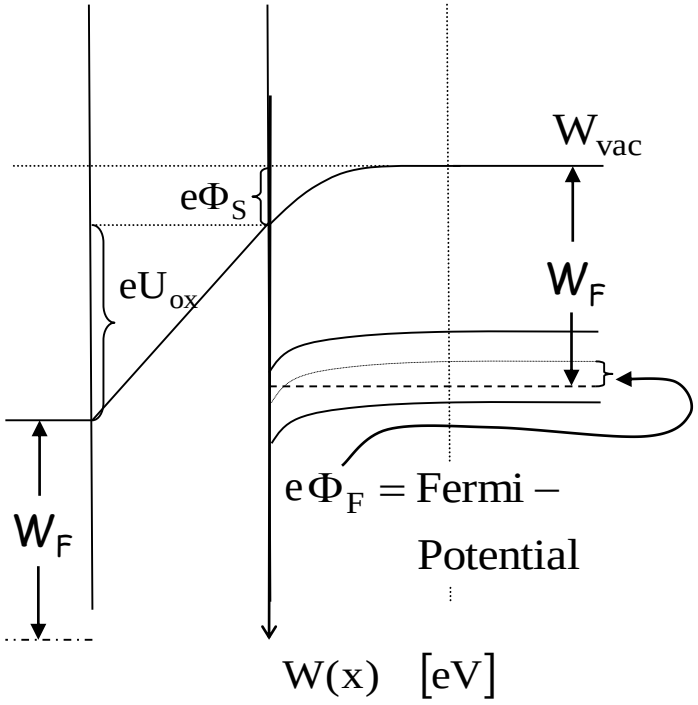
$$Q_d = -\sqrt{2eN_A \varepsilon \cdot \Phi_S}$$

Condition for threshold: $U_{GS}=U_T$ when $\Phi_S = 2\Phi_F$

$$-Q_{d_{max}} = \sqrt{2eN_A \varepsilon (2\Phi_F)} = (U_{GS} - \Phi_S) C_{ox}$$

$U_{GS} \equiv U_T$

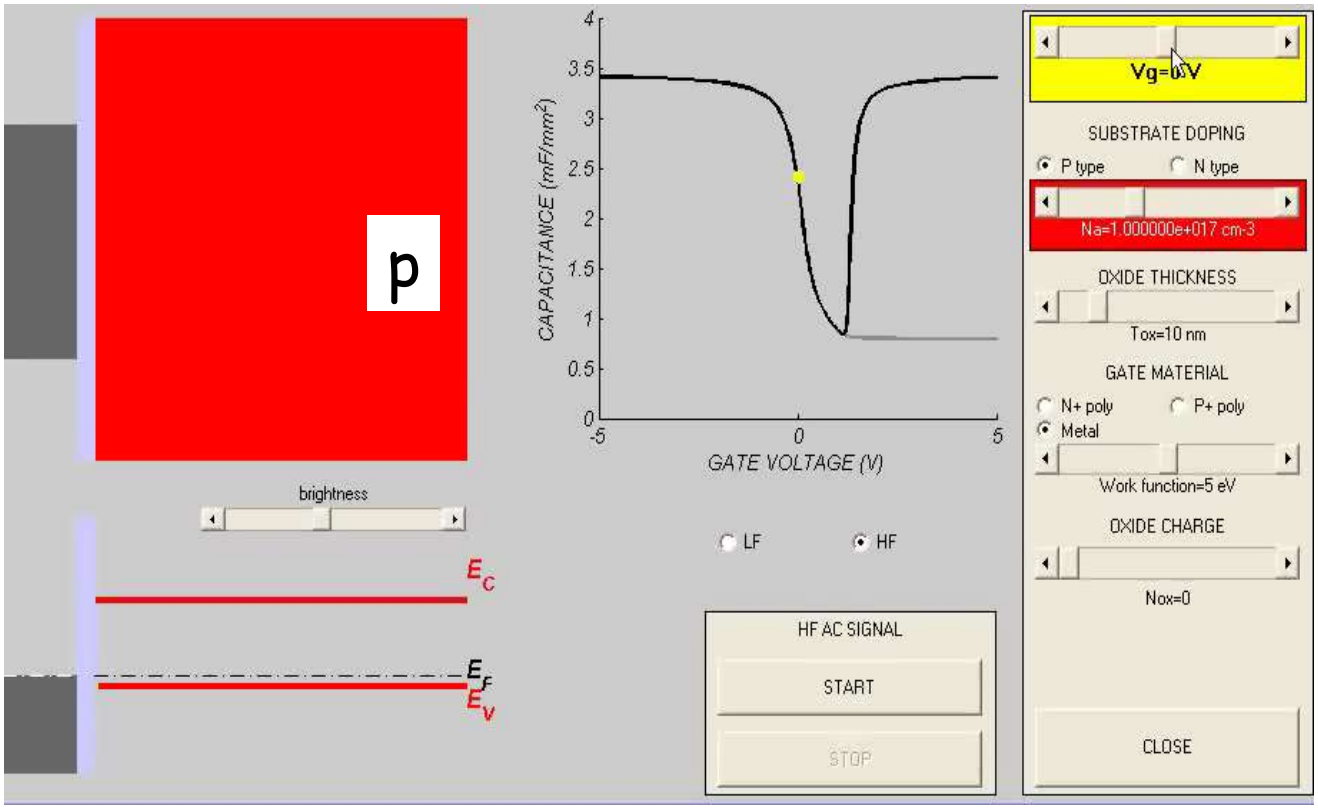
$\Phi_S = 2\Phi_F$



$$U_T = \frac{1}{C_{ox}} \sqrt{2eN_A \varepsilon (2\Phi_F)} + 2\Phi_F$$

C_{ox} is the surface specific capacity = ε/d_{ox}

Demonstration: $V_T = f(d_{ox}$ und $N_A)$



Try also pdf file "MOScapAnim" in OPAL folder

»Wissen schafft Brücken.«