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select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 – Process Integration

9. Web-based virtual Lecture: June 17 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here 

"SCT_SS20_09.1" 12:57

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TECHNISCHE UNIVERSITÄT DRESDEN

Outline

Review:
- SCT Basics
- MOS Capacitor
- MOS-Cap-CV
- MOS-FET

  Triode- Saturation-
  Subthreshold range
- Al-Gate FET
- SRAM production
- V_T dependencies

Today: E/D Logic

SC-Basics

http://www.computerhistory.org/siliconengine/timeline/

Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transistors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

Review:

- SCT Basics
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- MOS-Cap-CV
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  Triode- Saturation-
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Today: E/D Logic

Continue

"SCT_SS20_09.2" 06:43

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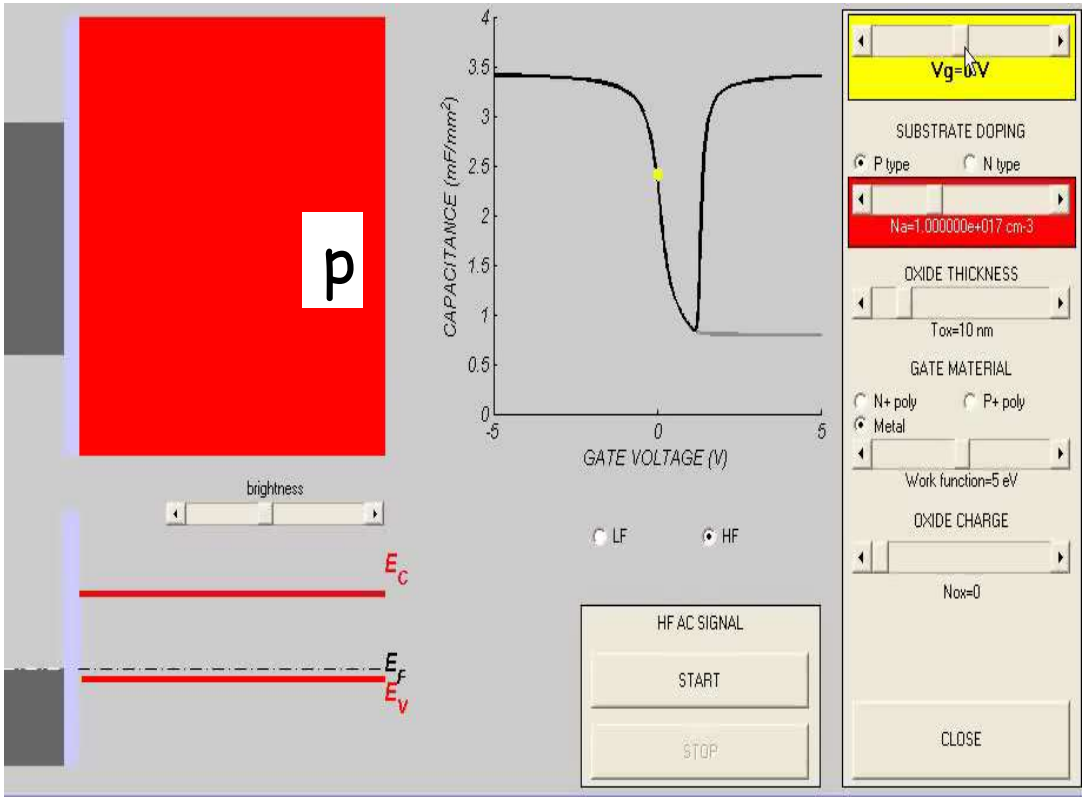
http://www.computerhistory.org/siliconengine/timeline/

Demonstration: $V_T = f(d_{ox}$ und $N_A)$



$$Q_G = (U_{GS} - \Phi_S)C_{ox} = -Q_d$$

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Einsatzspannung $U_{GS}=U_T$ wenn $\Phi_S = 2\Phi_F$

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$\Phi_S = 2\Phi_F$

$$U_T = \frac{1}{C_{ox}}\sqrt{2eN_A\varepsilon(2\Phi_F)} + 2\Phi_F$$

Please check also pdf file "MOScapAnim" at the OPAL folder

Demonstration: $V_T = f(d_{ox}$ und $N_A)$

Continue

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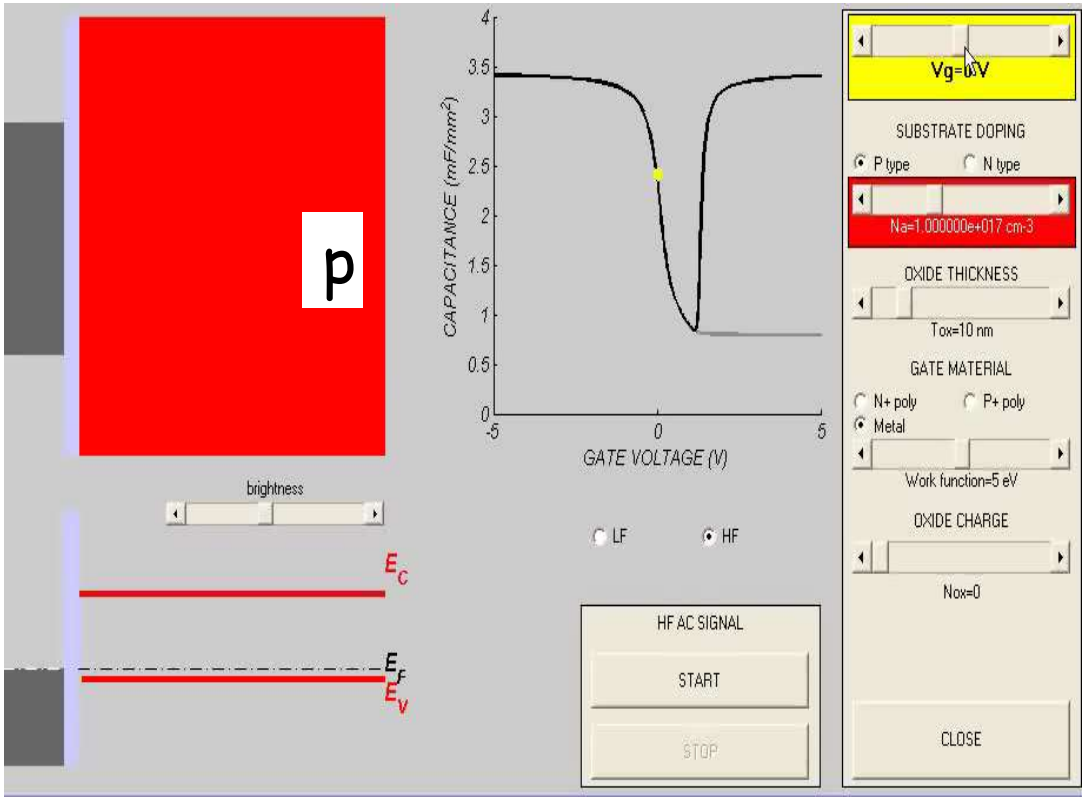
From ideal to real conditions



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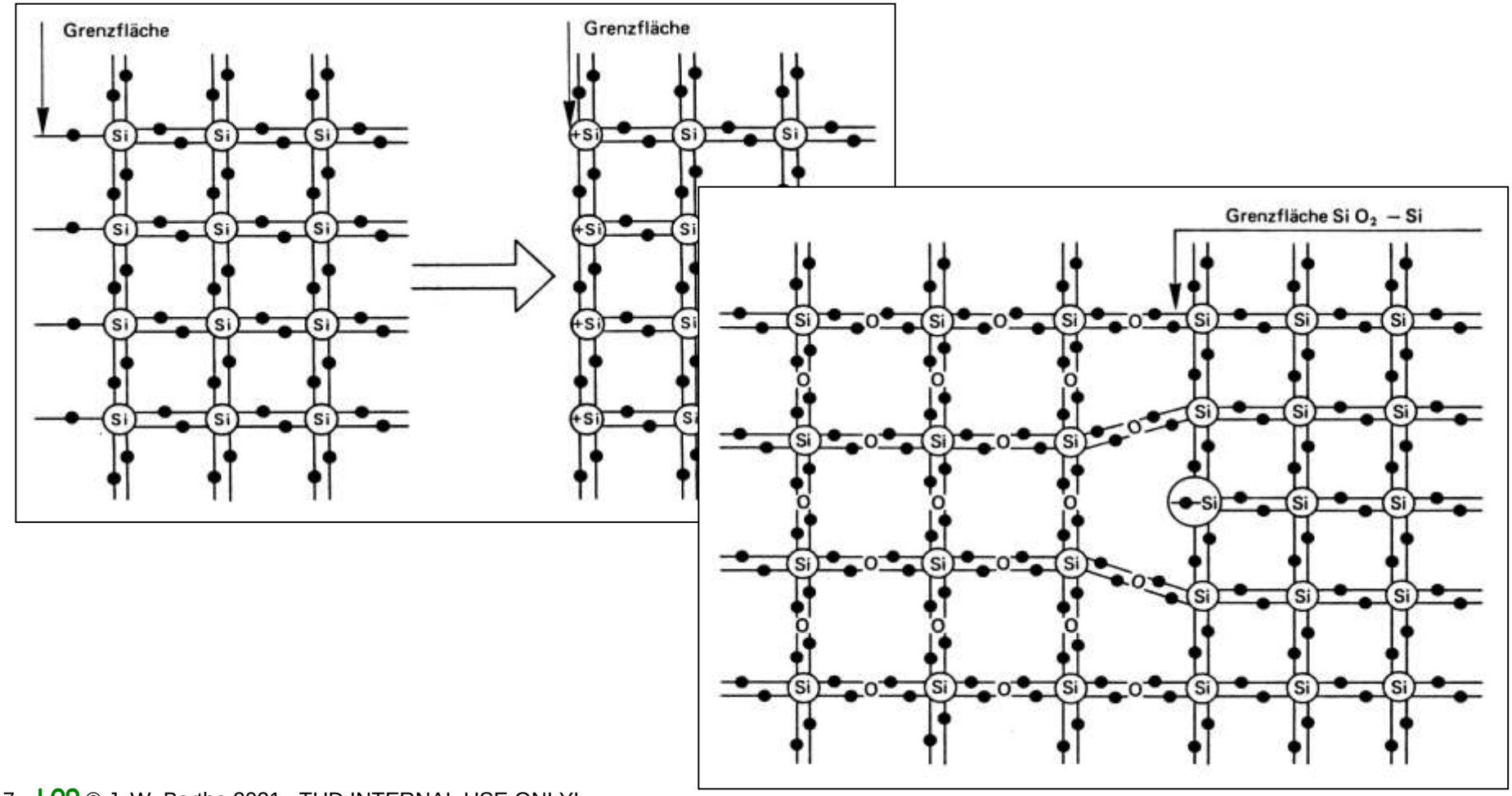
Please check also pdf file "MOScapAnim" at the OPAL folder

Transition to real conditions:
Including oxide charges

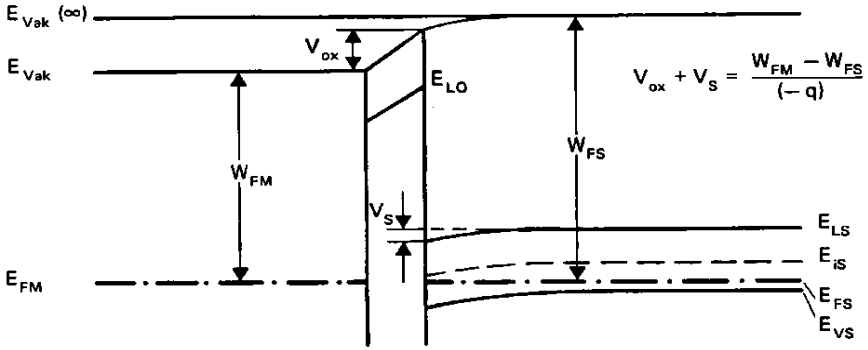


Transition to real conditions:
Including different workfunctions for Si and gate

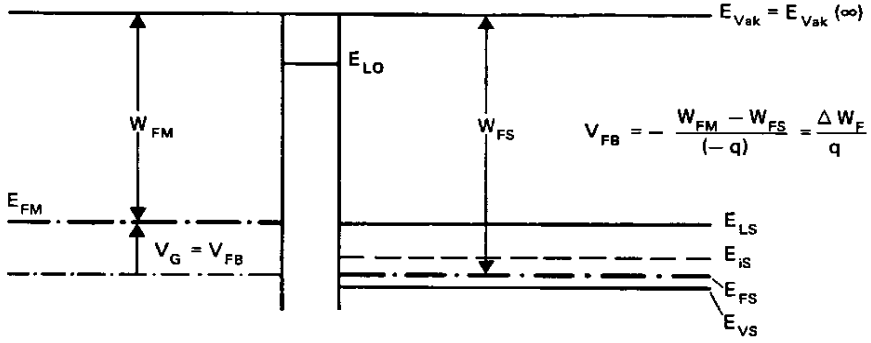
Workfunction of
n-Si ca. 4.3 eV
p-Si ca 5.1 eV

METAL	WORKFUNCTION (eV)	METAL	WORKFUNCTION (eV)
Al	4.3	Ru	4.7
Ti	4.33	Rh	4.98
V	4.3	Hf	3.9
Cr	4.5	Ta	4.25
Mn	4.1	W	4.55
Fe	4.7	Re	4.96
Co	5	Os	4.83
Ni	5.15	Ir	5.27
Nb	4.3	Au	5.1
Mo	4.6	TaN/TaSiN	3.9-4.3

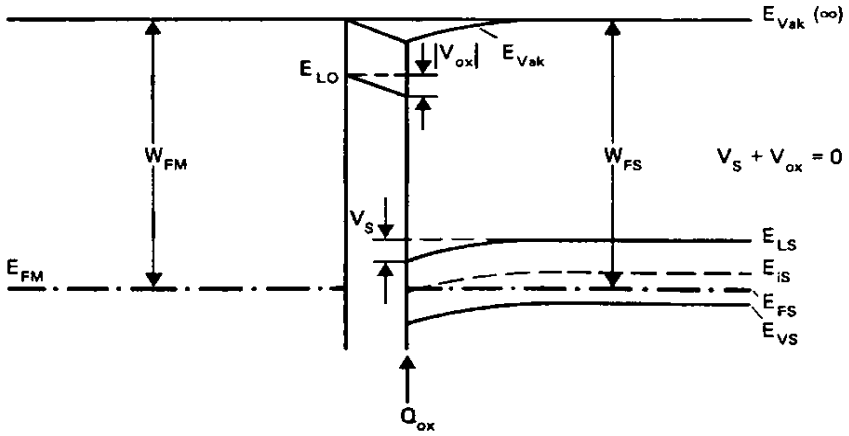
Consideration of work function difference and oxide charges



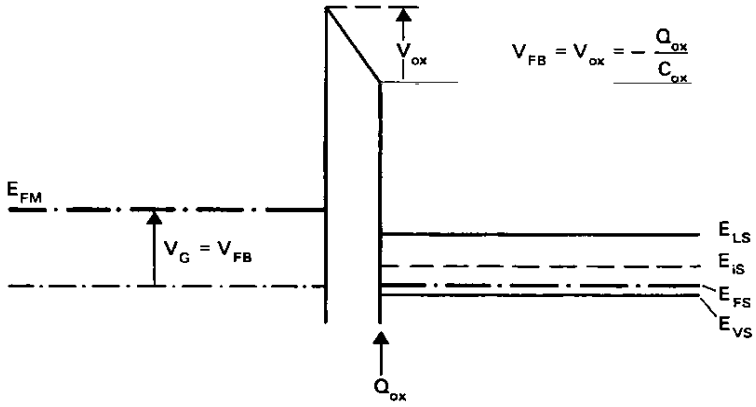
MOS-Struktur mit $\Delta W_F \neq 0$ im thermodynamischen Gleichgewicht



MOS-Struktur mit $\Delta W_F \neq 0$ im Flachbandzustand

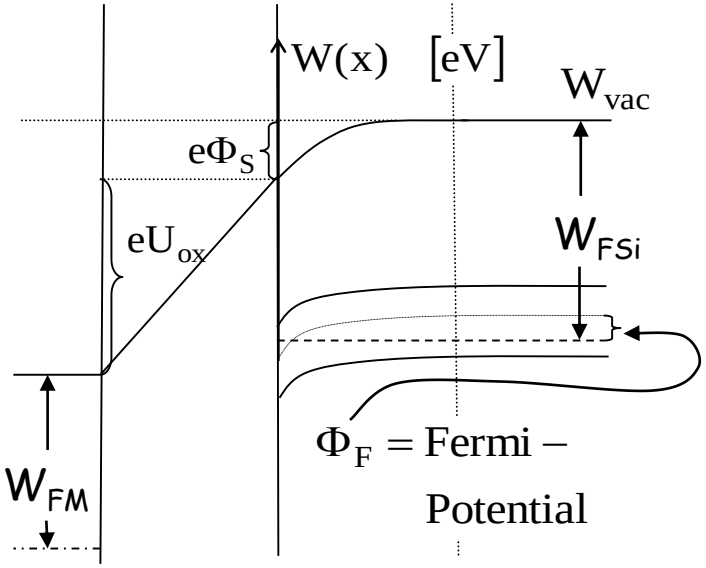


MOS-Struktur mit $Q_{ox} > 0$, $\Delta W_F = 0$ im thermodynamischen Gleichgewicht



MOS-Struktur mit $Q_{ox} > 0$, $\Delta W_F = 0$ im Flachbandzustand

Threshold voltage at MOS-FET /4



Ideal case:

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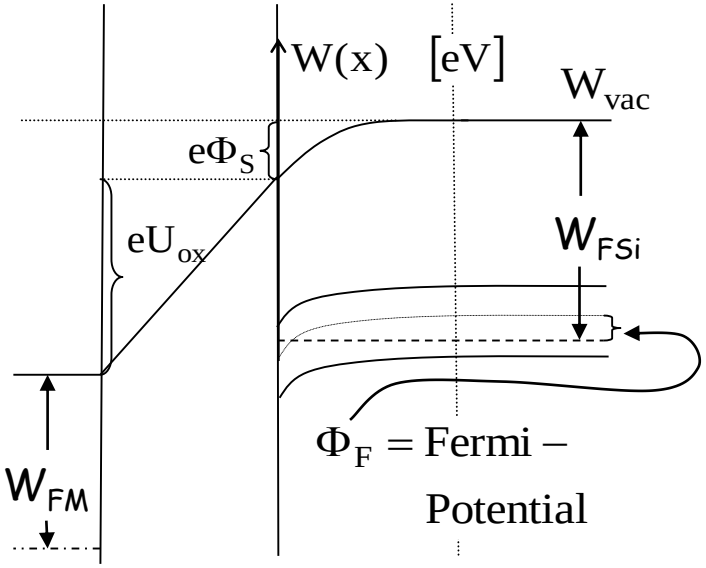
Oxide Charge and Workfunction included:

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{Si}eN_A(2\Phi_F)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

Threshold voltage at MOS-FET /4



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W_{FM}-W_{FSi}

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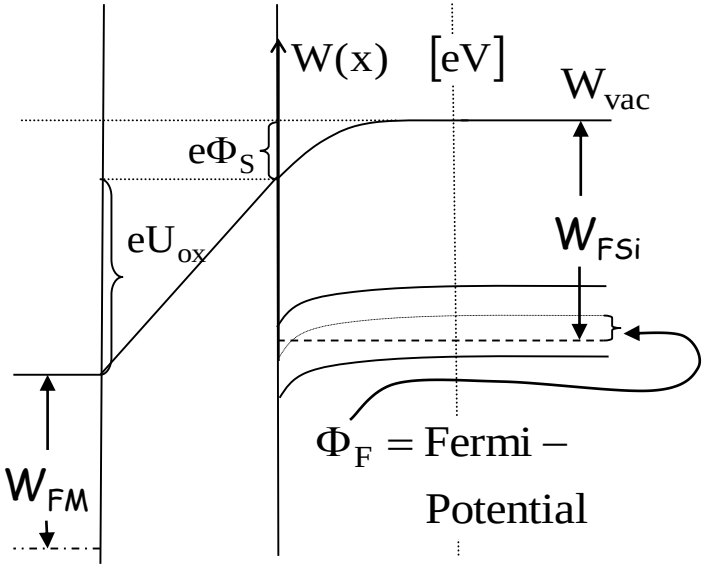
Threshold voltage at MOS-FET /4



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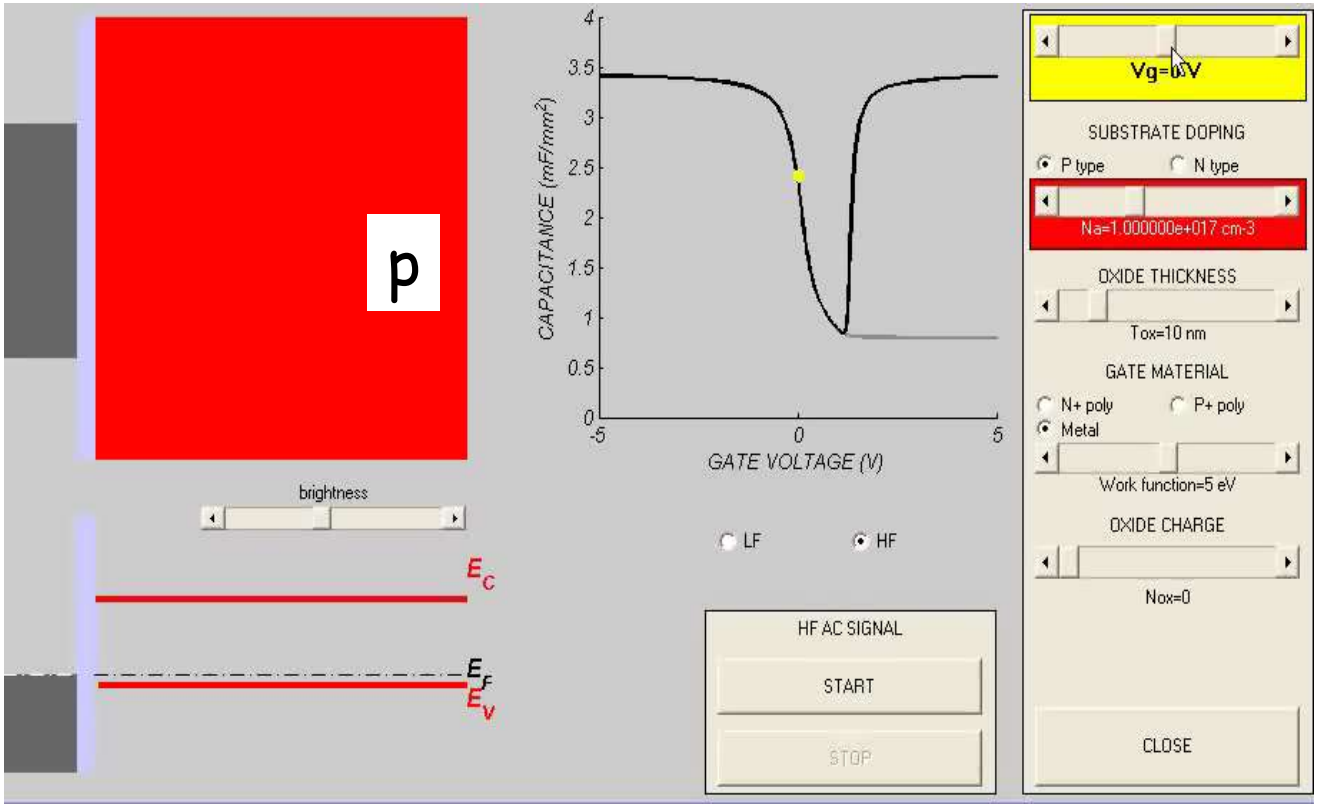
W_{FM}-W_{FSi}

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{Si}eN_A(2\Phi_F)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

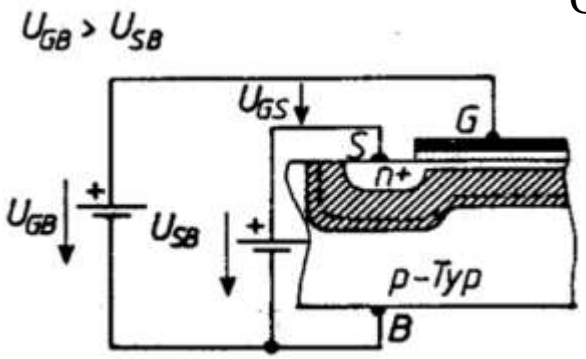
Further possibility to impact V_T: Application of a body potential V_{SB}

Demonstration: $V_T = f(d_{ox}, N_A, W_F \text{ und } Q_{ox})$



Please check also pdf file "MOScapAnimVt" at the OPAL folder

Threshold voltage at MOS-FET /5



$$Q_G = U_{ox} \cdot C_{ox} = (V_{GS} + V_{SB} - \Phi_s) \cdot C_{ox} = -Q_d$$

$$Q_d = -eN_A \cdot x_d = -eN_A \sqrt{\frac{2\varepsilon \Phi s}{eN_A}}$$

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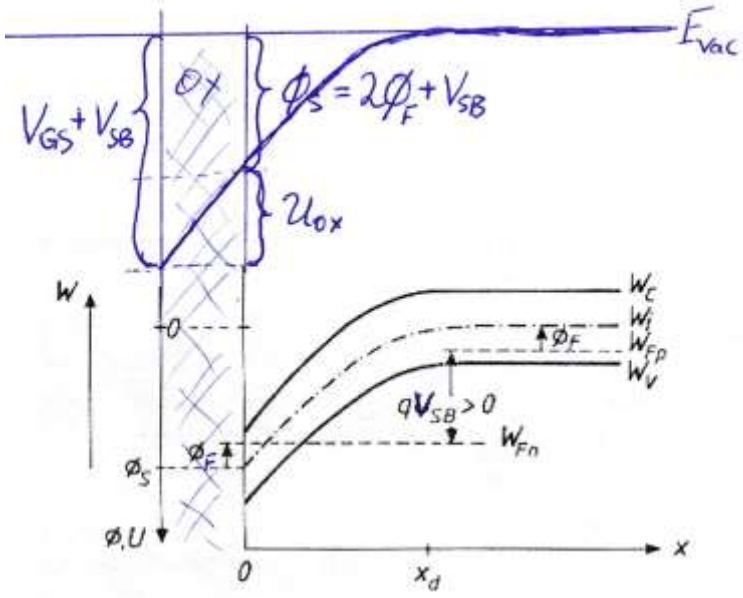
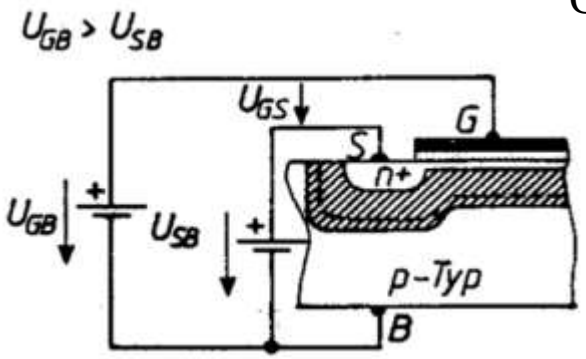
Threshold V_T reached when including substrate bias:



Threshold voltage at MOS-FET /5



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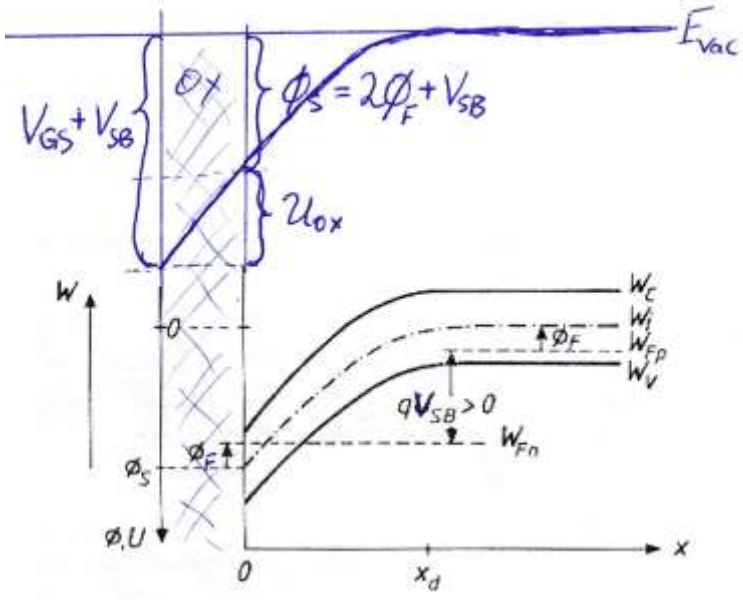


$$V_{GS} \equiv V_T \qquad \text{then} \qquad \Phi_S \to \Phi_S + V_{SB} \to 2\Phi_F + V_{SB}$$

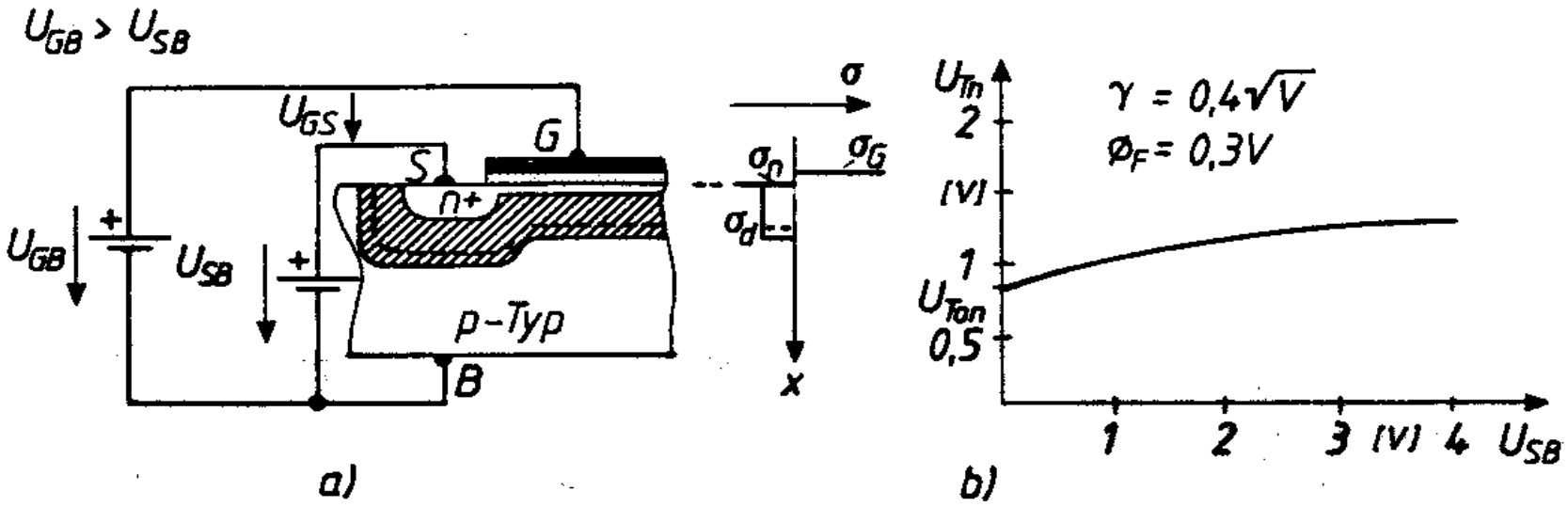
$$-Q_{d_{max}} = \sqrt{2eN_A\varepsilon(2\Phi_F + V_{SB})} = (V_{GS} - 2\Phi_F)C_{ox}$$

$$V_T = \frac{1}{C_{ox}}\sqrt{2eN_A\varepsilon(2\Phi_F + V_{SB})} + 2\Phi_F$$

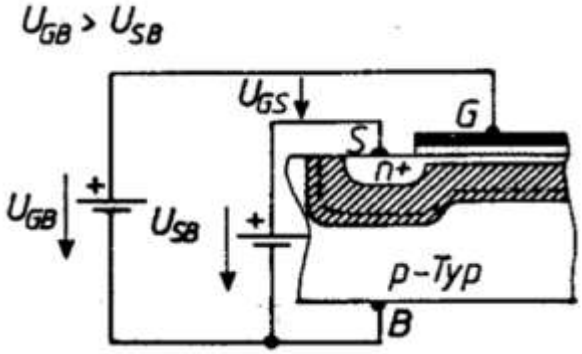
Consideration of Oxide Charge and Workfunction

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{Si}eN_A(2\Phi_F + V_{SB})} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

V_T with substrate bias



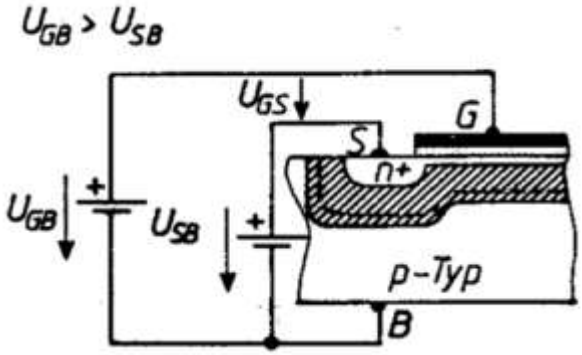
Threshold voltage at MOS-FET /6



$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

Controllable Parameters:
- -Dielectric Thickness / Dielectric Constant (k)
- -Substrate Dopant Concentration
- -Oxide Charge
- -Workfunction Difference
- -Body Potential

Threshold voltage at MOS-FET /6



W_{FM}-W_{FSi}

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Threshold voltage at MOS-FET /6

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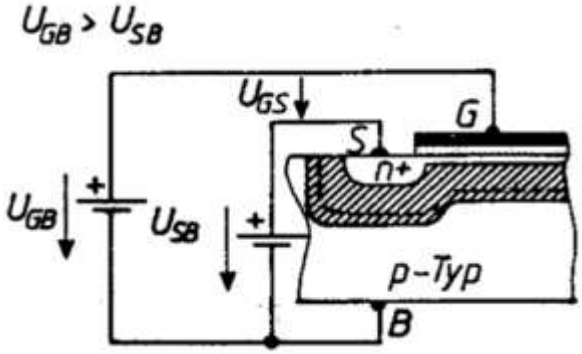
VIDEO CAMPUS SACHSEN

Parasitic FET



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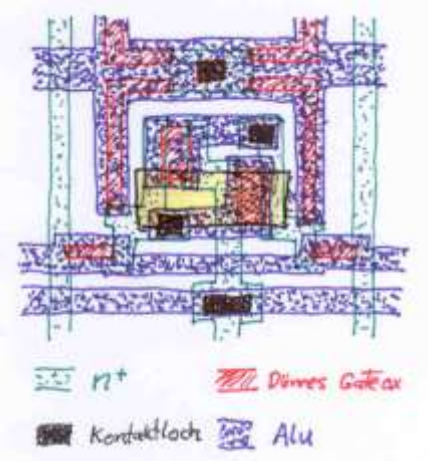
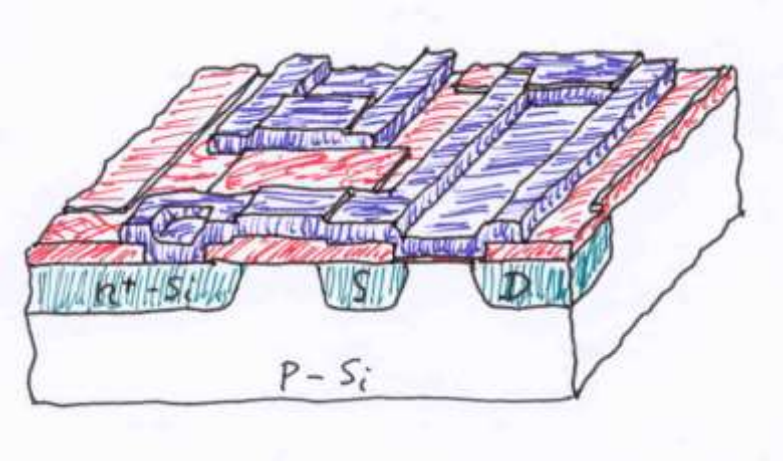
2.4.1 Parasitic Transistor

What's a parasitic FET?

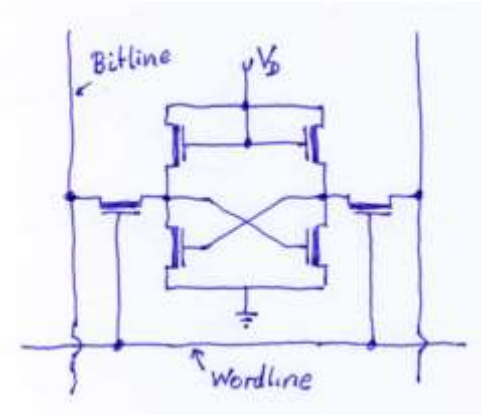
2.4.1 Parasitic Transistor

What's a parasitic FET?



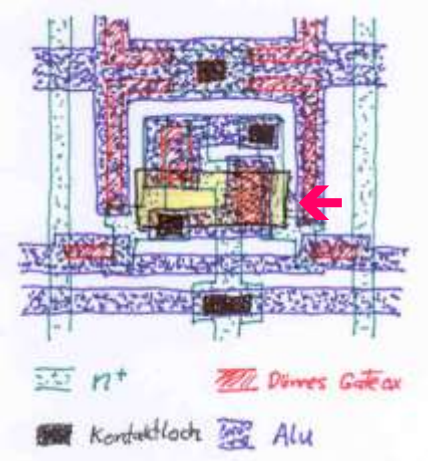


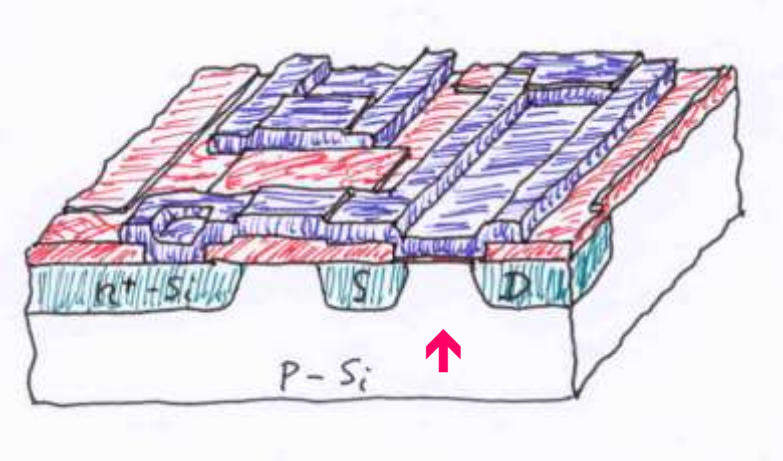
Remember our SRAM cell:



2.4.1 Parasitic Transistor

What's a parasitic FET?





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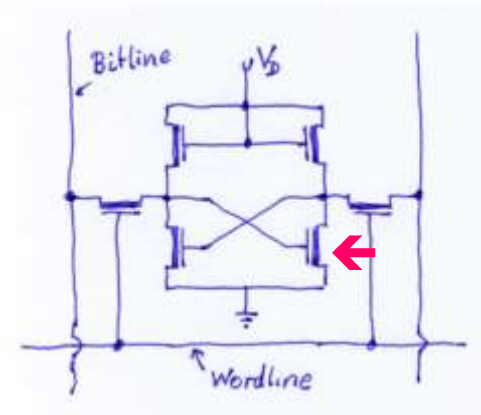
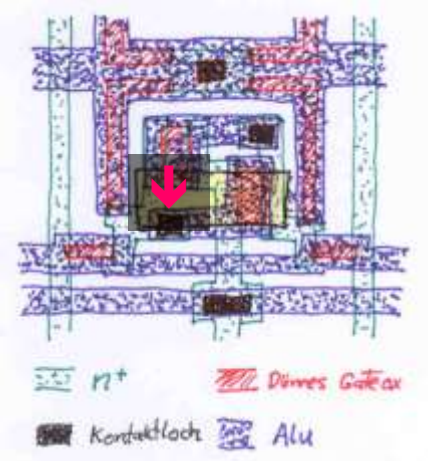
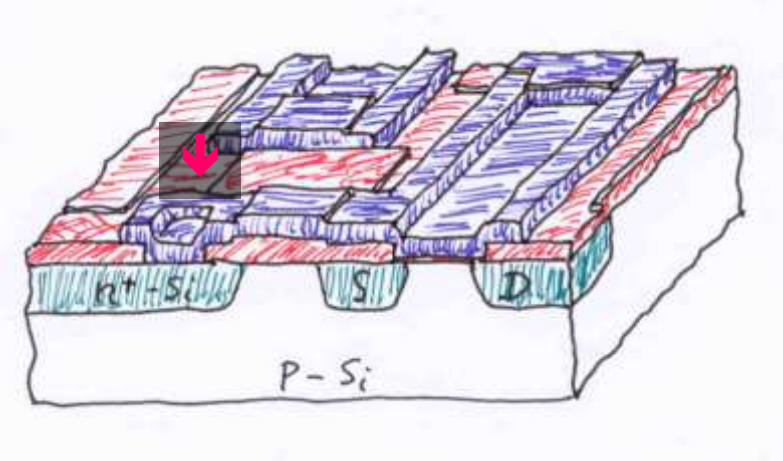


A regular FET is the switching transistor shown in the different pictures and consist of the n^+ Source, the p-substrate and the n^+ Drain region, the substrate region is covered with the thin oxide and the gate electrode.

2.4.1 Parasitic Transistor

What's a parasitic FET?





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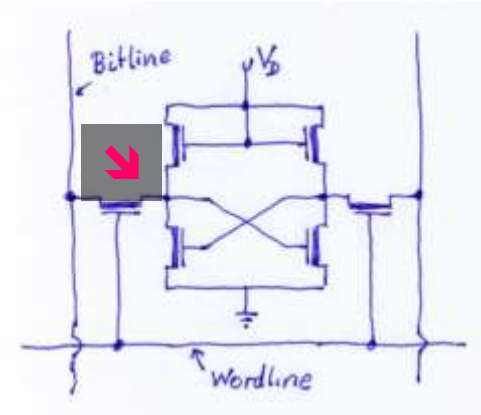
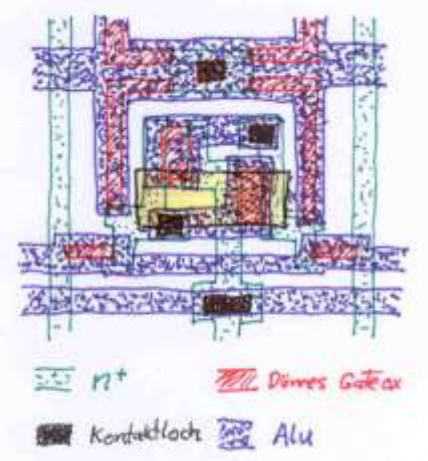
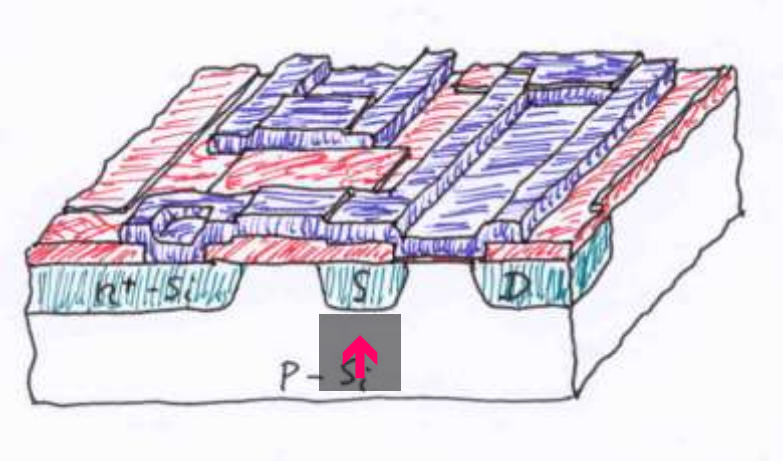


The Gate-line runs over the fieldox to the left and connects to the Drain of the left switching transitor resp. the Source of the left load transistor.

2.4.1 Parasitic Transistor

What's a parasitic FET?





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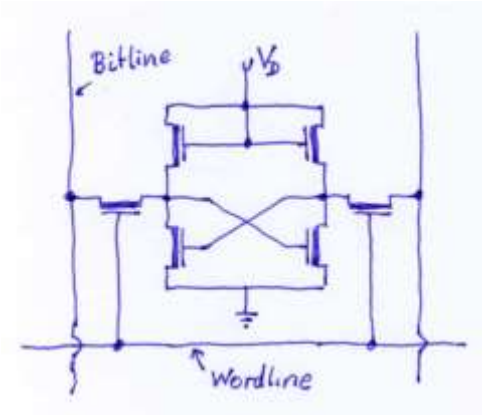
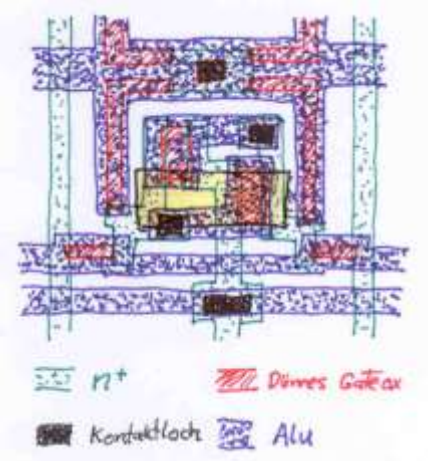
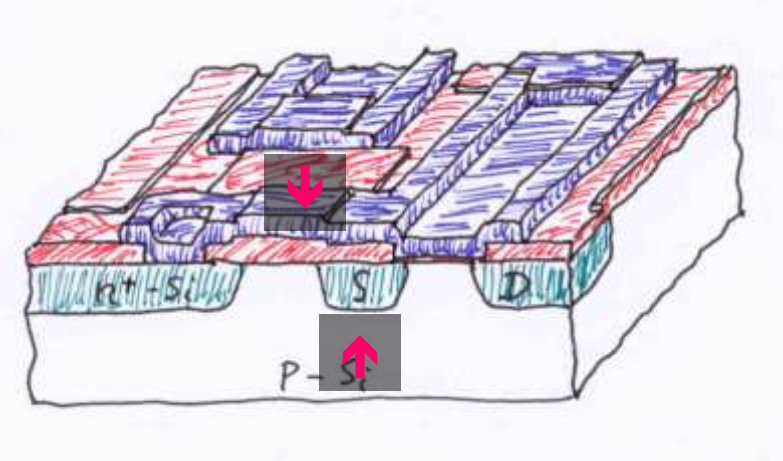


We can think of the source,

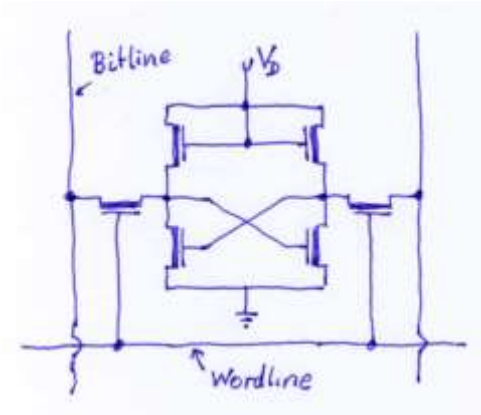
2.4.1 Parasitic Transistor

What's a parasitic FET?





Remember our SRAM cell:



We can think of the source, the Gate over the fieldox,

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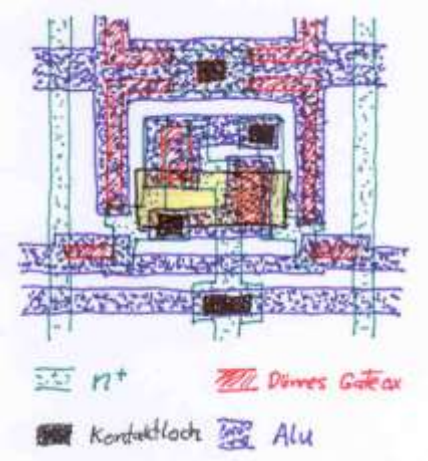

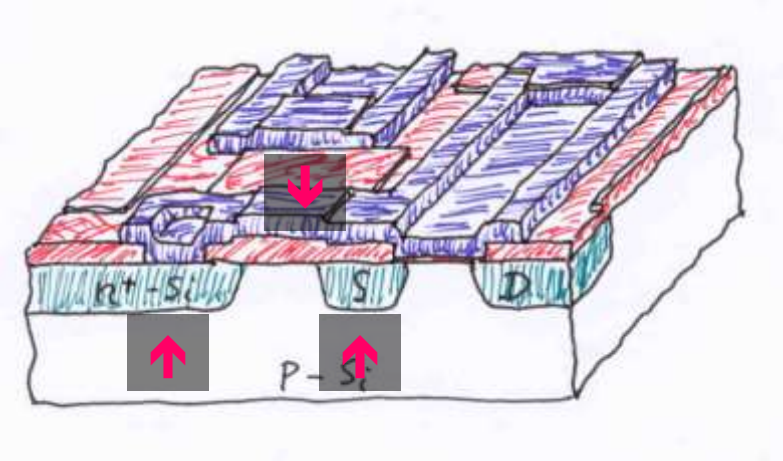

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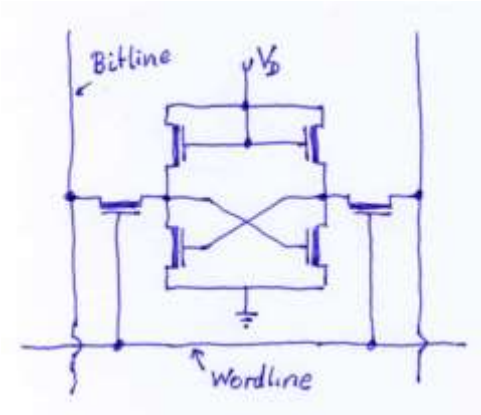

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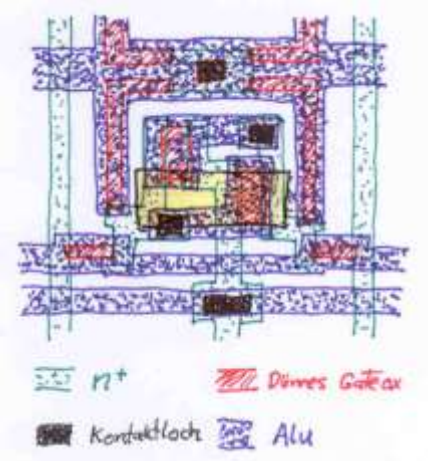

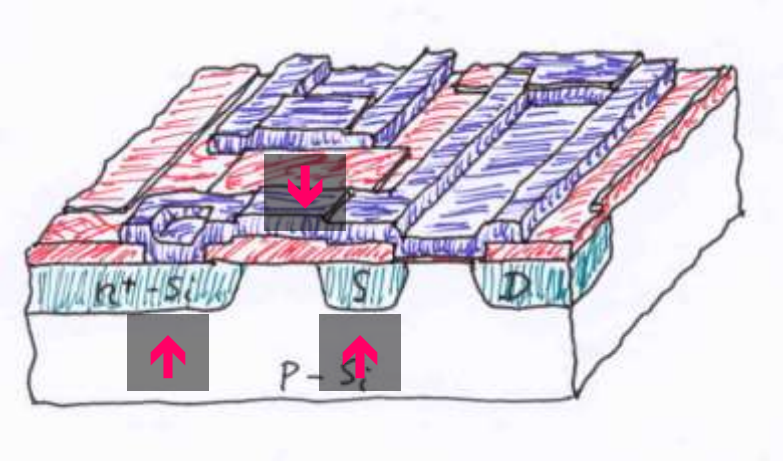

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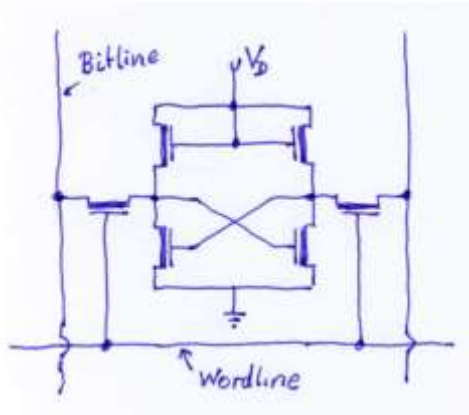

We can think of the source, the Gate over the fieldox, and the n^+ line as a further MOS FET, which has a high threshold voltage due to the large thickness of the fieldox.

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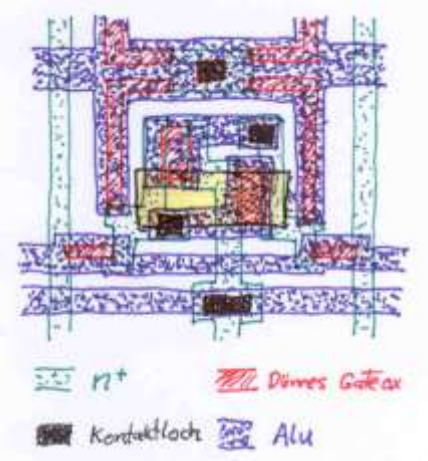

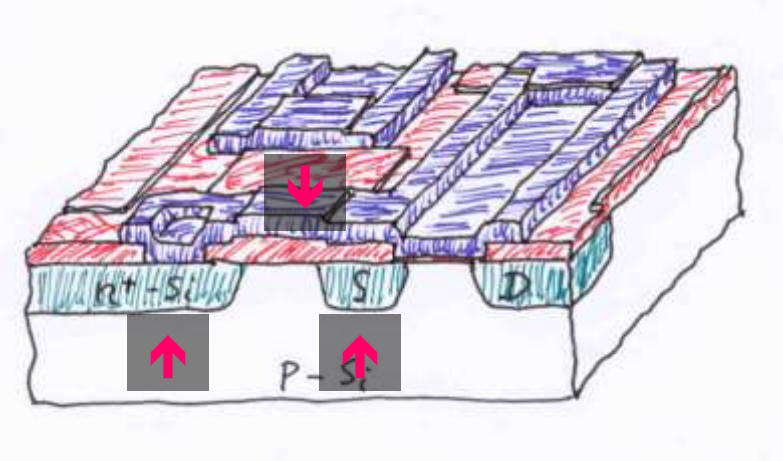

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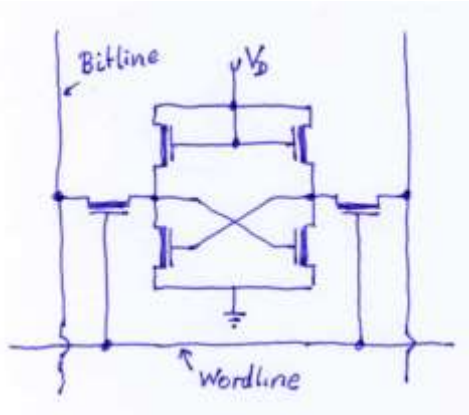

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This FET is called parasitic transistor. It might unintentionally connect any n^+ region where Gate lines run over the fieldox. To avoid this, the fieldox thickness has to be as large as possible.

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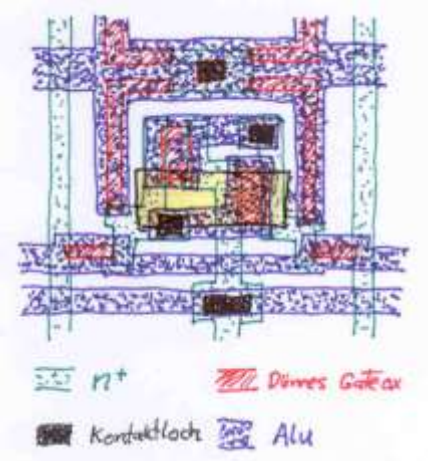

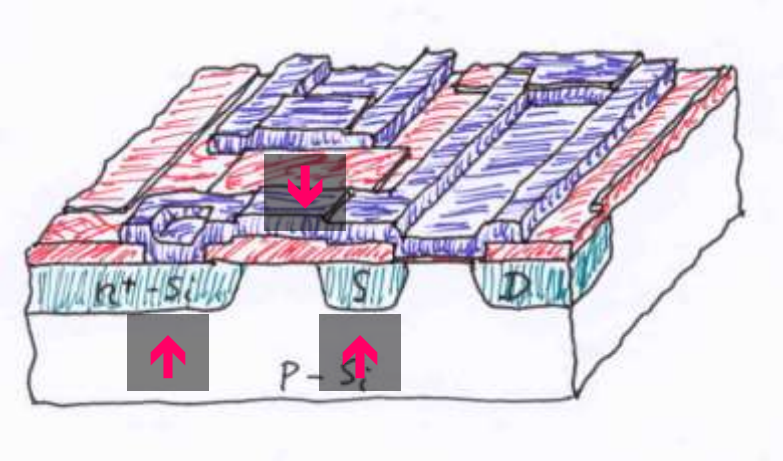

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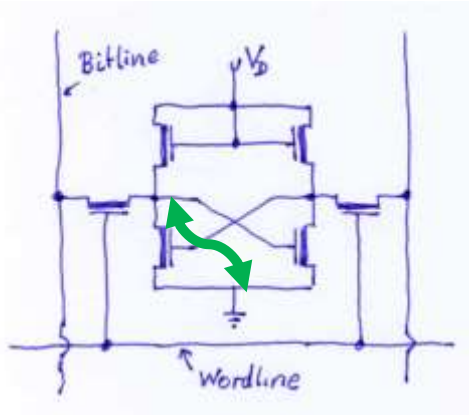

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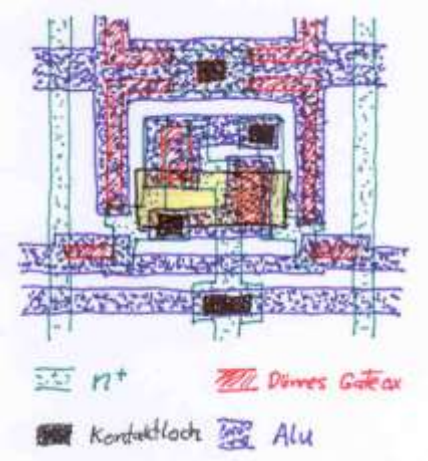

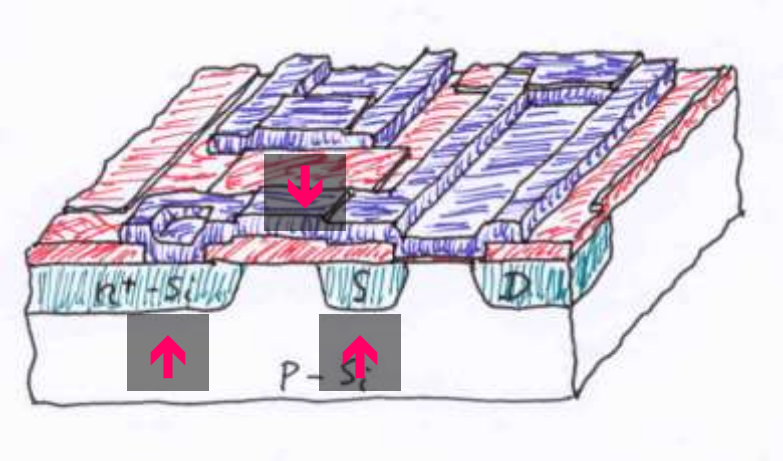

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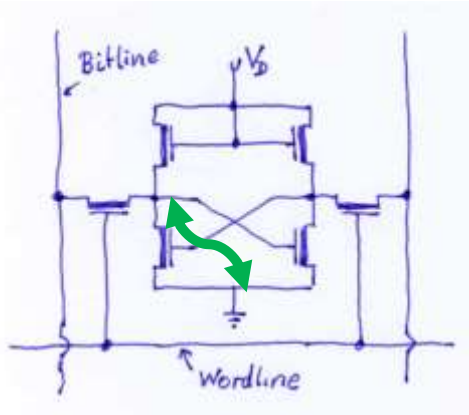

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$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

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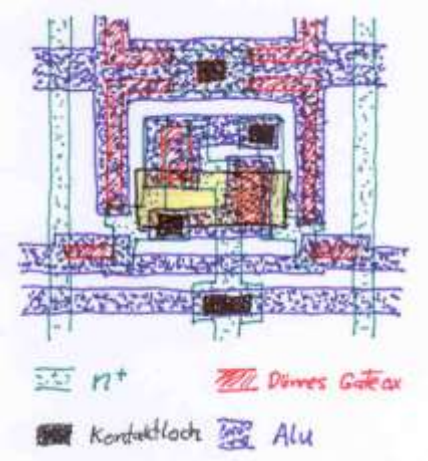

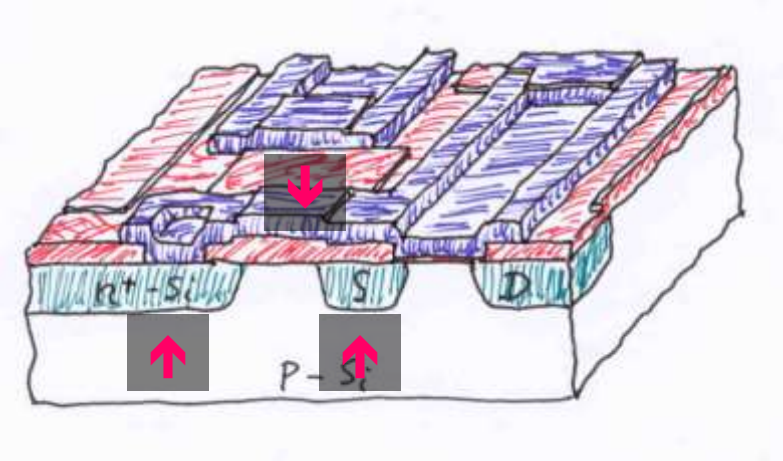

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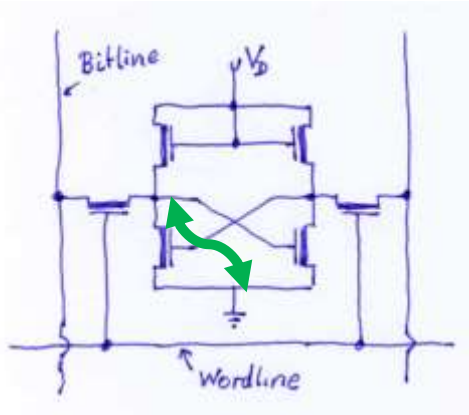

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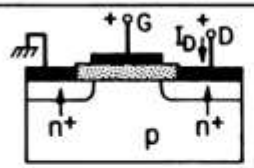
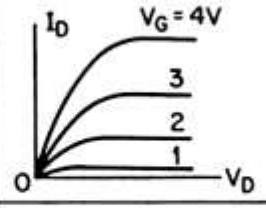
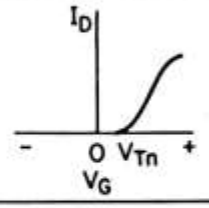
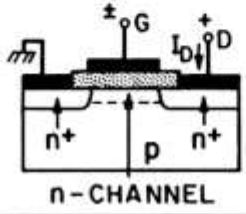
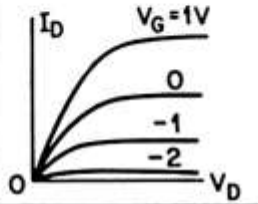
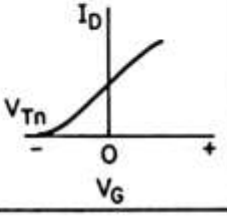
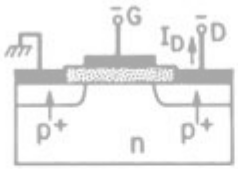
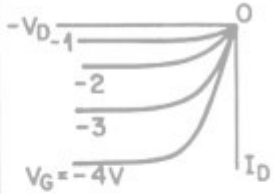
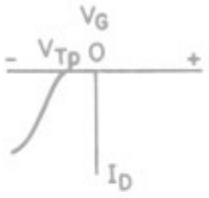
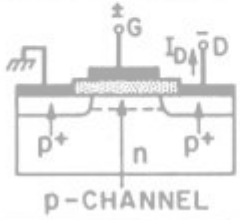
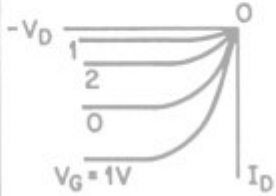
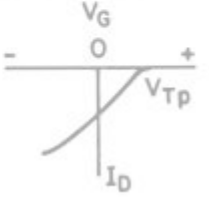
Continue ➡

"SCT_SS20_09.05" 17:53

VIDEO CAMPUS SACHSEN

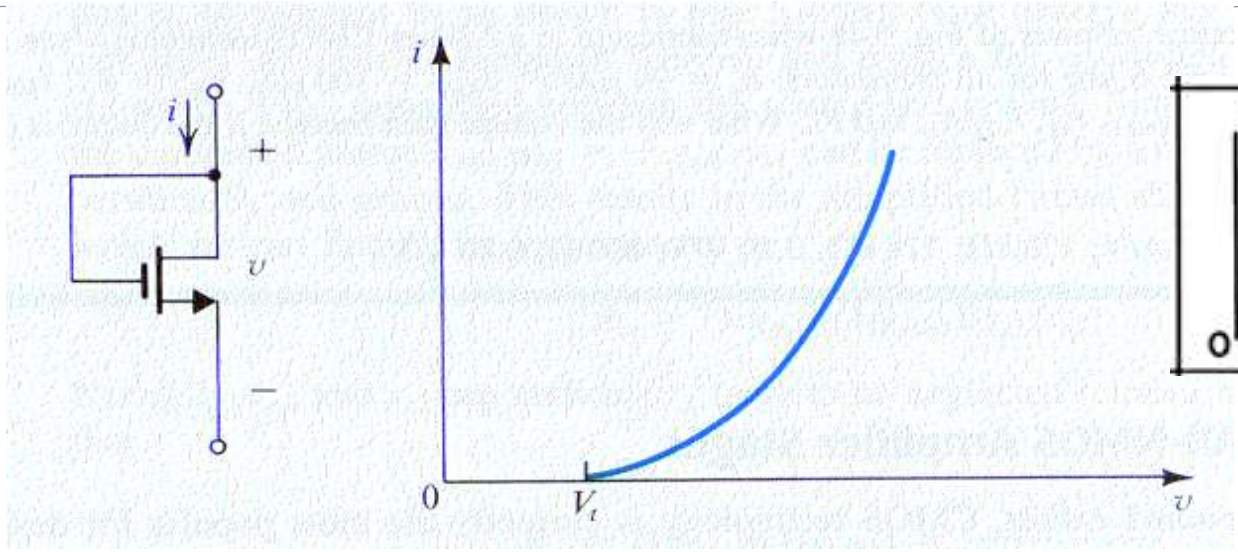
E/D

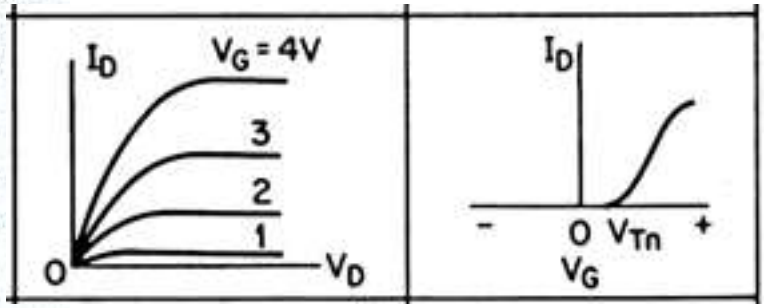
2/4 Types of MOSFET

TYPE	CROSS SECTION	OUTPUT CHARACTERISTICS	TRANSFER CHARACTERISTICS
n-CHANNEL ENHANCEMENT (NORMALLY OFF)			
n-CHANNEL DEPLETION (NORMALLY ON)			
p-CHANNEL ENHANCEMENT (NORMALLY OFF)			
p-CHANNEL DEPLETION (NORMALLY ON)			

Shifting V_T of the n-channel enhancement FET to negative values creates a **n-channel Depletion transistor!**
This can be utilized as a novel load element.

Load resistor by enhancement- or depletion-Transistor





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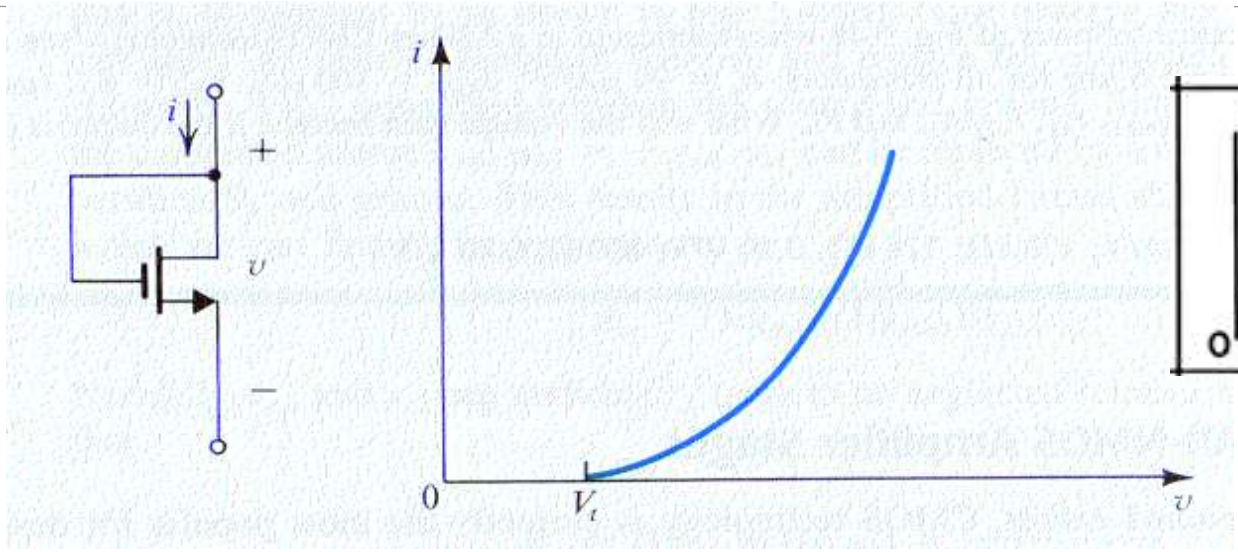

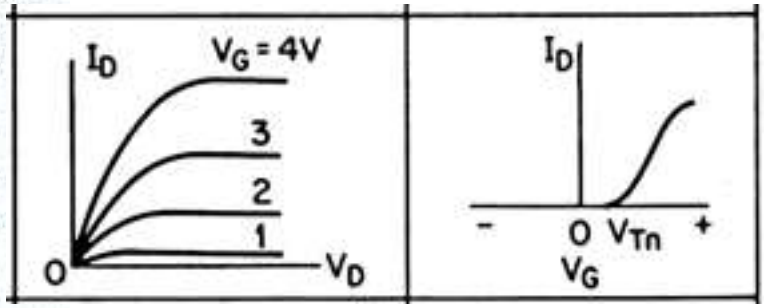

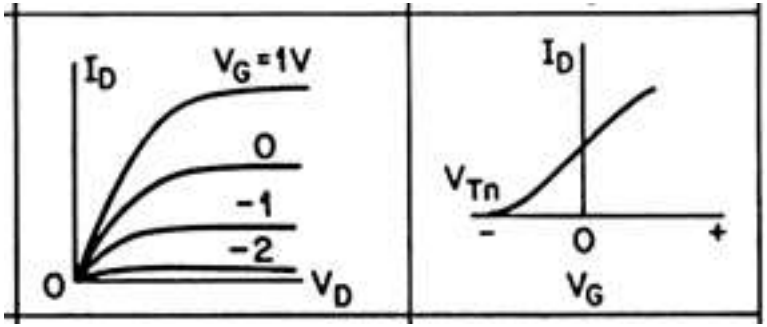

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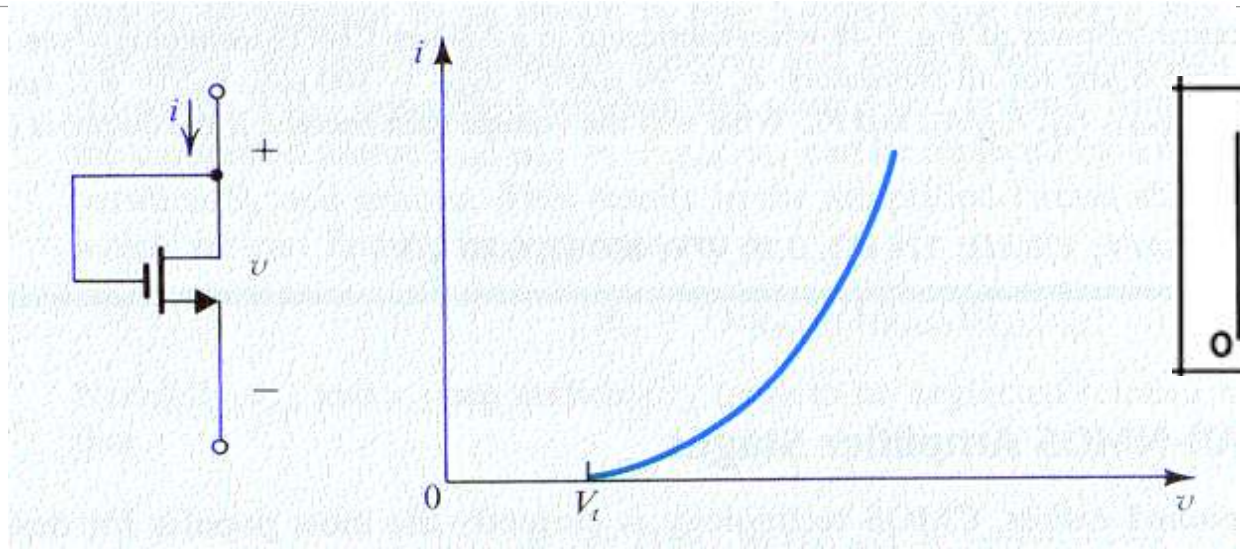
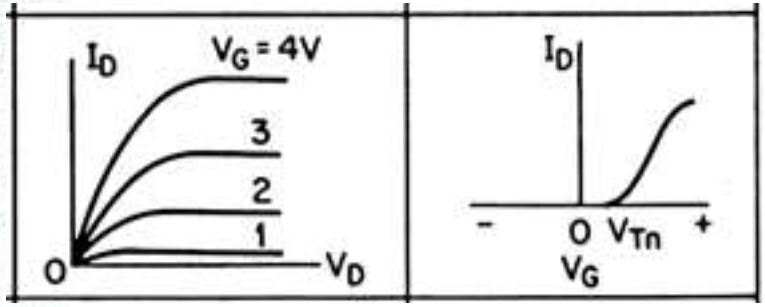
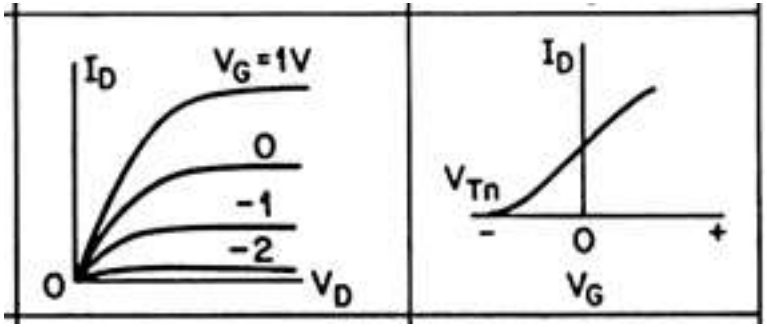
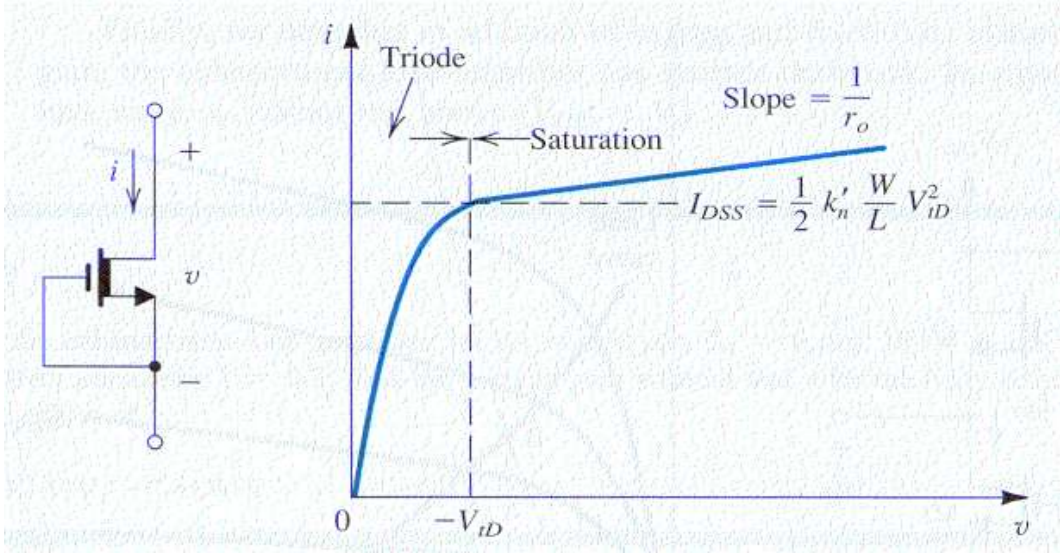


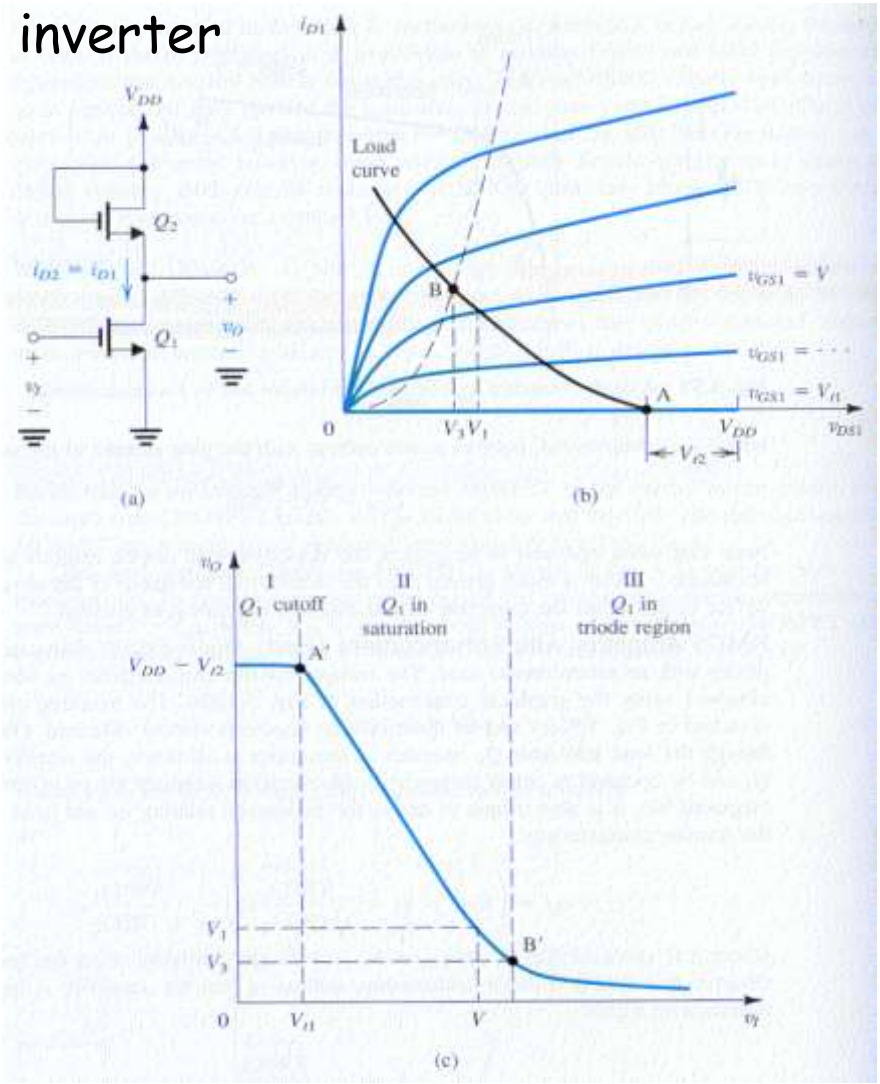






2.4.3 Load resistor by enhancement- or depletion-Transistor

E/E inverter



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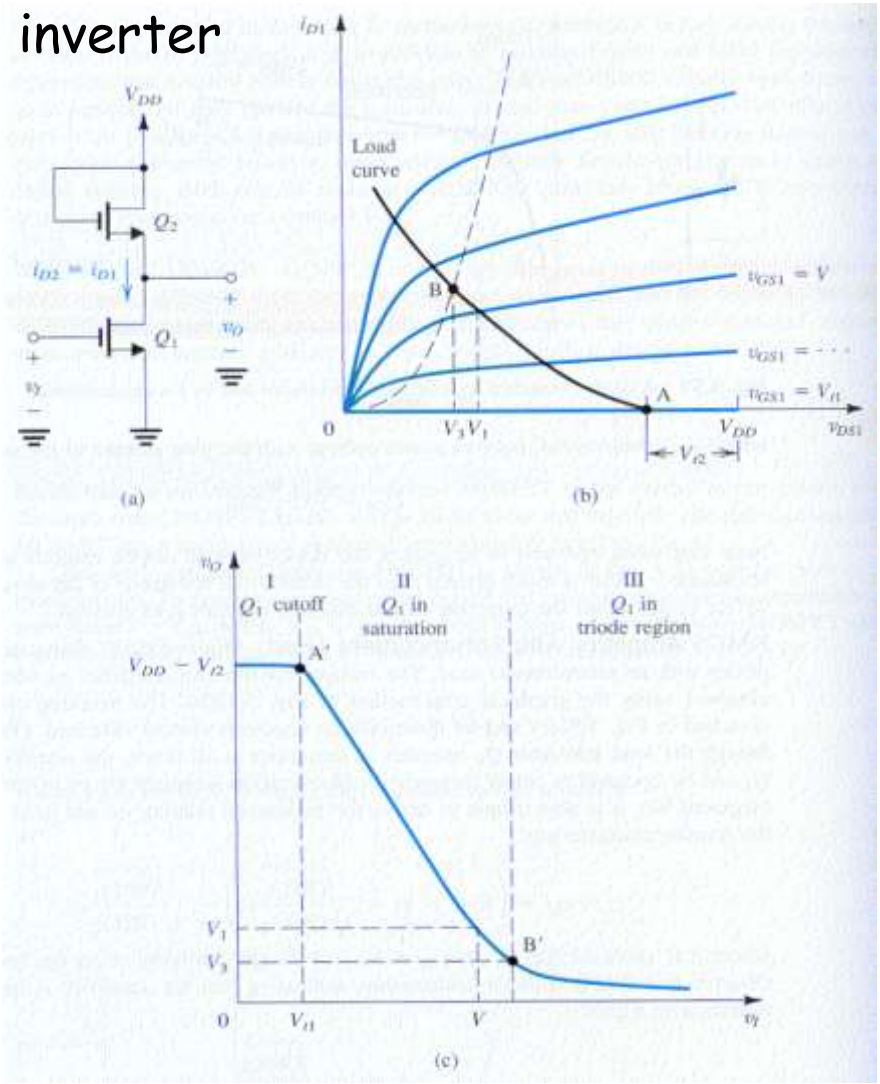
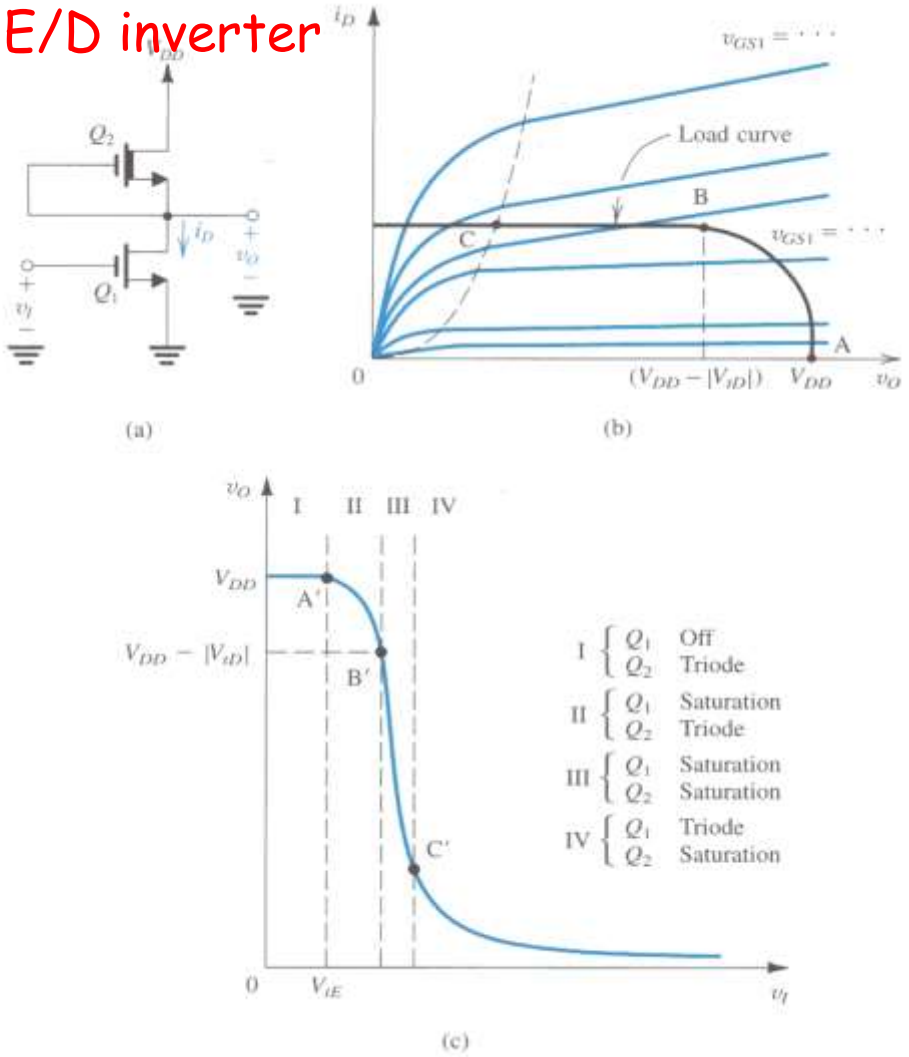


E/D inverter



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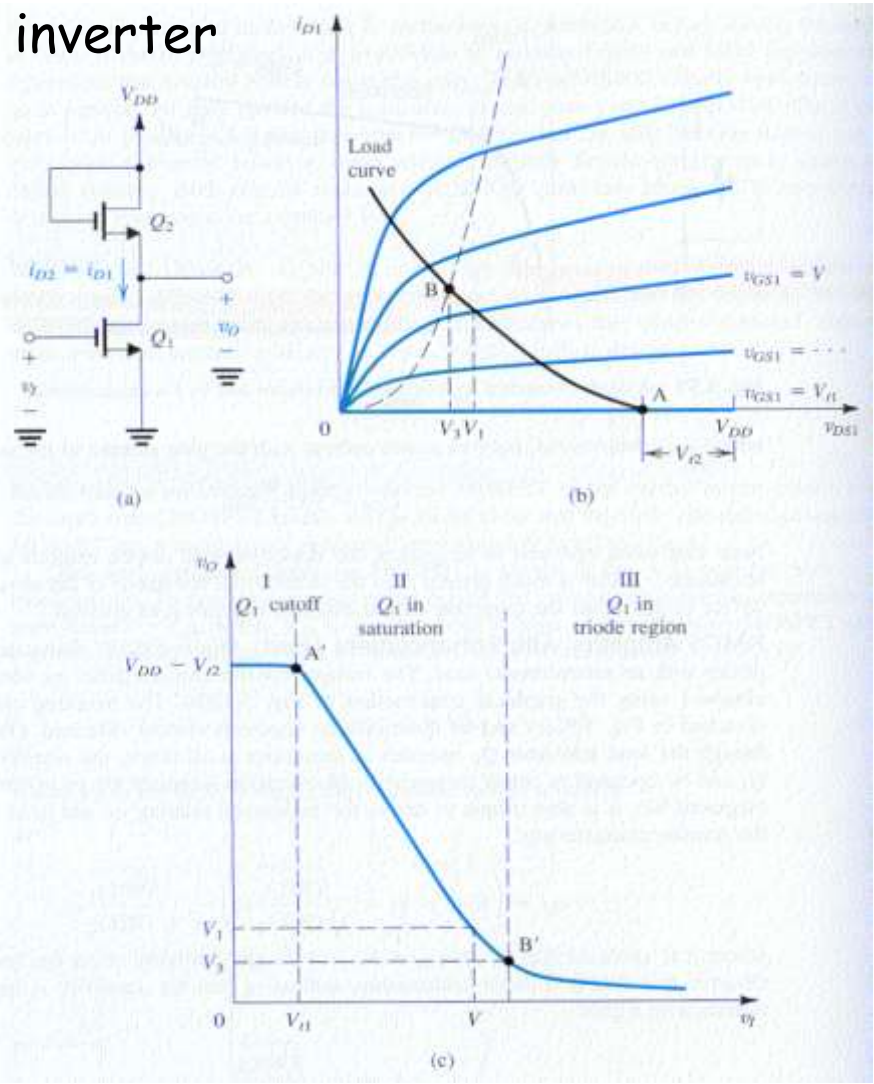

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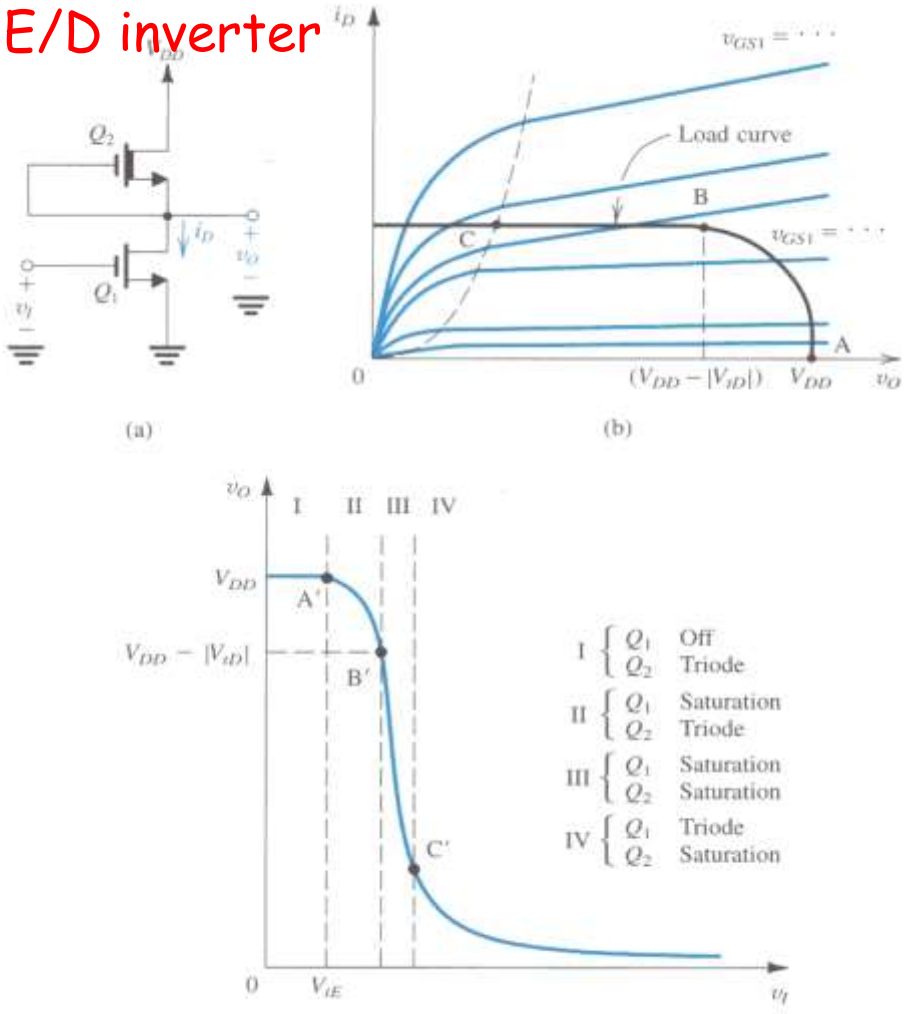


Much better transfer behavior of the E/D inverter!

1. $V_{outmax}=V_{DD}$
2. Slope in the transfer curve high

2.4.4 N-MOS Enhancement/Depletion Process flow

-Field oxidation

-Mask 1: S/D opening, P-Diffusion

-Post oxidation – drive in

-Mask 2: V_T adjustment of the Enhancement Transistor via B-Implant

-Mask 3: Etching of Gate- und S/D contact

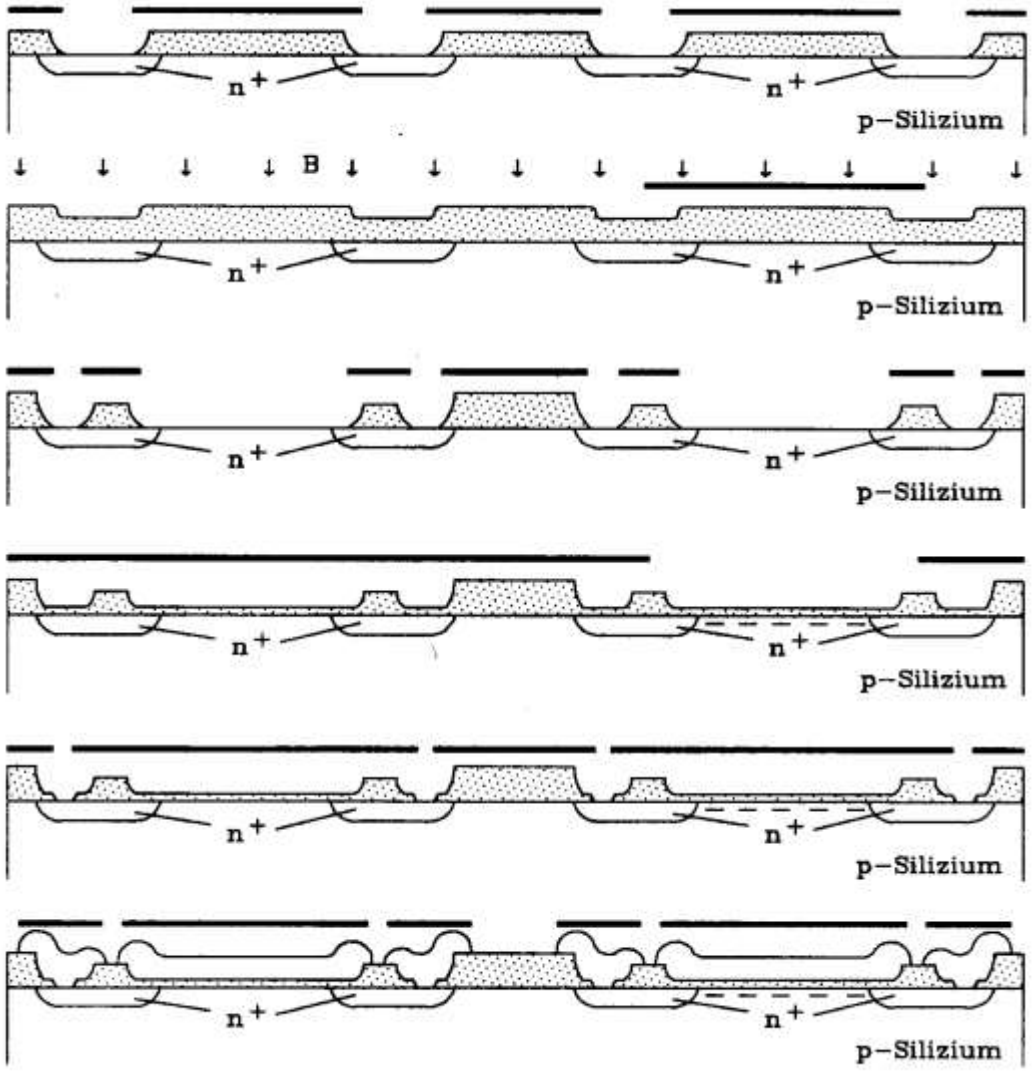
-Gate oxidation

-Mask 4: V_T adjustment of the Depletion Transistor via As-Implant through the Gateox

-Mask 5: Opening of S/D contacts

-Deposition of conductor layer (Al)

-Mask 6: Metal etch (both Gate and Source / Drain)



Intermediate Summary:

- Semiconductor properties

- Process Integration:
  Match Electric function with Design and Materials Properties

- MOSFET properties:
  I_{Dsat} depends on: W/L, d_{ox}, μ, ε_r, V_{dd}
  V_T depends on d_{ox}, N_A, Q_{ox}, ΔW, V_{SB}

- Types of MOSFET:
  N-Channel, P-Channel, Enhancement-, Depletion-

- Different inverters:
  E/E inverter (4 Masks) and E/D inverter (5 or 6 Masks)

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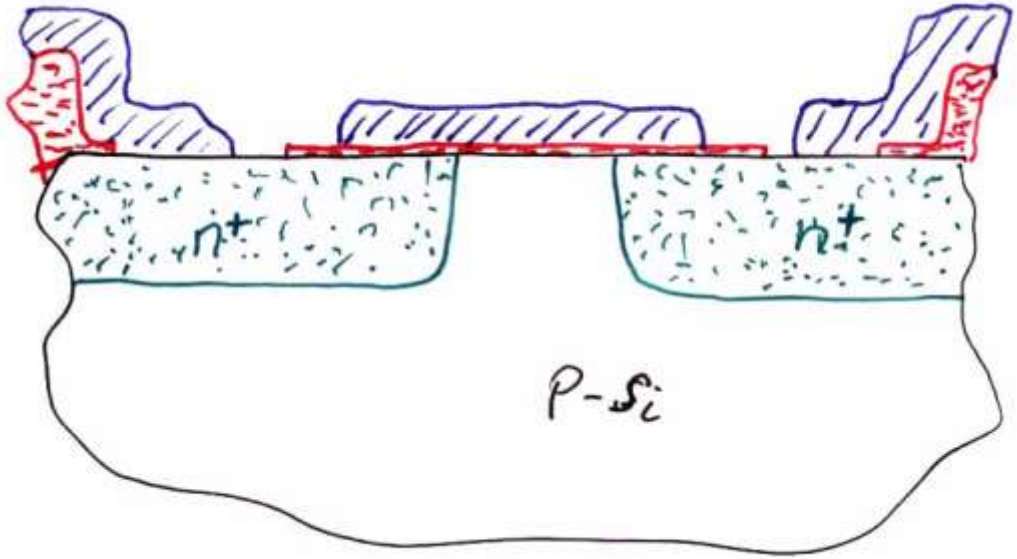
3. Self Aligned Process

No sub micrometer integration without self alignment!

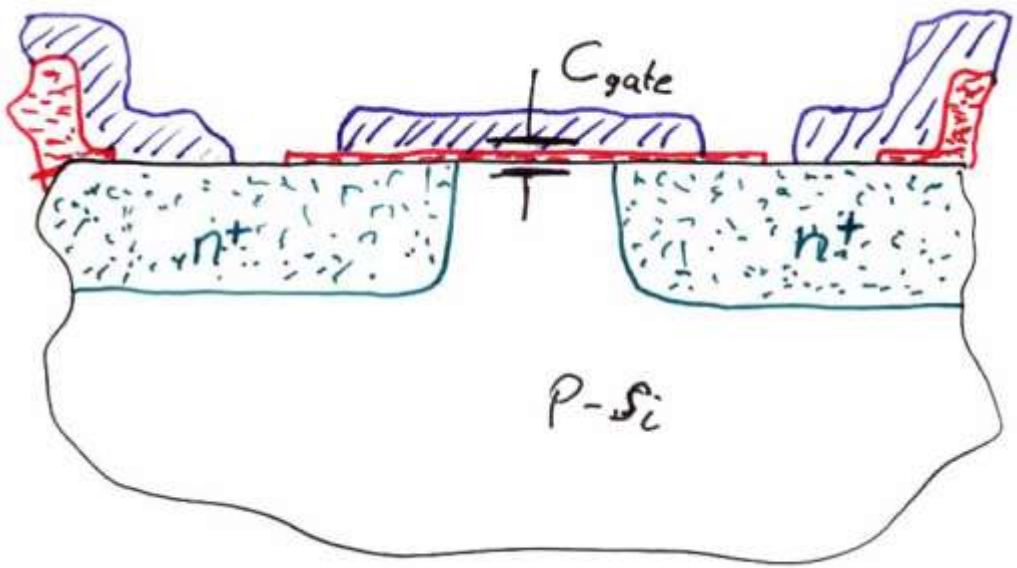
3.1 Al(Metal)-Gate -> Si-Gate

The FET has two important Capacities:



3.1 Al(Metal)-Gate -> Si-Gate

The FET has two important Capacities:



The Gate capacity determined by the charge to form the inversion channel

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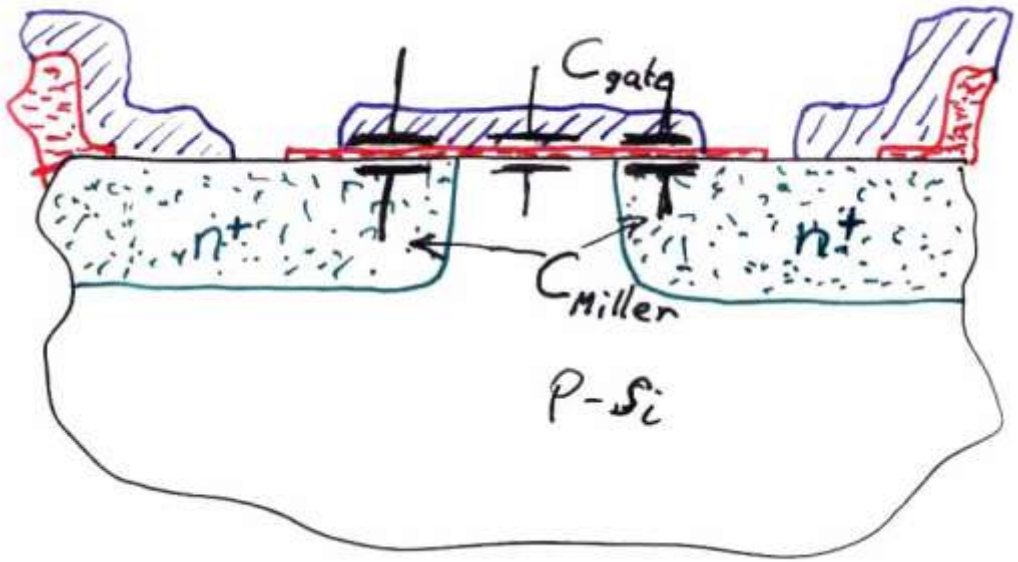

The Gate capacity determined by the charge to form the inversion channel

and the parasitic capacitors resulting from the overlap of the gate metal with the source/drain region.

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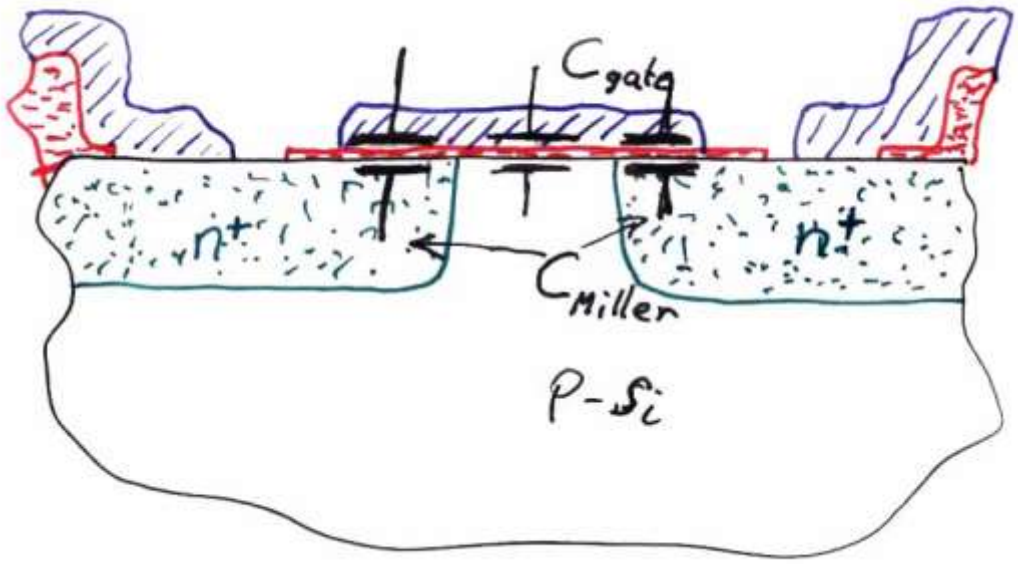


The Gate capacity determined by the charge to form the inversion channel

and the parasitic capacitors resulting from the overlap of the gate metal with the source/drain region.

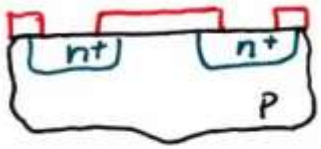
The overlap is associated with the limited overlay accuracy of the mask aligner. (Pattern must be larger by twice the overlay accuracy!)

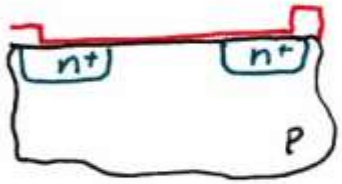
Innovation: Si-Gate Process

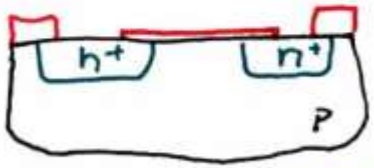
Remember!

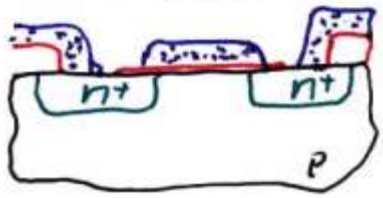
Metal Gate FET requires 4 Mask Levels:

- S/D
- Fieldox
- Contact
- Metal









Innovation: Si-Gate Process

Now, a new integration scheme:

Remember!

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- Contact
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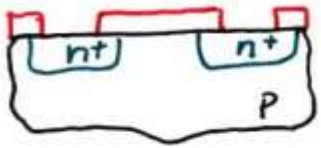

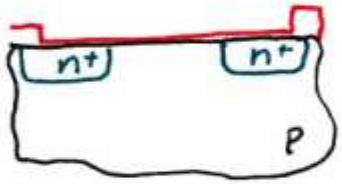

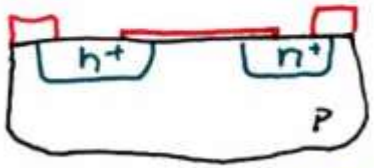

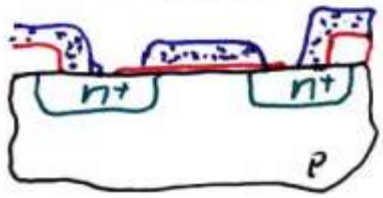

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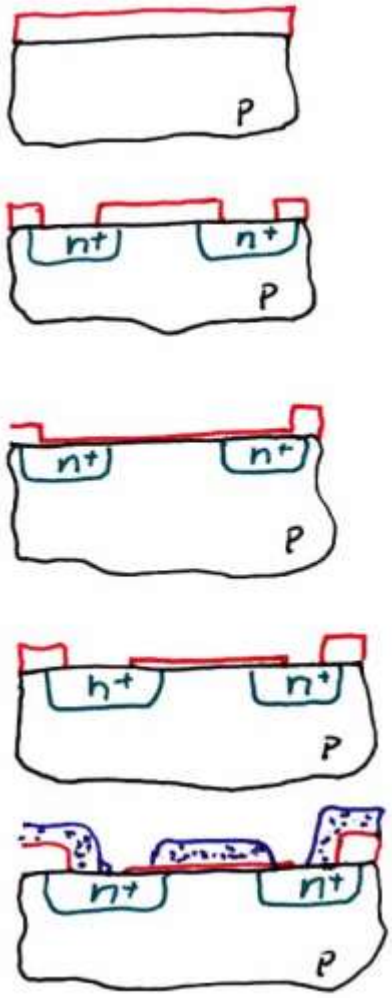

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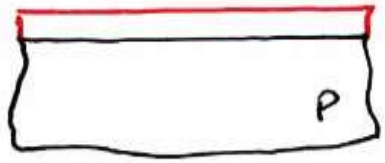

We start with the "field Oxidized" Wafer

Innovation: Si-Gate Process

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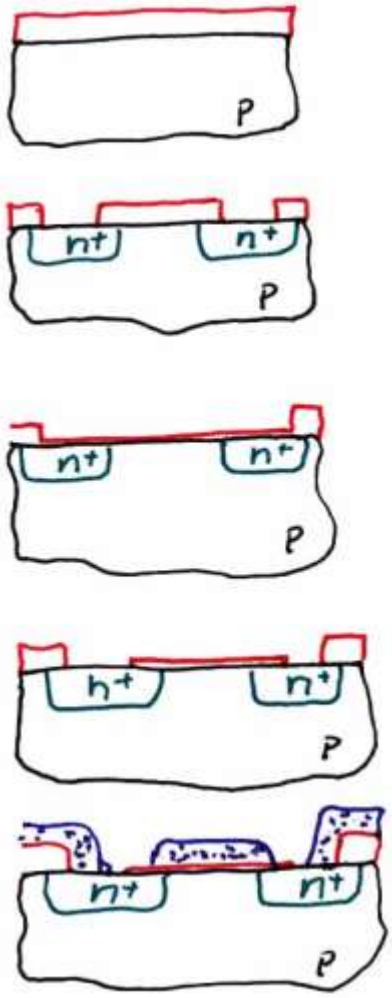

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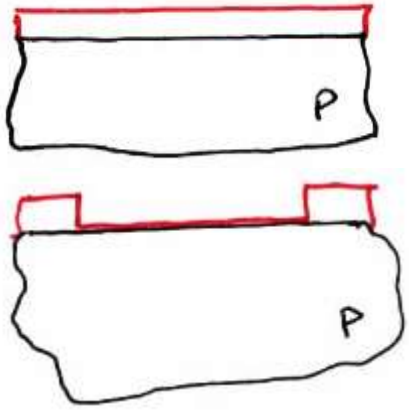

We start with the "field Oxidized" Wafer

define the Field ox and grow the Gate ox

Innovation: Si-Gate Process

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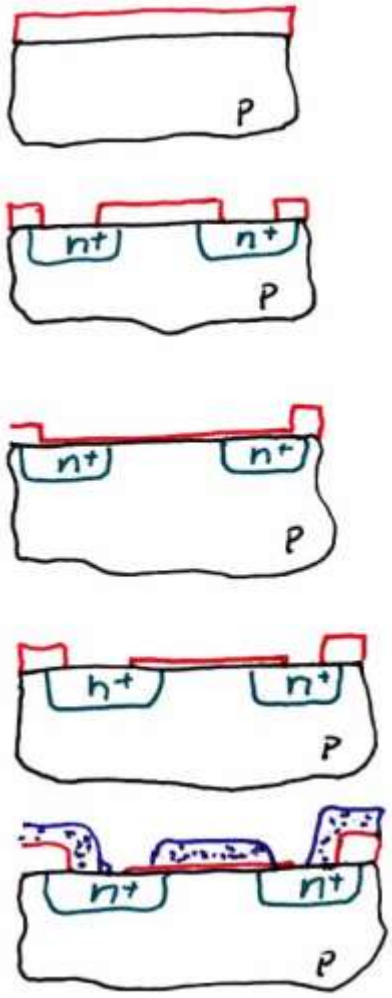

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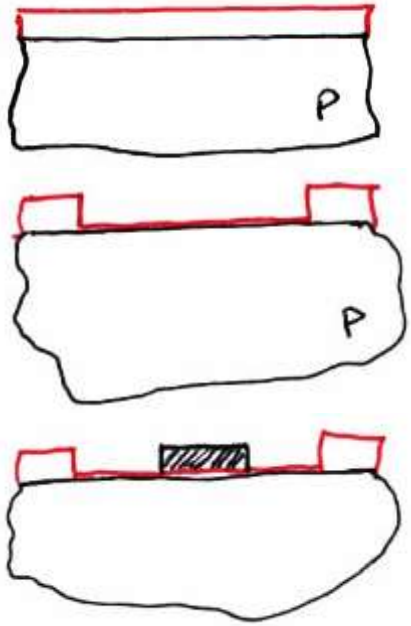

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define the Field ox and grow the Gate ox

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Innovation: Si-Gate Process

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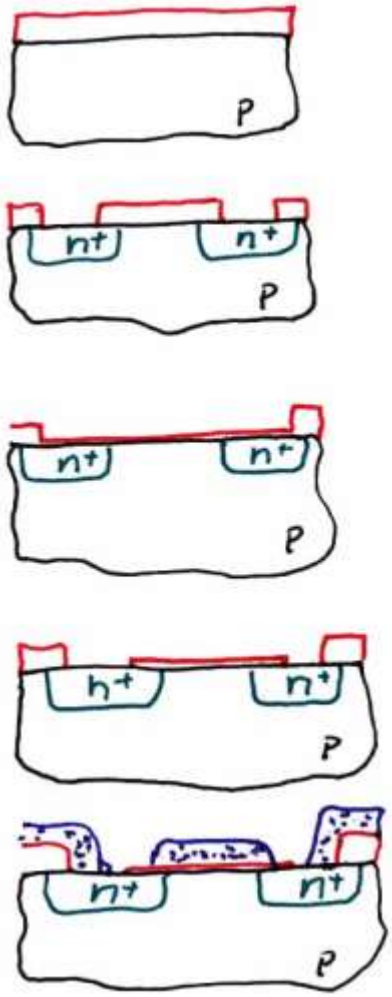

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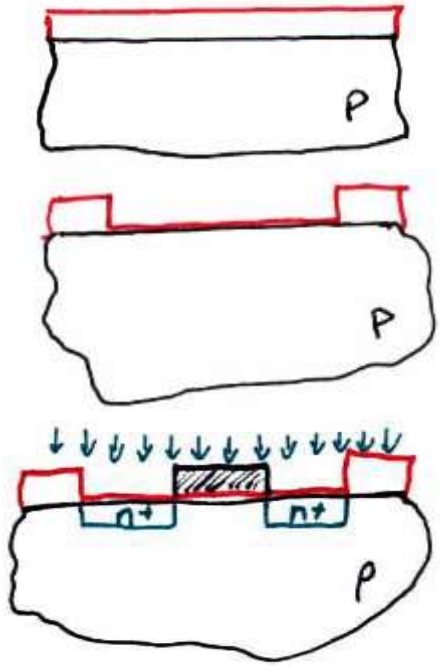

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Implant S/D

Innovation: Si-Gate Process

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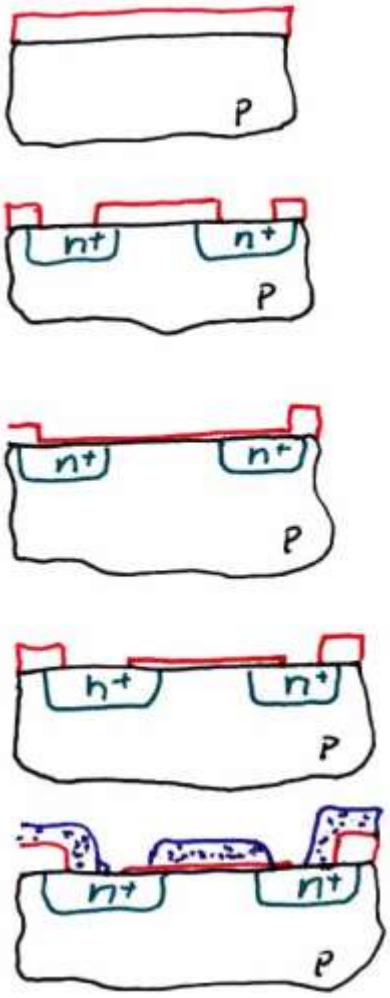

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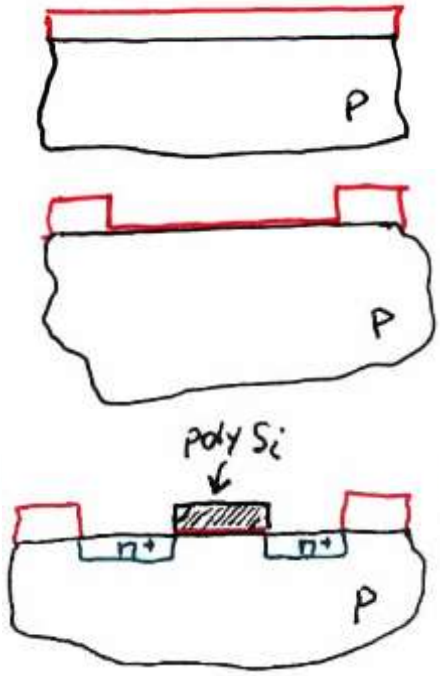

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Implant S/D

Etch back Gate ox

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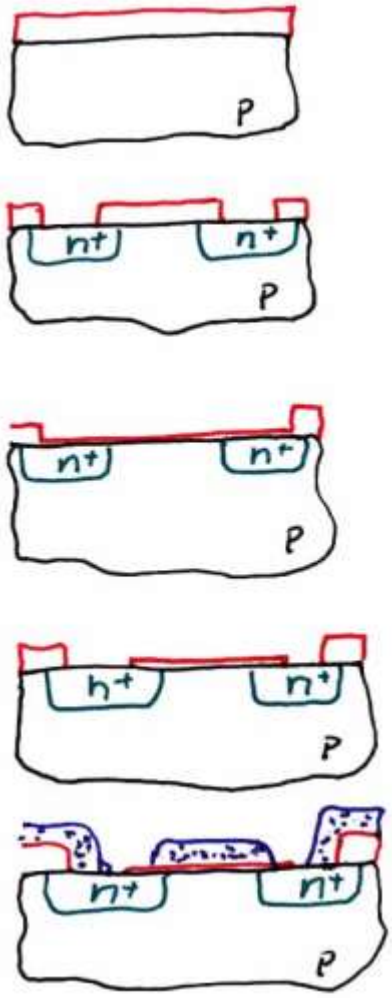

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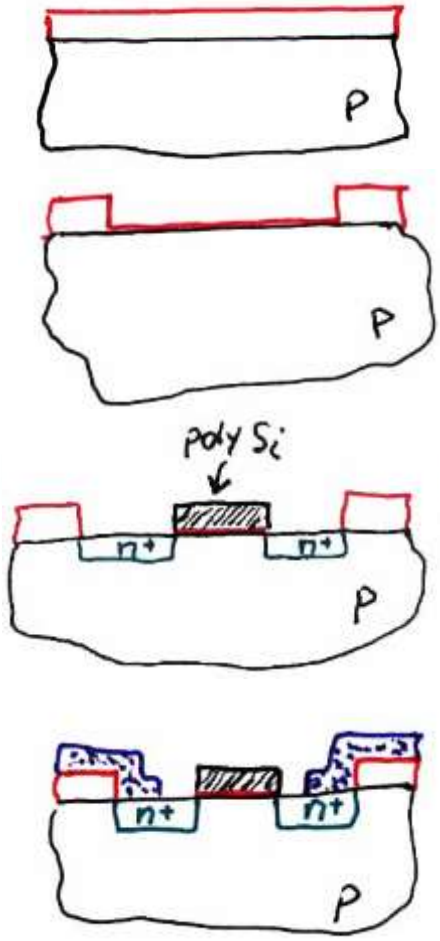

We start with the "field Oxidized" Wafer

define the Field ox and grow the Gate ox

define a poly Si Gate

Implant S/D

Etch back Gate ox

define Metal lines

Innovation: Si-Gate Process

The **Si Gate FET** is the first application of a class of process methods called

self aligned techniques

In this case: No mask required to define S/D!

☺ Miller capacities are minimized
☺ overlay requirements are relaxed
☺ one mask layer saved
☺ one additional wire level
(n⁺, poly Si, Alu)

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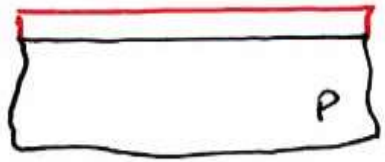

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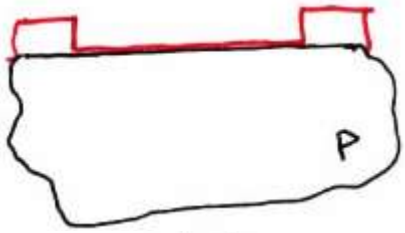
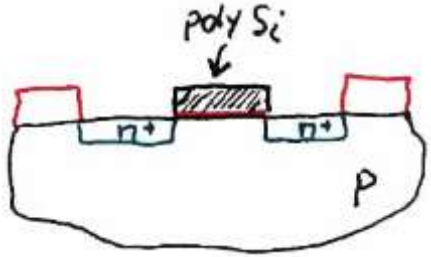


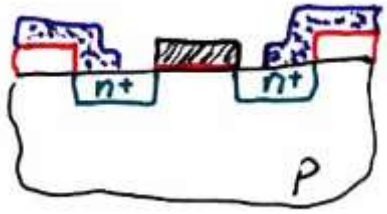
define the Field ox and grow the Gate ox

define a poly Si Gate



Implant S/D

Etch back Gate ox



define Metal lines

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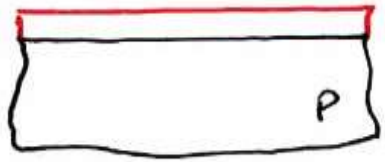

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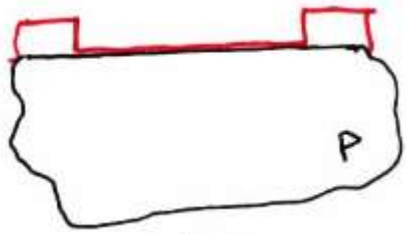

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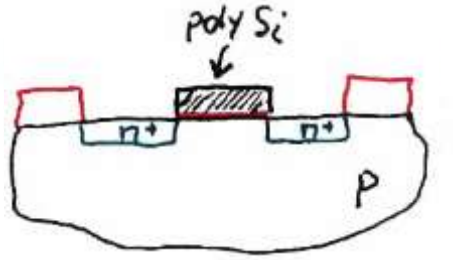

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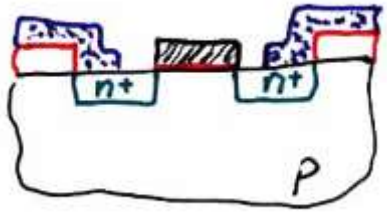

define Metal lines

Continue ⇨

"SCT_SS20_09.07" 02:36

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Summary

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

»Wissen schafft Brücken.«