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Lecture SCT2 - Process Integration

10. Web-based virtual Lecture: June 24 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here

"SCT_SS21_10.1" 18:13

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Outline

Review:
- SCT Basics
- MOS-Cap-CV
- MOS-FET
- Al-Gate FET
- SRAM production
- V_T dependencies
- E/D Logic
- Si Gate

Today: Further self alignment

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

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"SCT_SS20_10.2" 59:08

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SC-Basics

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Remember? Parasitic FET's

What's a parasitic FET?

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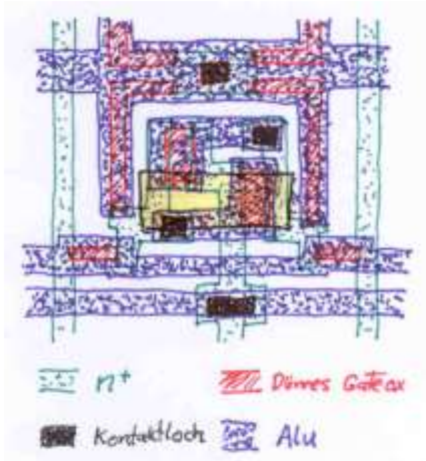
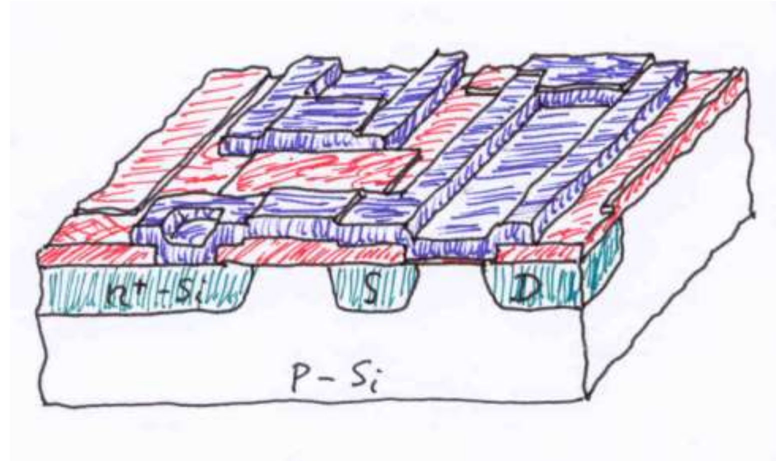
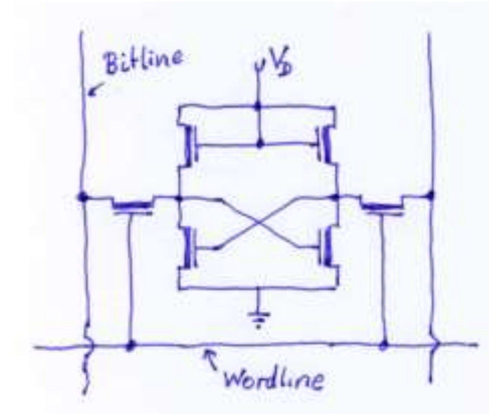
What's a parasitic FET?

Remember our SRAM cell:







Remember? Parasitic FET's

What's a parasitic FET?

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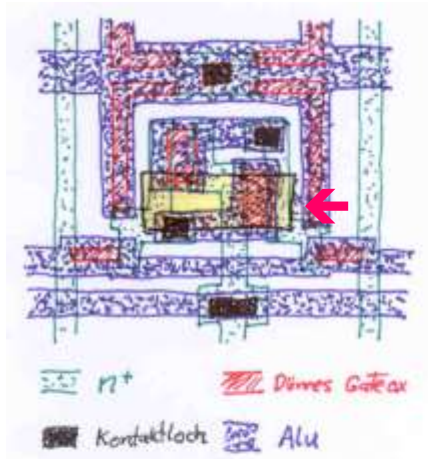
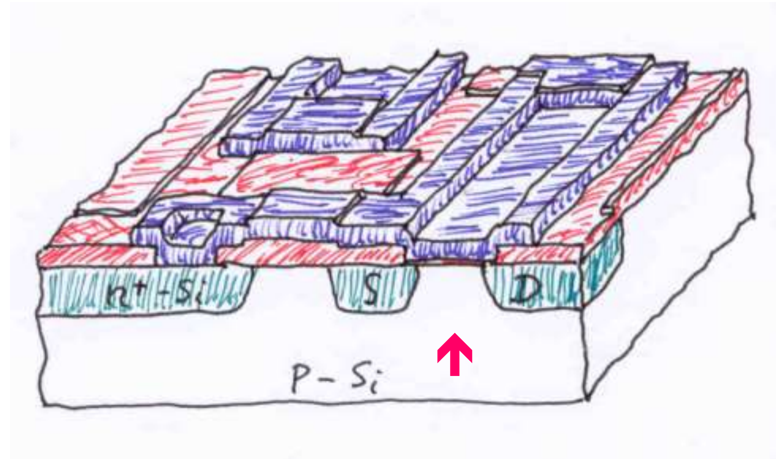
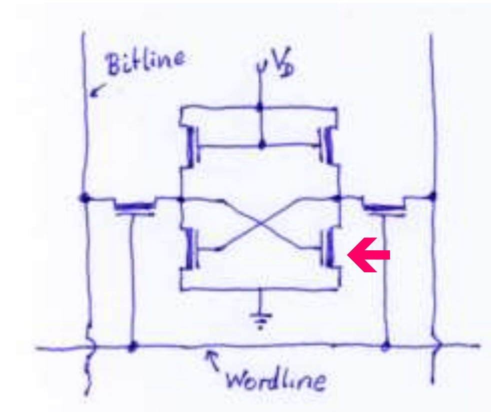




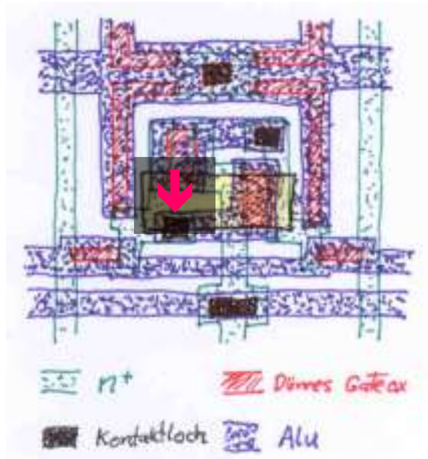


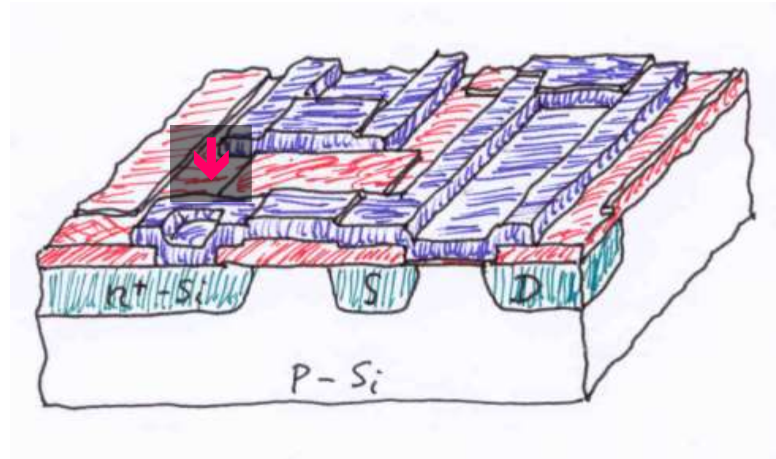
A regular FET is the switching transistor shown in the different pictures and consist of the n⁺ Source, the p-substrate and the n⁺ Drain region, the substrate region is covered with the thin oxide and the gate electrode.

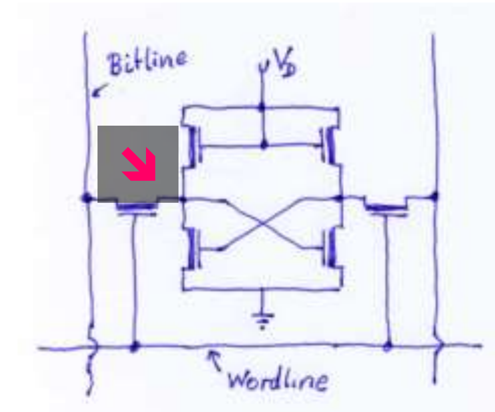
Remember? Parasitic FET's

What's a parasitic FET?

Remember our SRAM cell:







The Gate-line runs over the fieldox to the left and connects to the Drain of the left switching transitor resp. the Source of the left load transistor.

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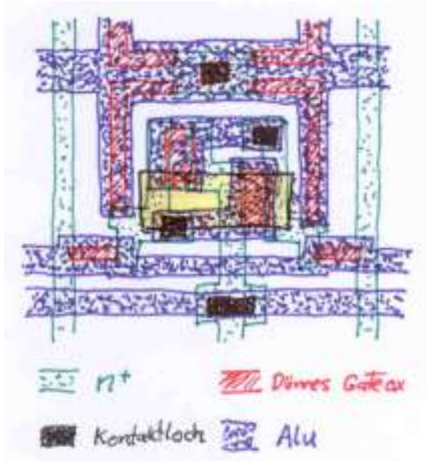
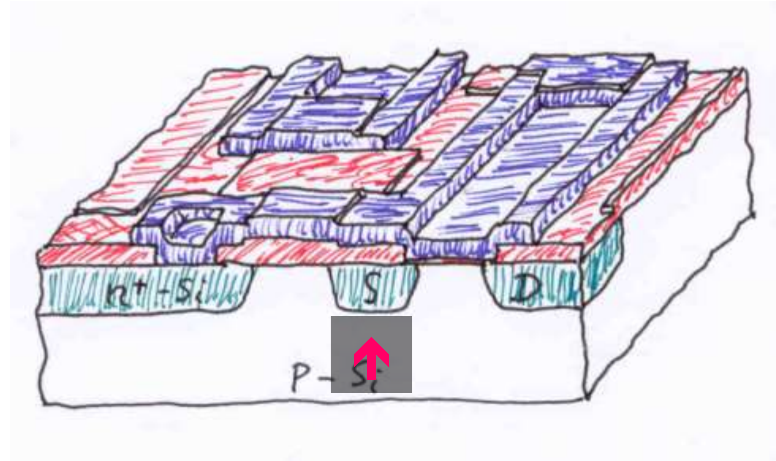
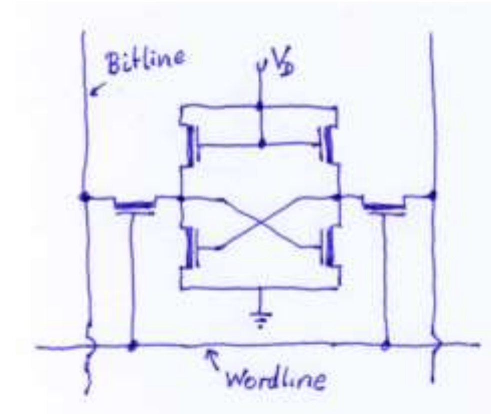
Remember? Parasitic FET's

What's a parasitic FET?

Remember our SRAM cell:







We can think of the source,

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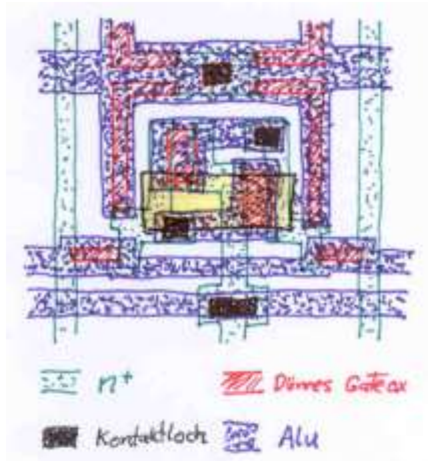
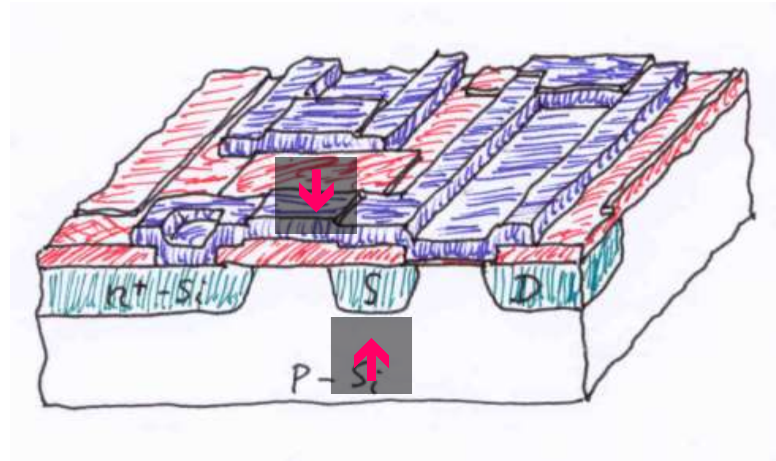
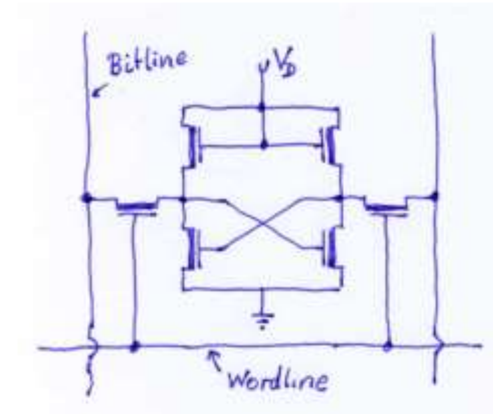
Remember? Parasitic FET's

What's a parasitic FET?

Remember our SRAM cell:







We can think of the source, the Gate over the fieldox,

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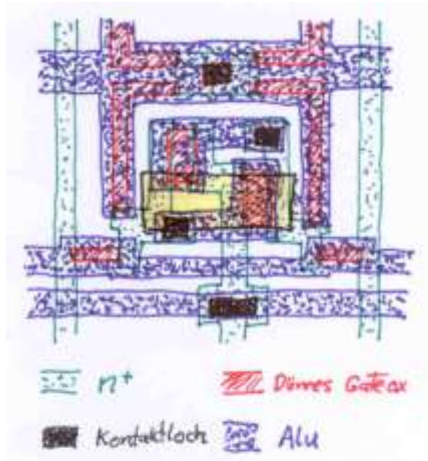
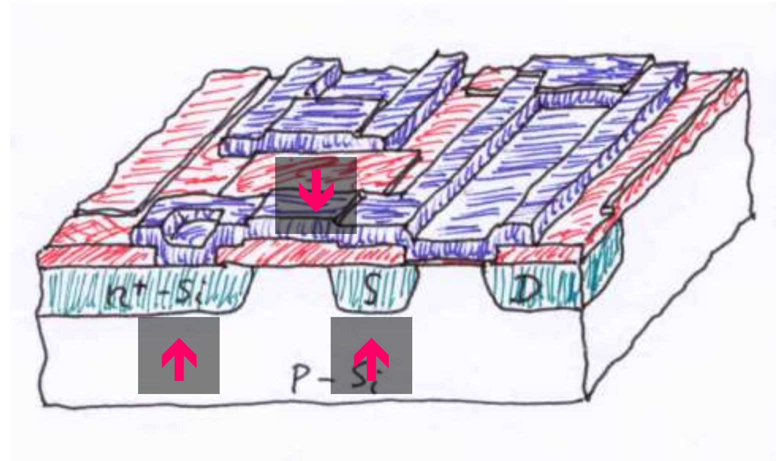
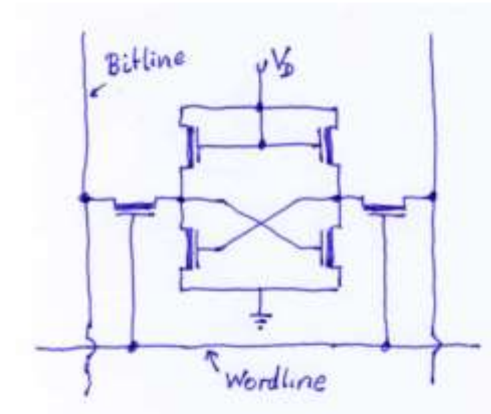
Remember? Parasitic FET's

What's a parasitic FET?

Remember our SRAM cell:







We can think of the source, the Gate over the fieldox, and the n^+ line

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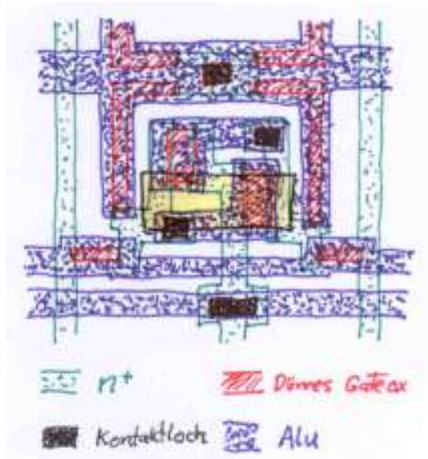
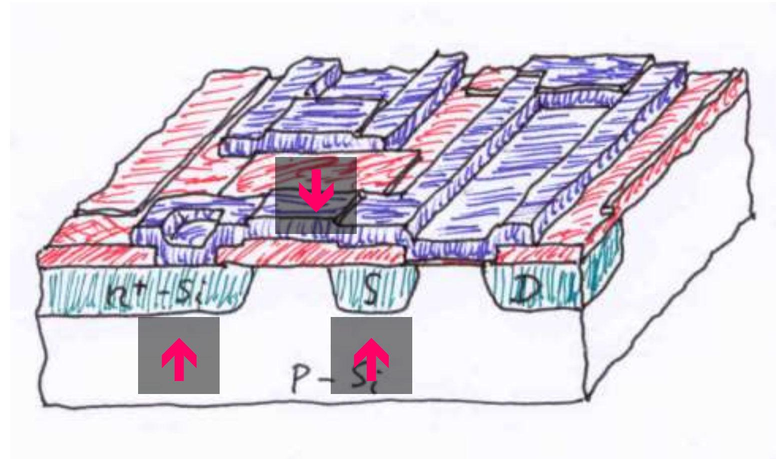
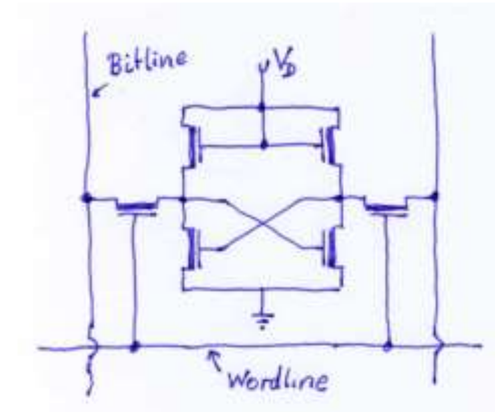
Remember? Parasitic FET's

What's a parasitic FET?

Remember our SRAM cell:





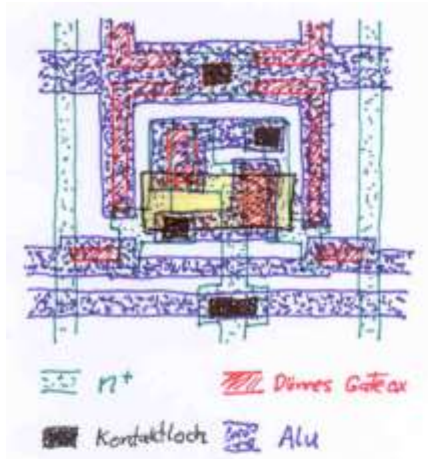


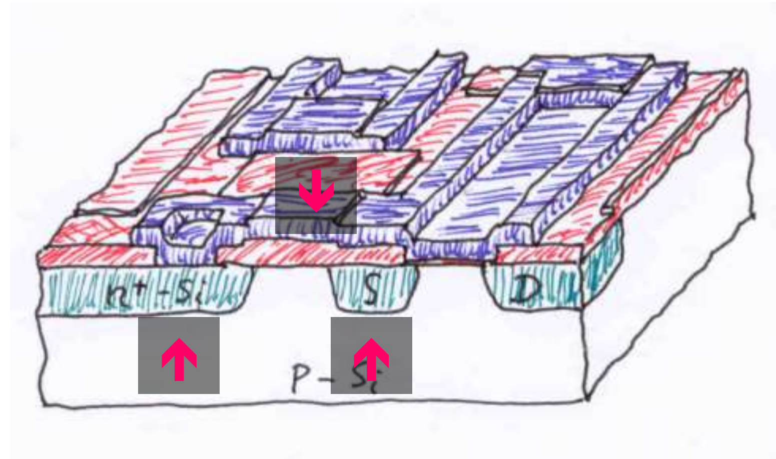
We can think of the source, the Gate over the fieldox, and the n^+ line as a further MOS FET, which has a high threshold voltage due to the large thickness of the fieldox.

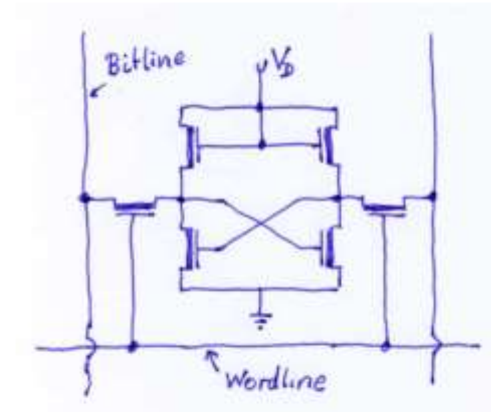
Remember? Parasitic FET's

What's a parasitic FET?

Remember our SRAM cell:







We can think of the source, the Gate over the fieldox, and the n^+ line as a further MOS FET, which has a high threshold voltage due to the large thickness of the fieldox.

This FET is called parasitic transistor. It might unintentionally connect any n^+ region where Gate lines run over the fieldox. To avoid this, the fieldox thickness has to be as large as possible.

Remember? Parasitic FET's

What's a parasitic FET?

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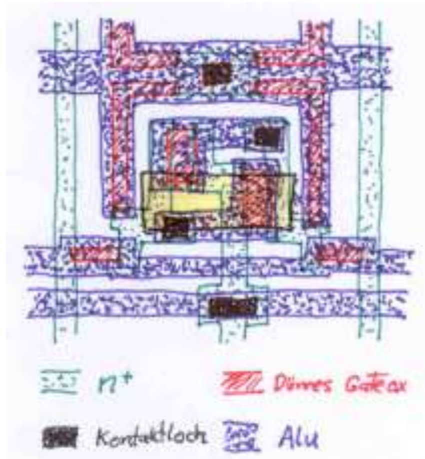

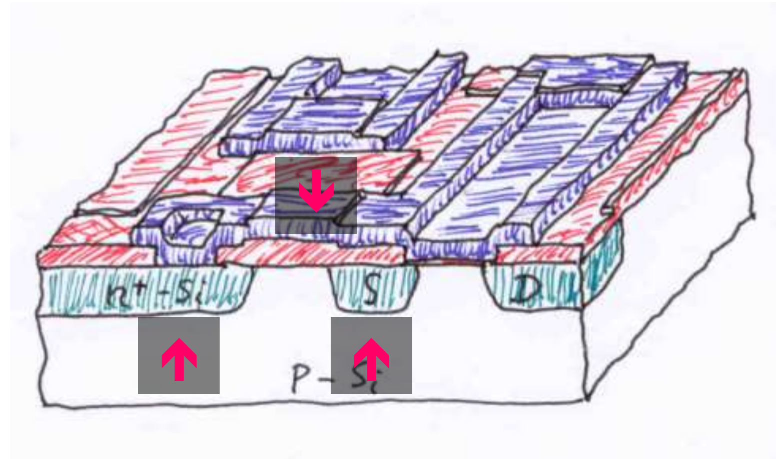

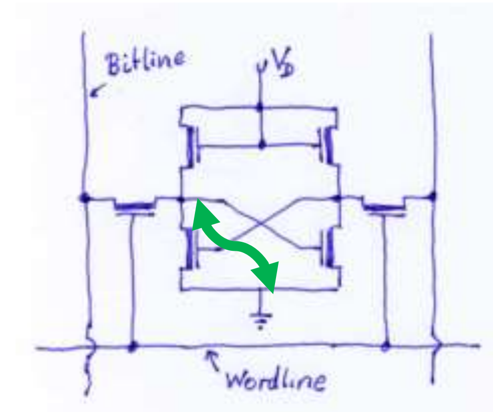

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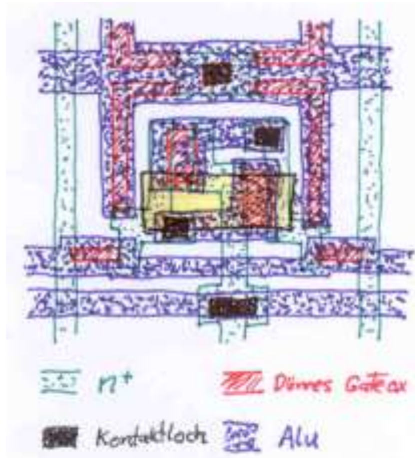

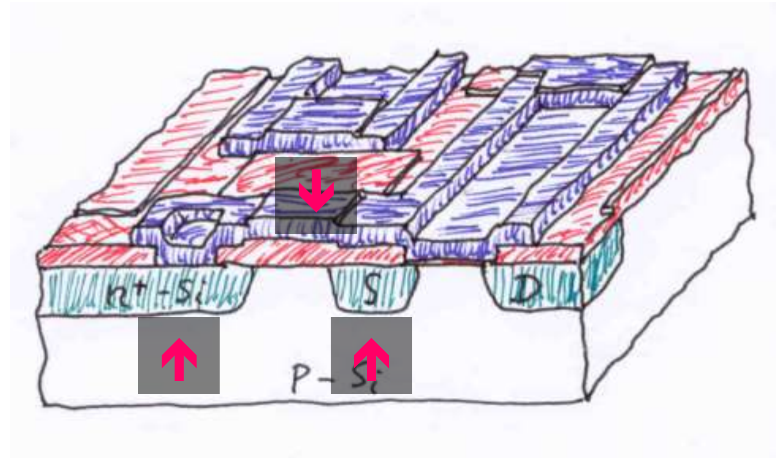

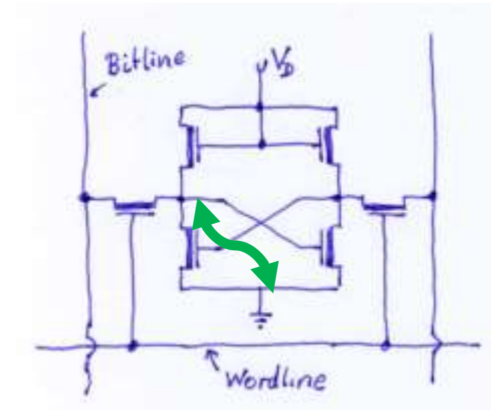

We can think of the source, the Gate over the fieldox, and the n+ line as a further MOS FET, which has a high threshold voltage due to the large thickness of the fieldox.

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$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A (2\Phi_F + V_{SB})} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

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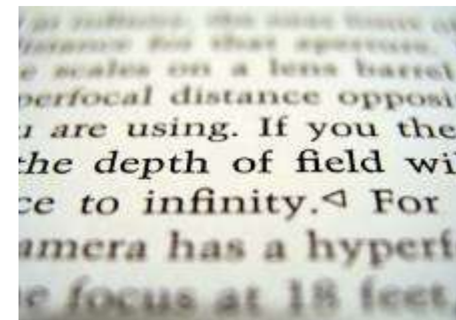
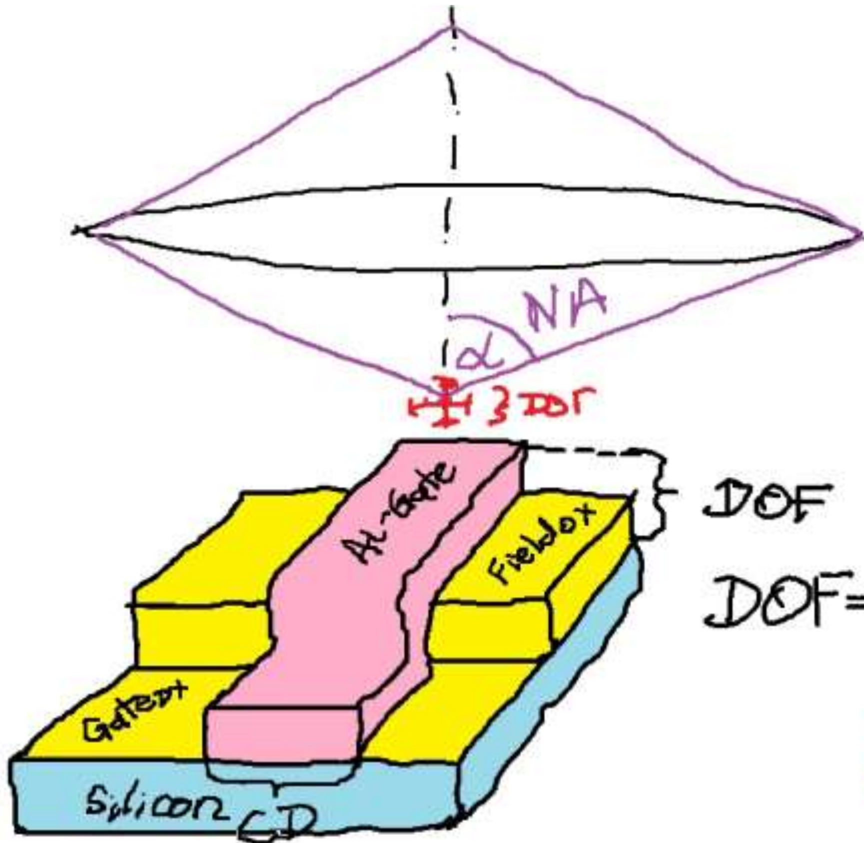
Challenges associated with large d_{fox} (field oxide thickness)

- Lithography on large topography

$CD=k_1\,\lambda/NA$ and $DOF=k_2\,\lambda/NA^2$

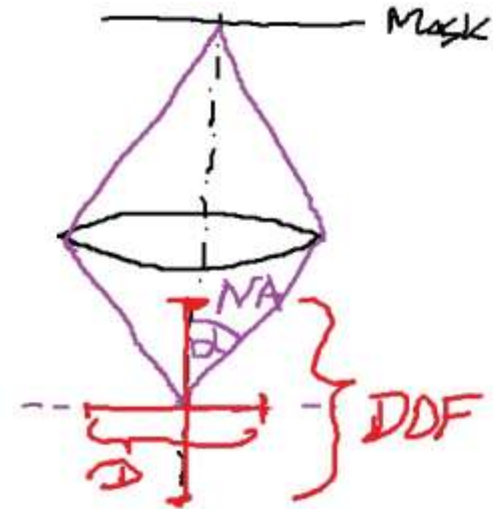




DOF

$$DOF = k_2 \frac{\lambda}{NA^2}$$

$$CD = k_1 \frac{\lambda}{NA}$$



Small CD (Gate L) requires low surface corrugation!

Challenges associated with large d_{fox} (field oxide thickness)

- Lithography on large topography
  $CD=k_1 \lambda/NA$ and $DOF=k_2 \lambda/NA^2$

- Step coverage of the metal layer

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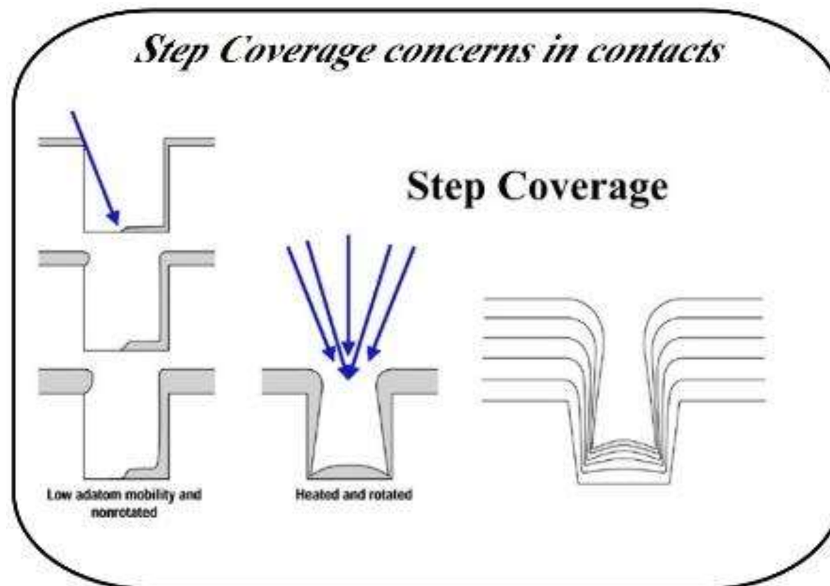
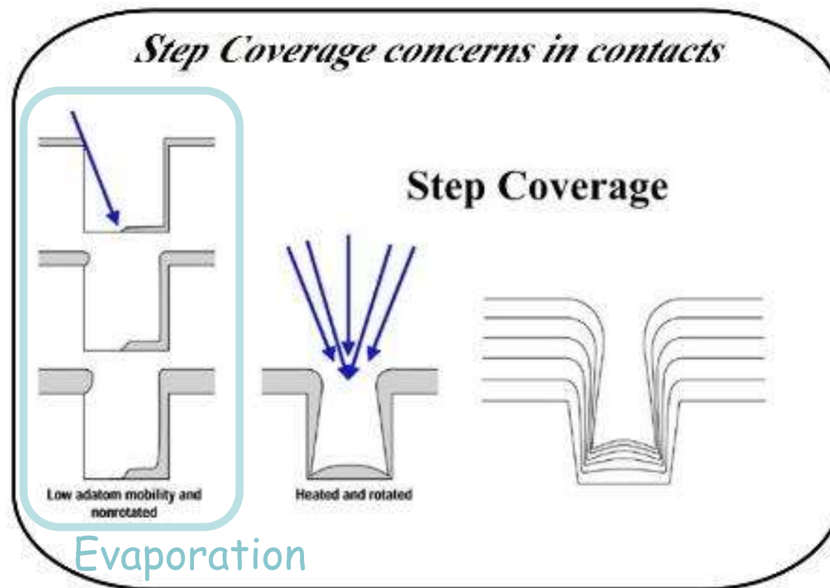
Concerns with PVD



+ Inherent Uniformity Issues!

Concerns with PVD



+ Inherent Uniformity Issues!

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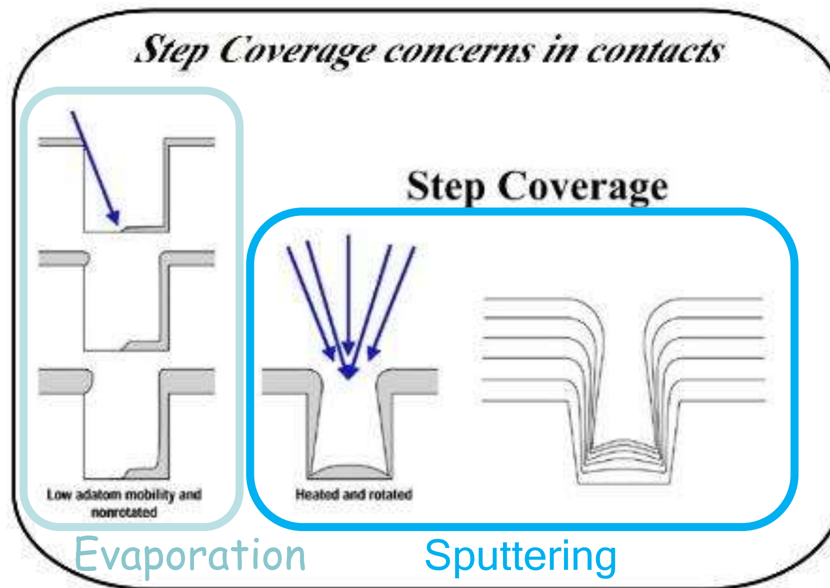
Concerns with PVD



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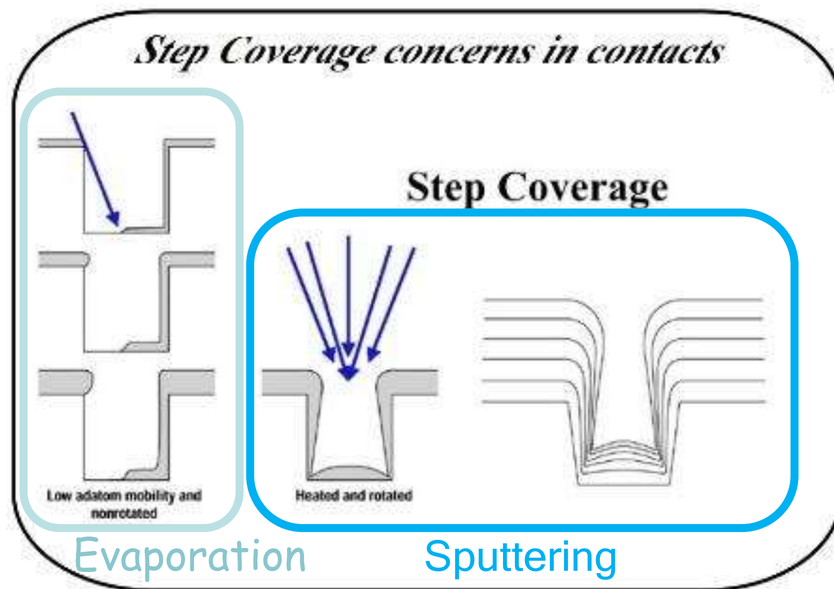
Concerns with PVD



EE143 – Ali Javey

+ Inherent Uniformity Issues!

Concerns with CVD

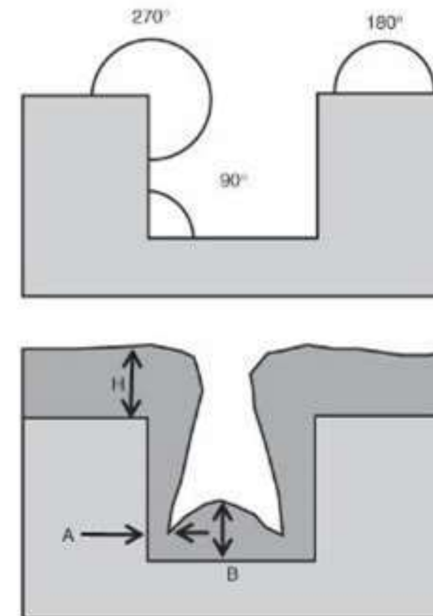


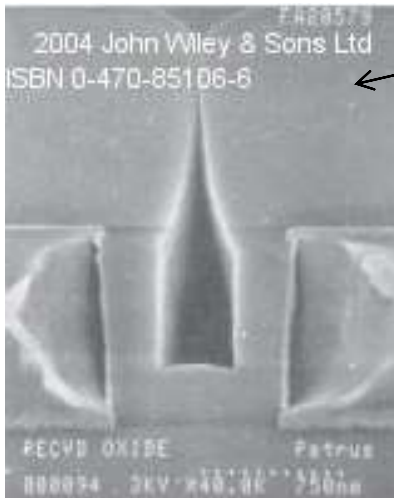
Figure 5-15

Top, arrival angles of depositing species at different positions; bottom, step coverage, A/H, and bottom coverage, B/H.

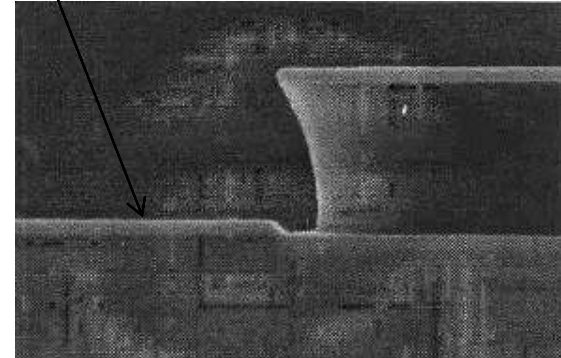
Introduction to microfabrication / Sami Franssila
ISBN 0-470-85106-6

Question:

Which deposition technique was used to make the structure below?



b)

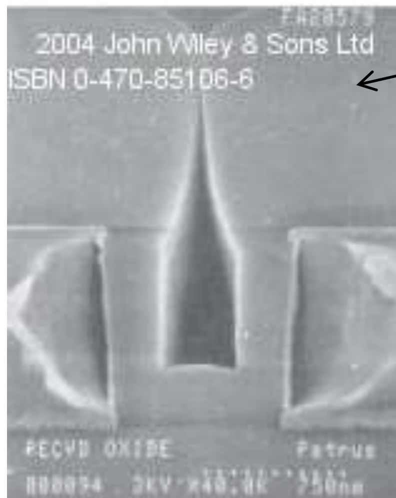


c)

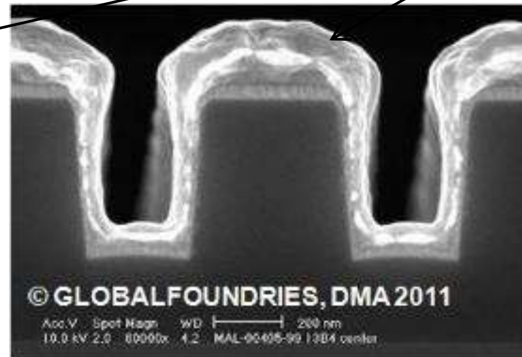
a)

Question:

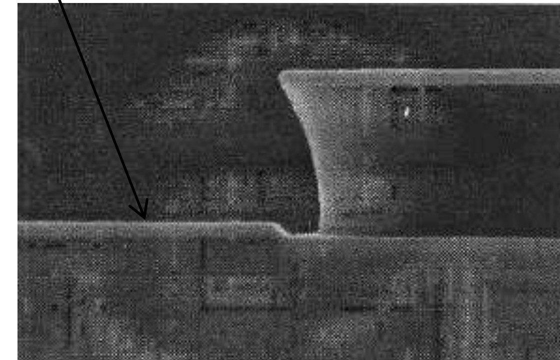
Which deposition technique was used to make the structure below?



a)



b)



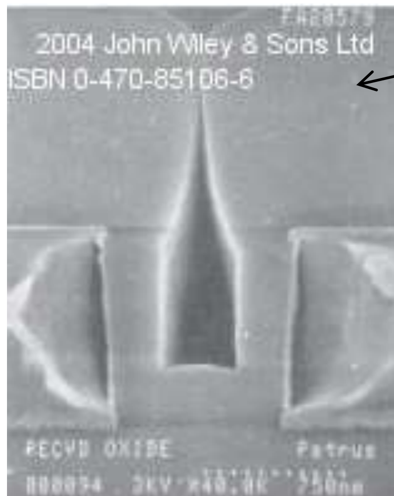
c)

Choices are:

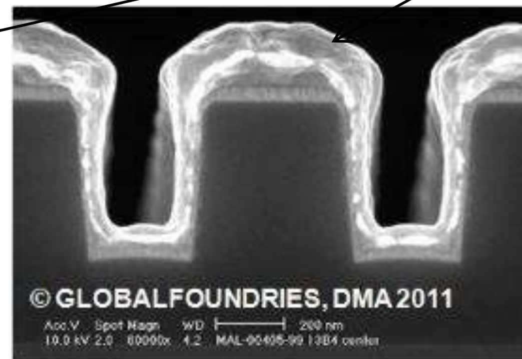
- PVD – evaporation,
- (PE)CVD,
- PVD - Sputtering

Question:

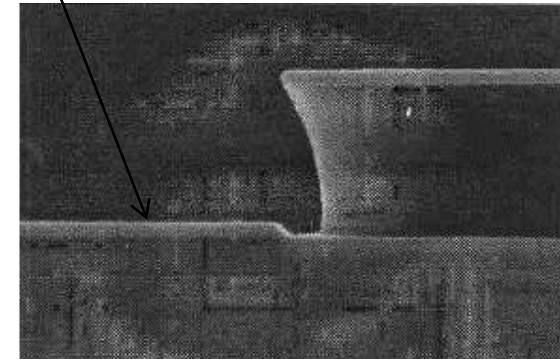
Which deposition technique was used to make the structure below?



a)



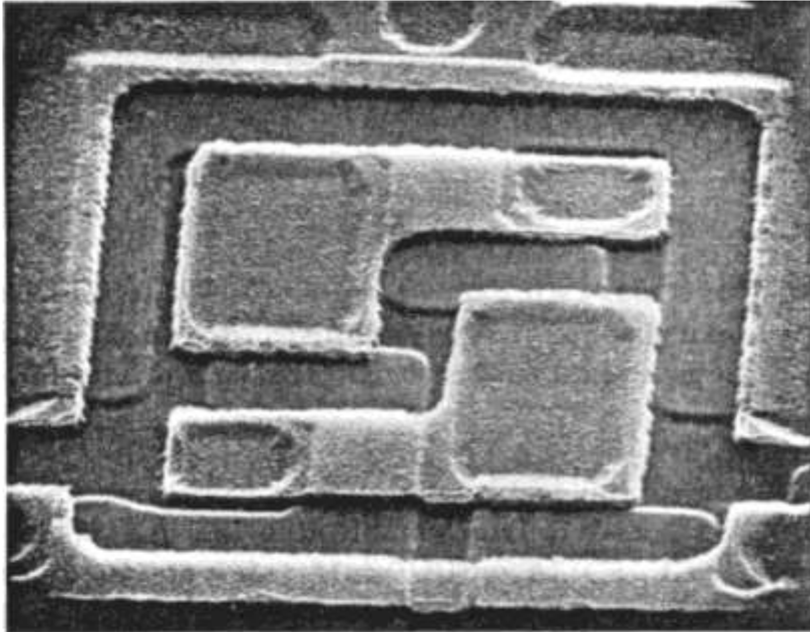
b)



c)

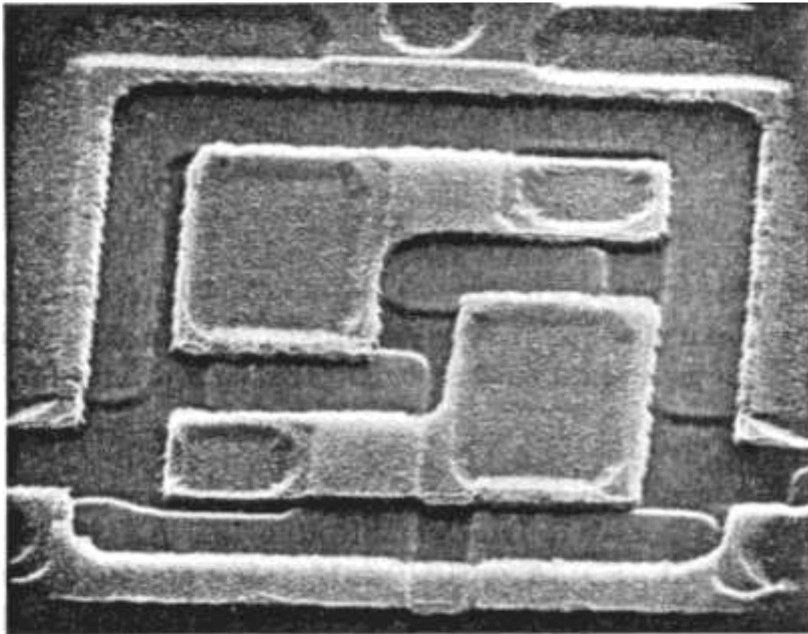
Choices are:

c) **PVD – evaporation,**
a) **(PE)CVD,**
b) **PVD - Sputtering**

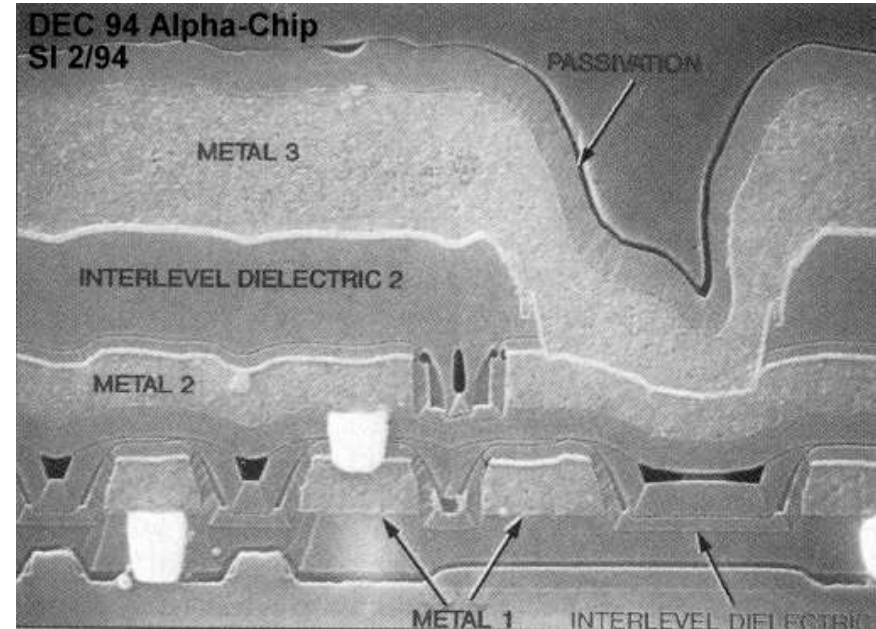


1 K Memory, IBM 1970

Evolution of the IC-Architecture: 2D → 3D

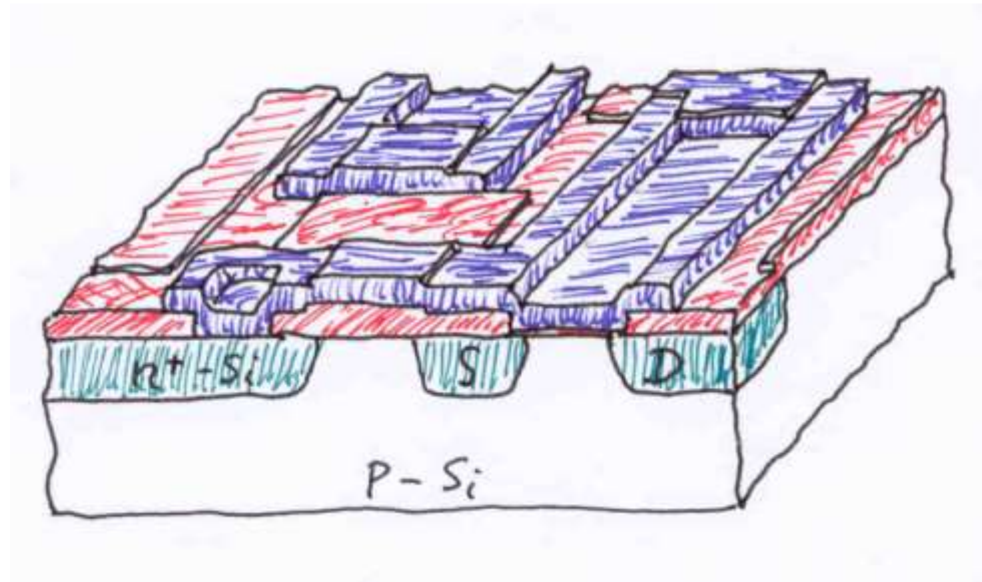


1 K Memory, IBM 1970



MPU „Alpha“, DEC 1994

How to avoid parasitic FETs



$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

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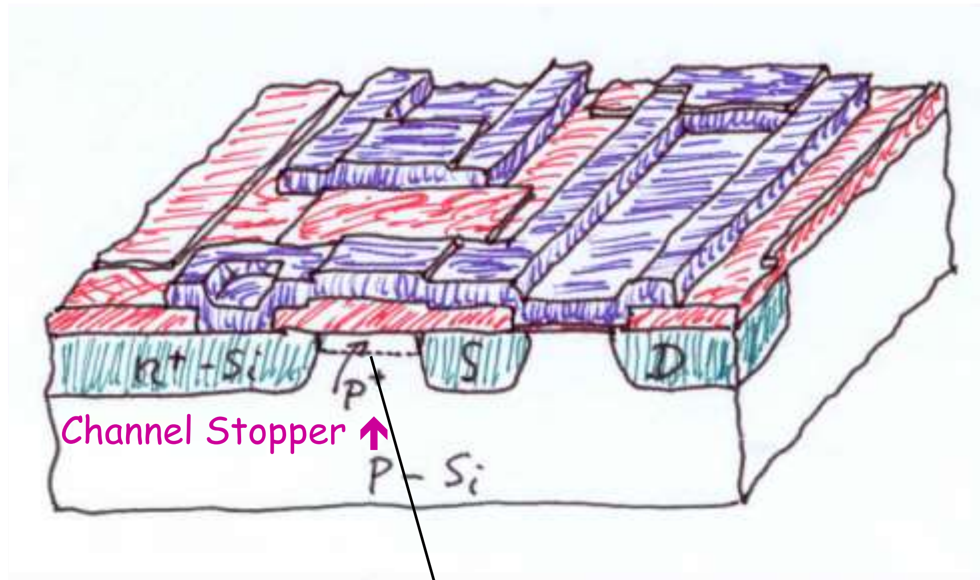
How to avoid parasitic FETs Innovation: 3.2 a Channel Stop

To further relax this problem, the p-substrate underneath the fieldox can be doped to p^+. This shifts V_T of the parasitic transistor to higher V_G and insures a safer operation.



This additional doping is called "channel stopper". By applying the "channel stopper", the threshold of the parasitic transistor can not be reached under normal operation.

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

How to avoid parasitic FETs Innovation: 3.2 a Channel Stop

To further relax this problem, the p-substrate underneath the fieldox can be doped to p⁺. This shifts V_T of the parasitic transistor to higher V_G and insures a safer operation.

Shit! Additional Mask Layer required!

This additional doping is called "channel stopper". By applying the "channel stopper", the threshold of the parasitic transistor can not be reached under normal operation.

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

How to avoid parasitic FETs Innovation: 3.2 a Channel Stop

To further relax this problem, the p-substrate underneath the fieldox can be doped to p^+. This shifts V_T of the parasitic transistor to higher V_G and insures a safer operation.

Shit! Additional Mask Layer required!

True ?

This additional doping is called "channel stopper". By applying the "channel stopper", the threshold of the parasitic transistor can not be reached under normal operation.

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

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3.2 LOCOS Process

A “self adjusting” way to combine the growth of the fieldox with the masking of the “Channel Stopper” is the so called LOCOS process which stands for **L**o**c**al **O**xidation **o**f **S**ilicon. With the following process flow:

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3.2 LOCOS Process

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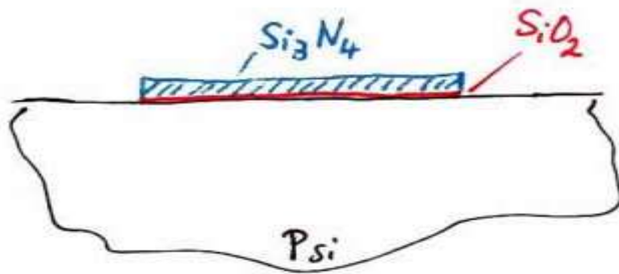
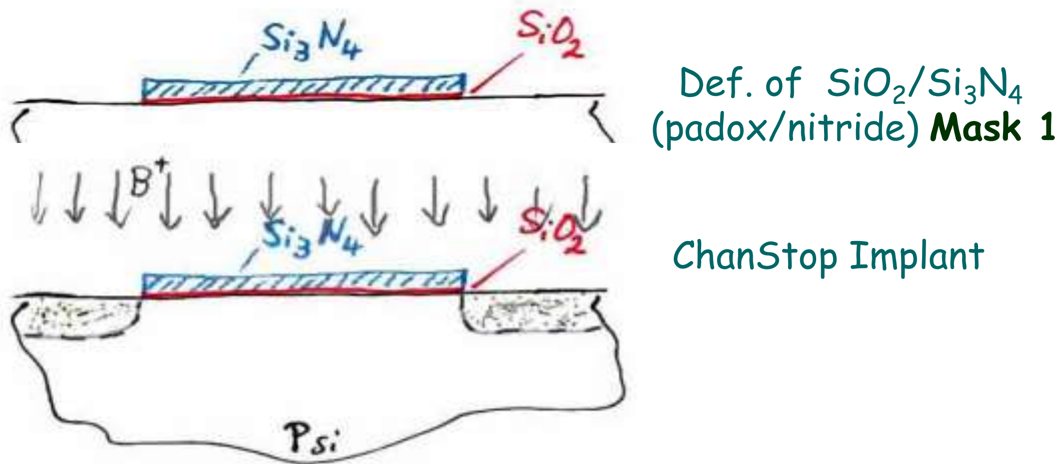


Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

3.2 LOCOS Process

A “self adjusting” way to combine the growth of the fieldox with the masking of the “Channel Stopper” is the so called LOCOS process which stands for **L**oc**a**l **O**xidation **o**f **S**ilicon. With the following process flow:



Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

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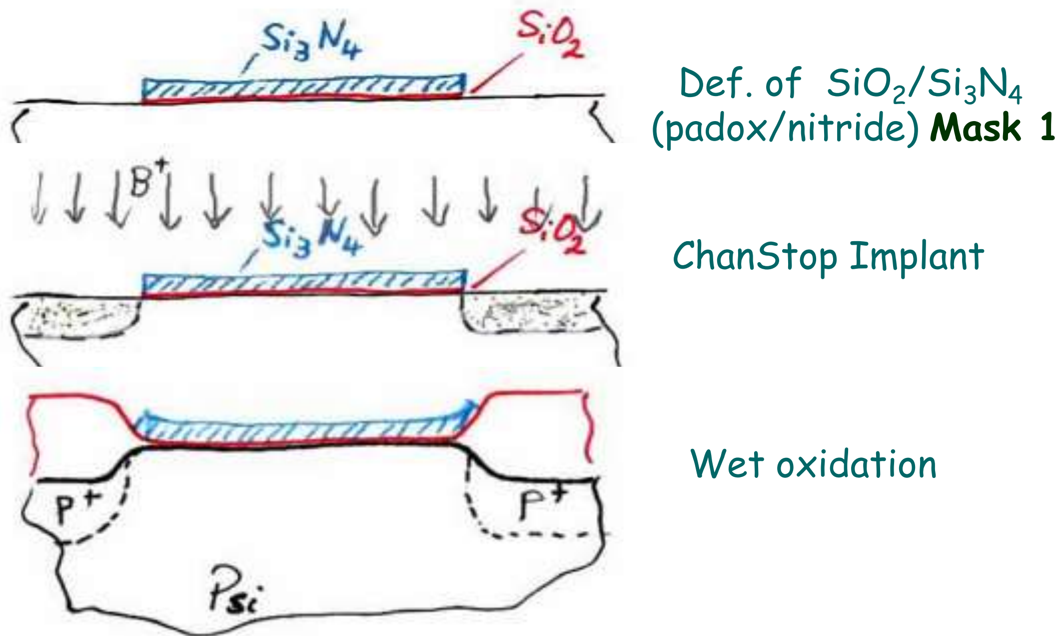

Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

Wet oxidation

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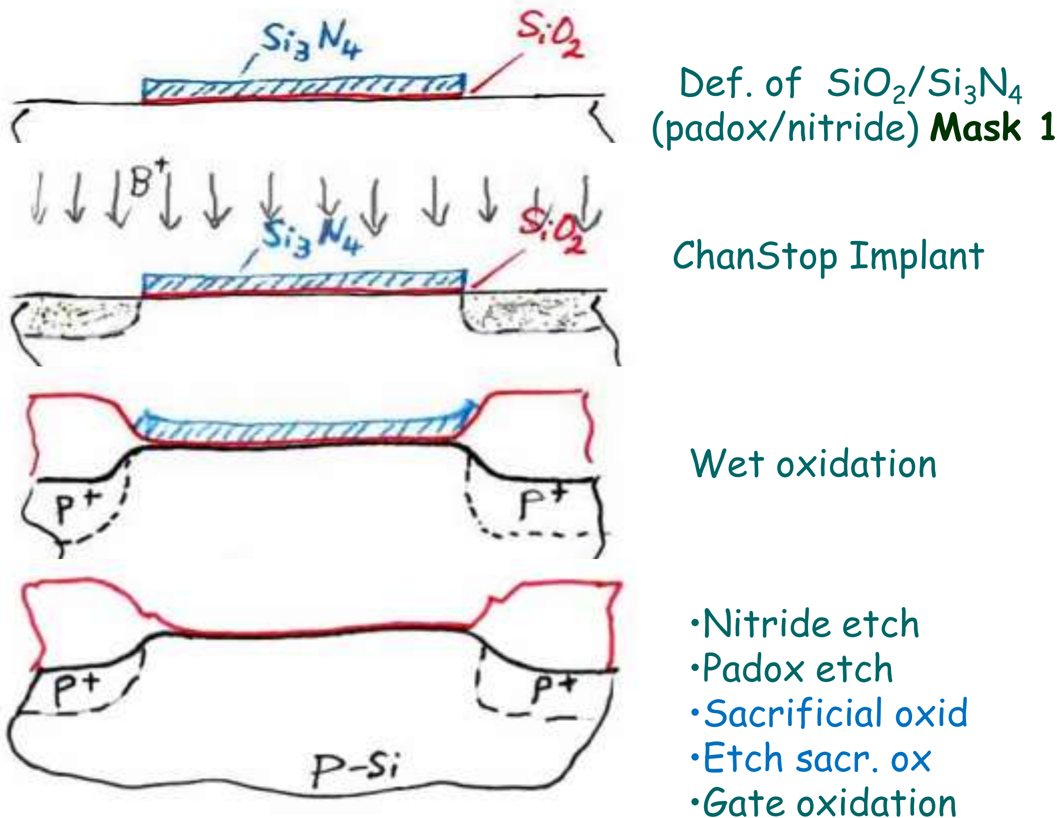
3.2 LOCOS Process

A "self adjusting" way to combine the growth of the fieldox with the masking of the "Channel Stopper" is the so called LOCOS process which stands for **L**ocal **O**xidation **of** **S**ilicon. With the following process flow:



Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

Wet oxidation

- Nitride etch
- Padox etch
- Sacrificial oxid
- Etch sacr. ox
- Gate oxidation

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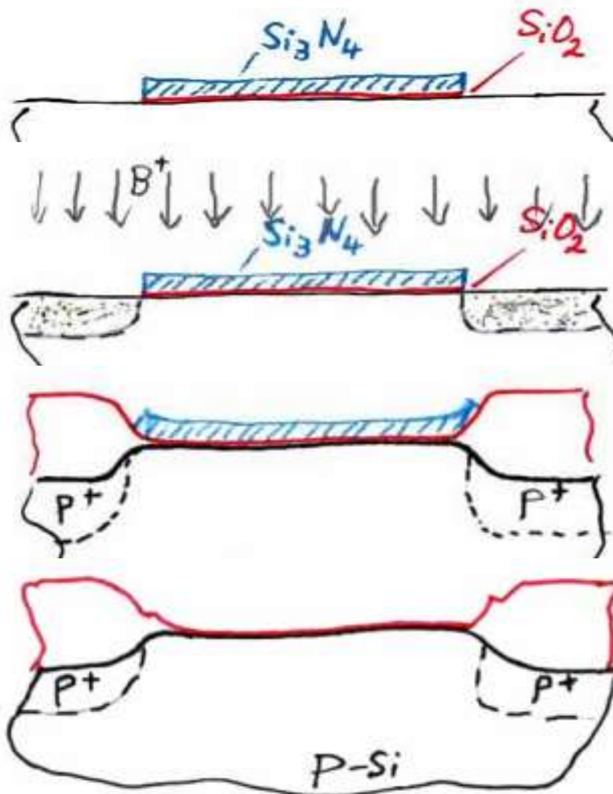
3.2 LOCOS Process

A "self adjusting" way to combine the growth of the fieldox with the masking of the "Channel Stopper" is the so called LOCOS process which stands for **L**ocal **O**xidation **o**f **S**ilicon. With the following process flow:

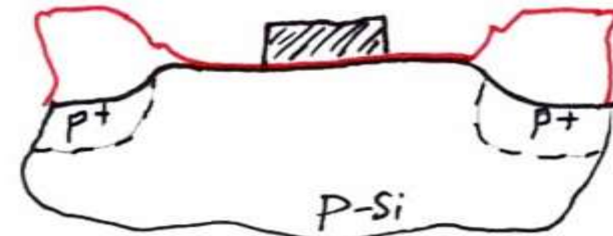


Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

Wet oxidation

- Nitride etch
- Padox etch
- Sacrificial oxid
- Etch sacr. ox
- Gate oxidation



Def. of poly Si Gate
Mask 2

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3.2 LOCOS Process

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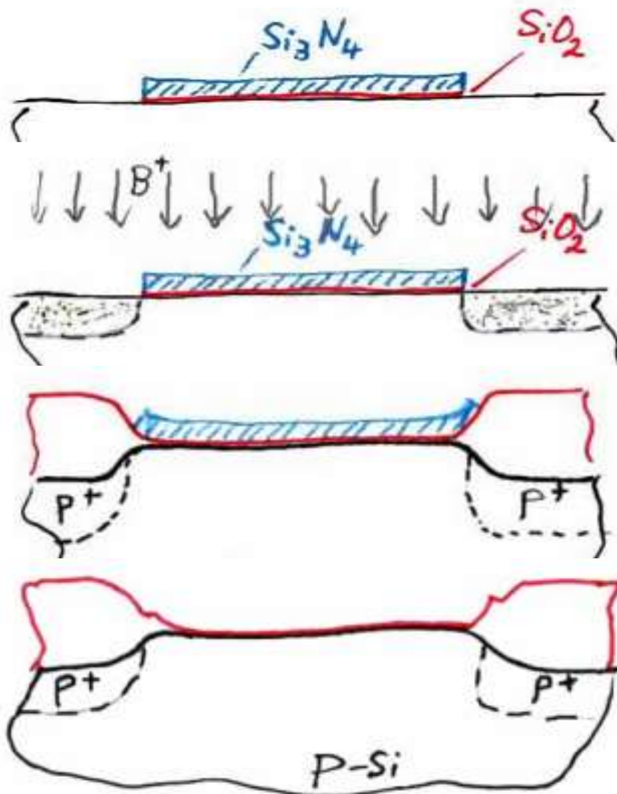
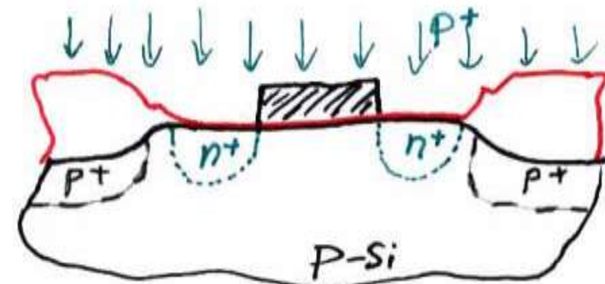


Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

Wet oxidation

- Nitride etch
- Padox etch
- Sacrificial oxid
- Etch sacr. ox
- Gate oxidation



S/D Implant

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3.2 LOCOS Process

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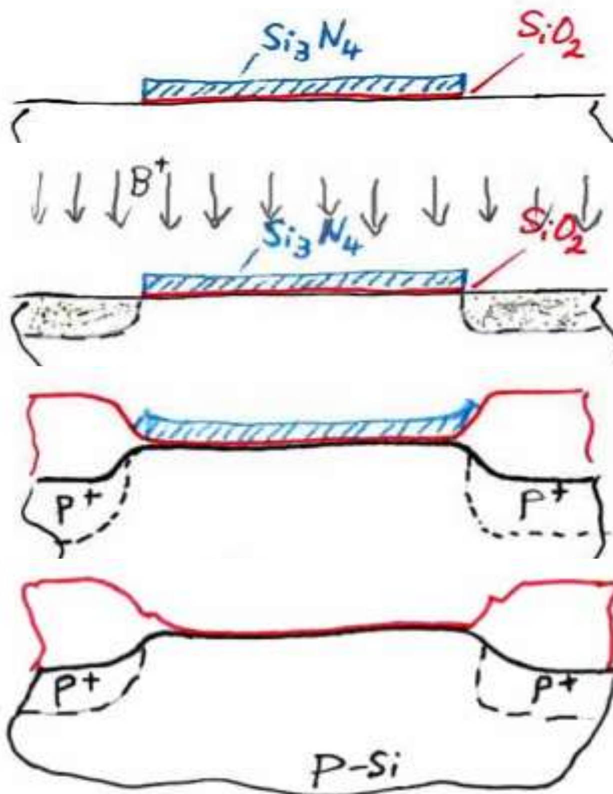

Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

Wet oxidation

- Nitride etch
- Padox etch
- Sacrificial oxid
- Etch sacr. ox
- Gate oxidation

and so on ...

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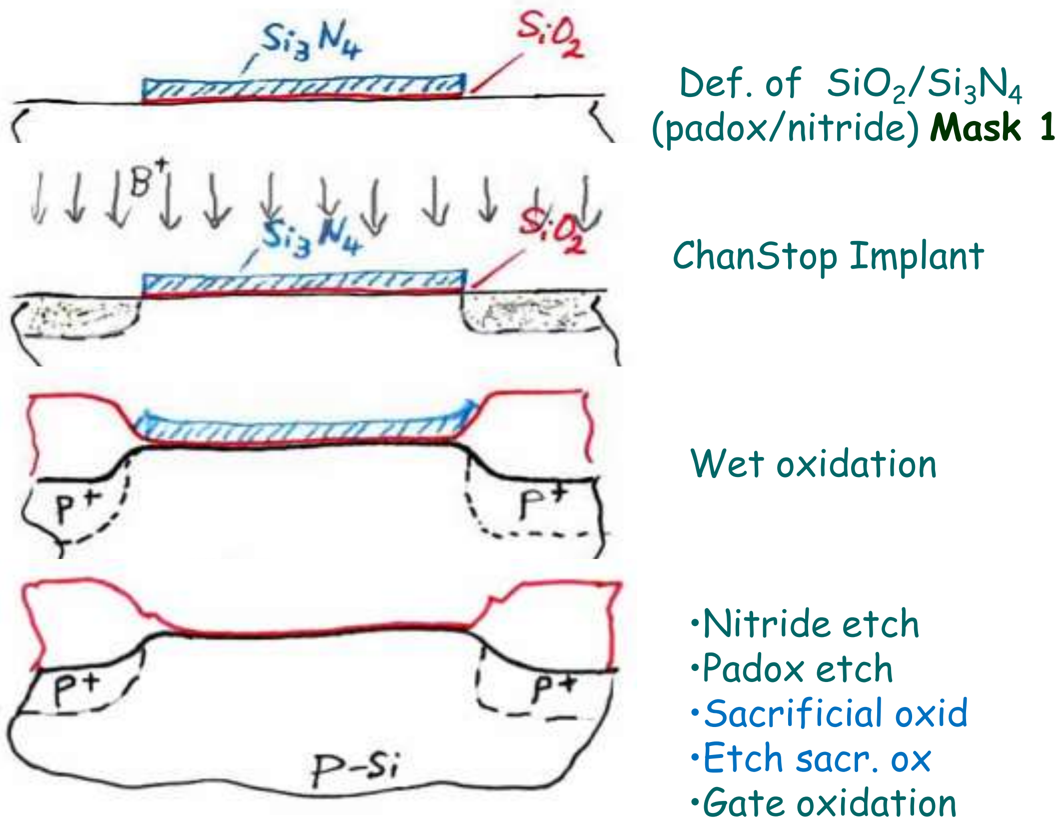
3.2 LOCOS Process

A “self adjusting” way to combine the growth of the fieldox with the masking of the “Channel Stopper” is the so called LOCOS process which stands for **L**ocal **O**xidation **o**f **S**ilicon. With the following process flow:

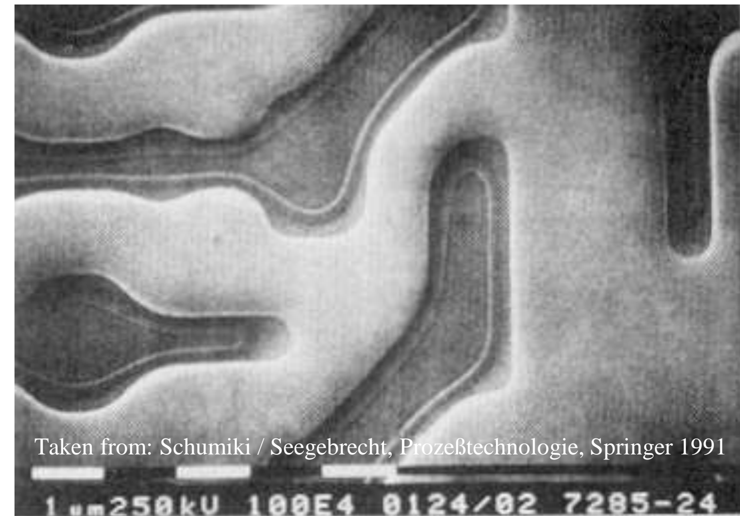


Def. of SiO_2/Si_3N_4 (padox/nitride) **Mask 1**

ChanStop Implant

Wet oxidation

- Nitride etch
- Padox etch
- Sacrificial oxid
- Etch sacr. ox
- Gate oxidation



Taken from: Schumiki / Seegebrecht, Prozeßtechnologie, Springer 1991

☺ **Self adjusted chanstop**

☺ **Fieldox can be thinner**

☺ **Only half of Fieldox thickness contributes to surface topography**

=> reduced DOF! or

=> smaller CD!

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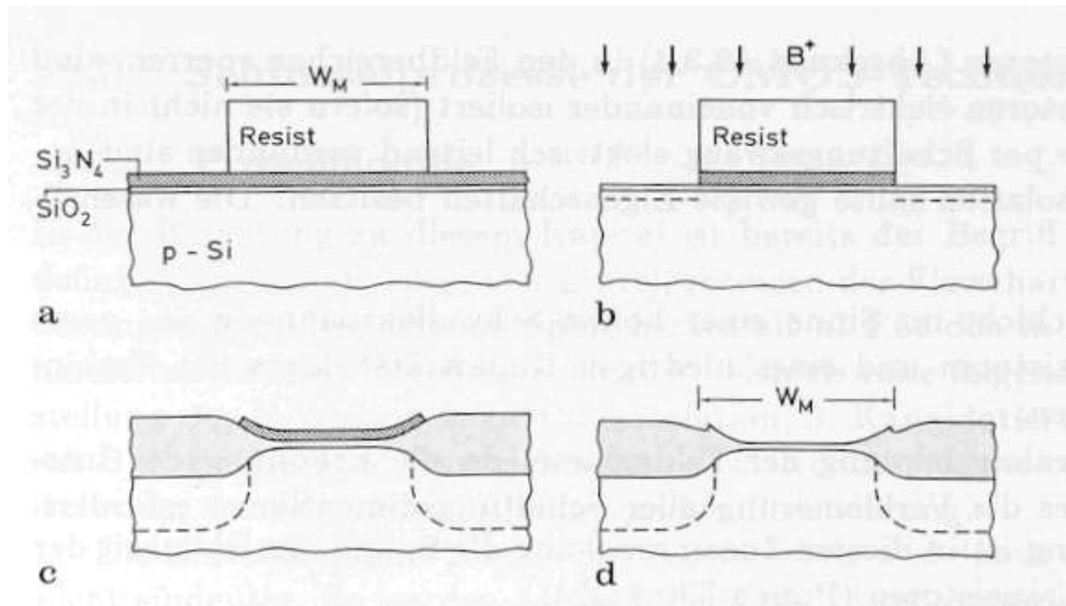
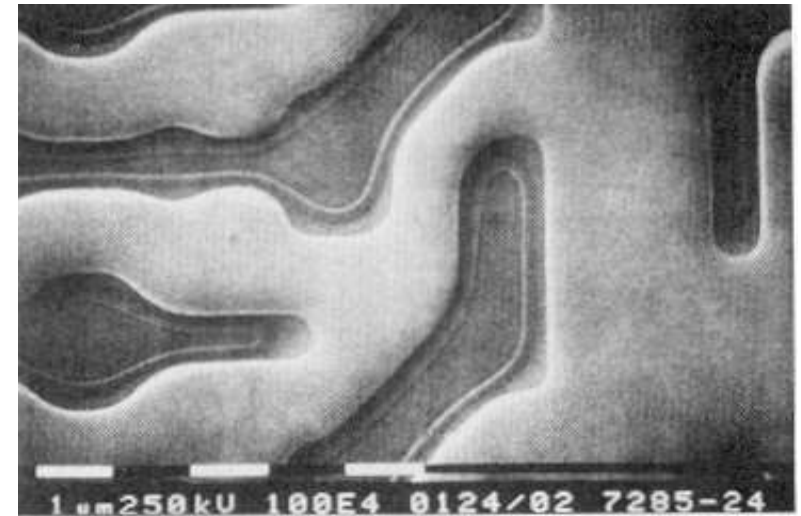
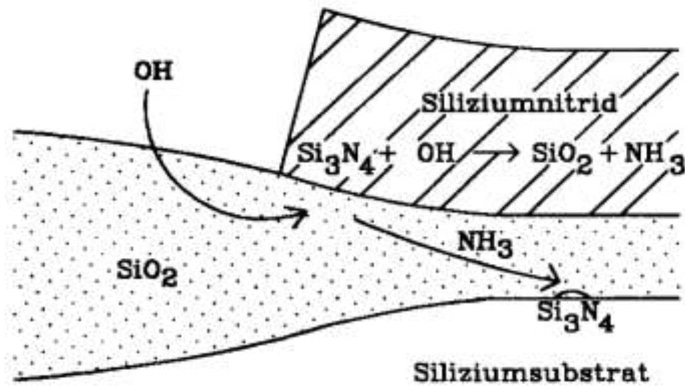
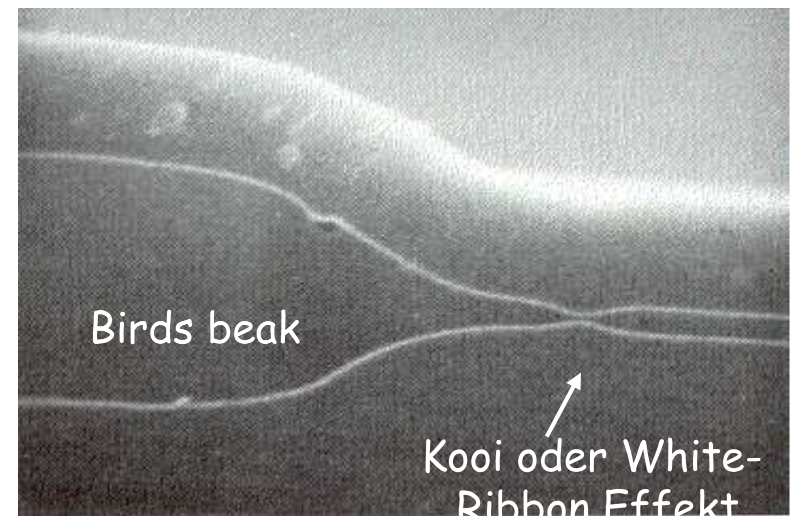
LOCOS (LOCal Oxidation Process)









Reason for sacrificial oxidation: Si_3N_4 residue must be removed before gate oxidation!

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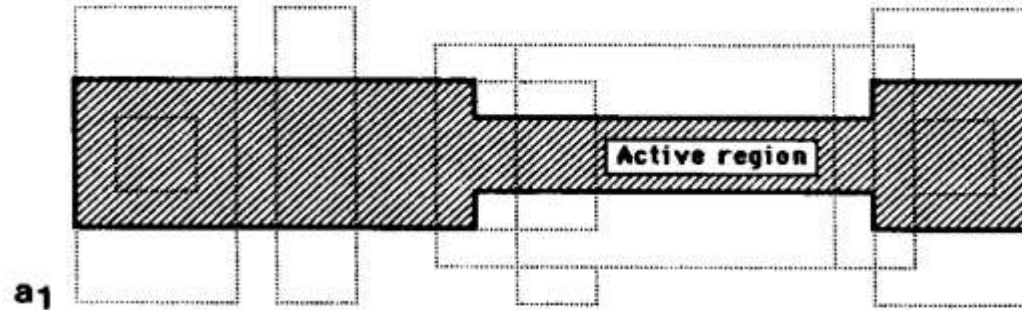
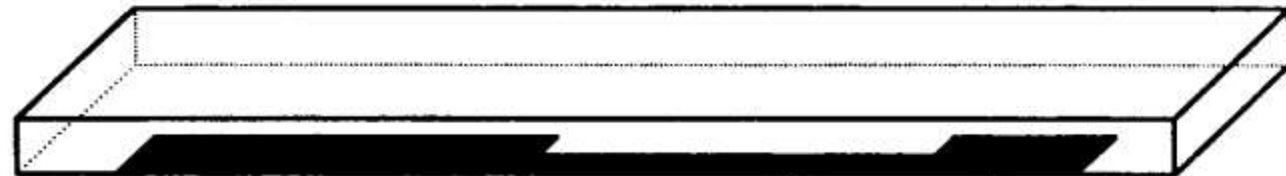
Example:
Integration Scheme of an ED Inverter in Si-Gate / LOCOS technique

3.2.1. E/D Si-Gate LOCOS Inverter Process

Mask1/Layout:

Def. Active Region



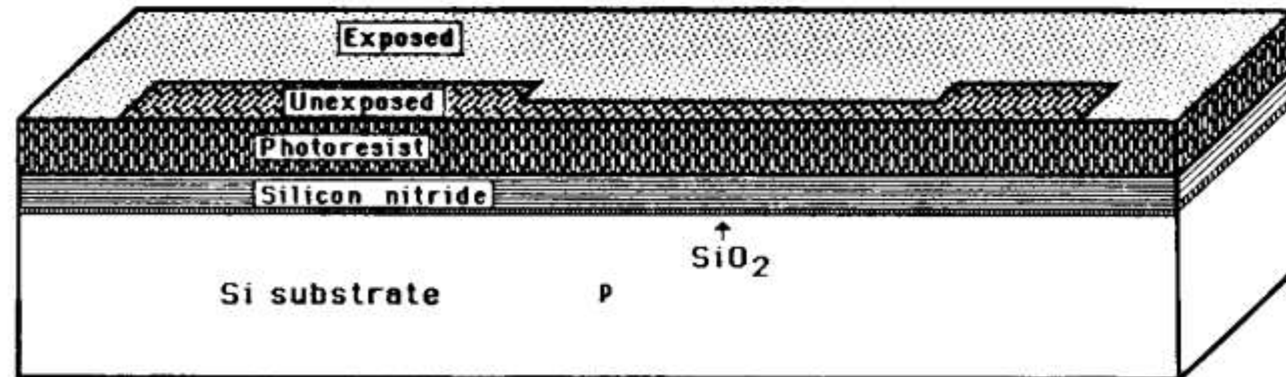


Padox

Nitride

Resist apply

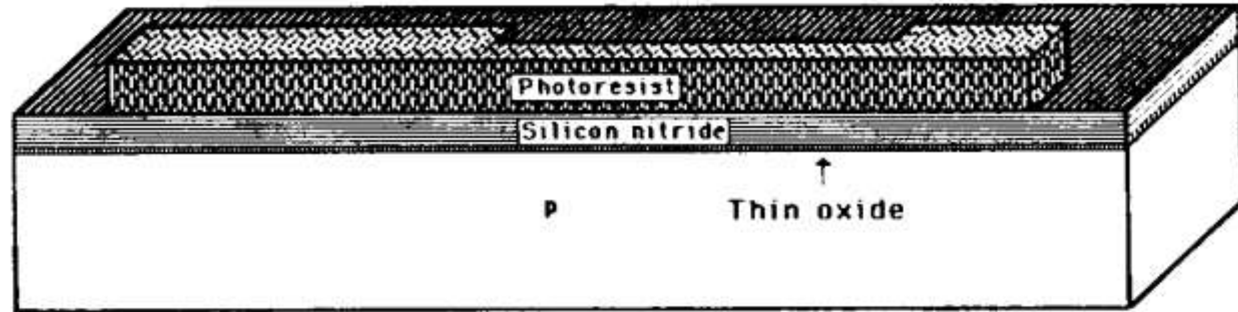
Expose



S.Wolf: Si Proc. VLSI ERA

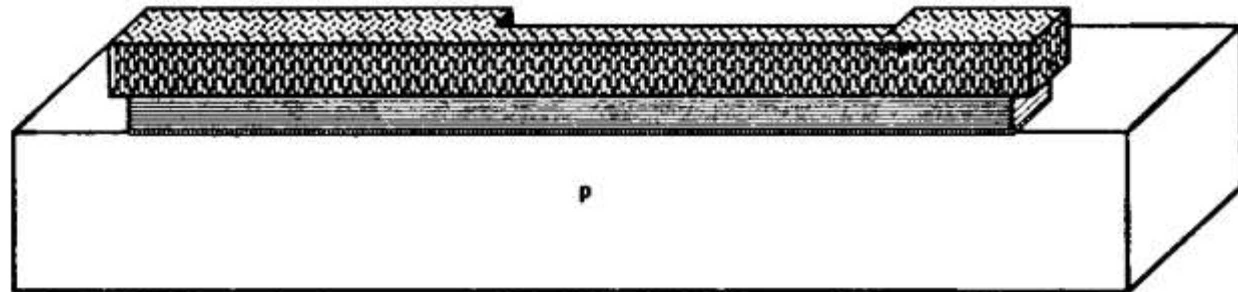
E/D N-MOS Prozess (2)

Develop

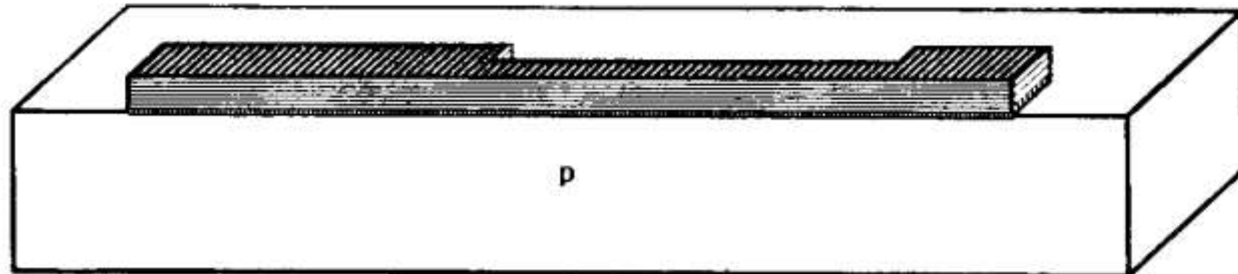


Nitride etch

Padox etch



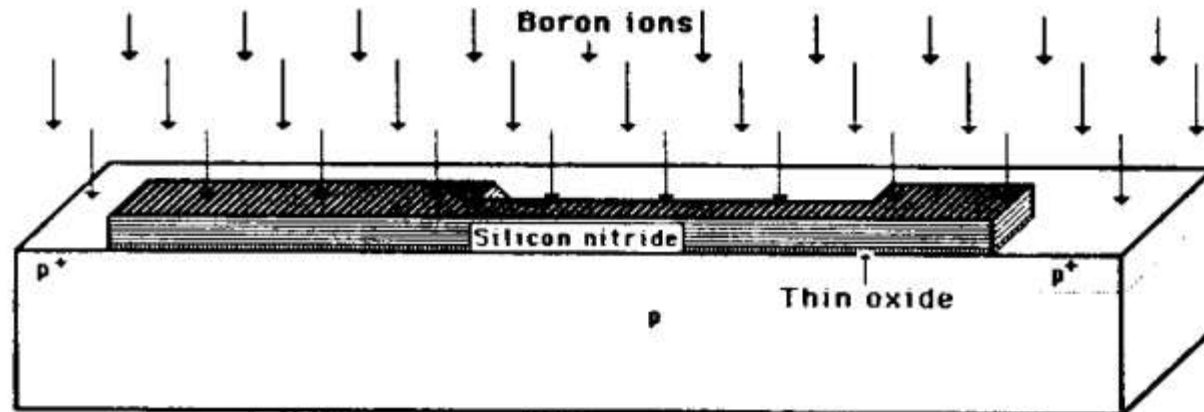
Resist strip



S.Wolf: Si Proc. VLSI ERA

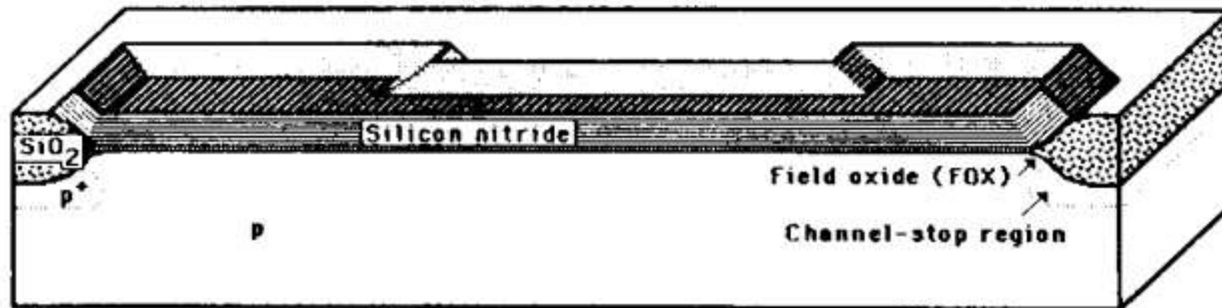
E/D N-MOS Prozess (3)

ChanStp Implant



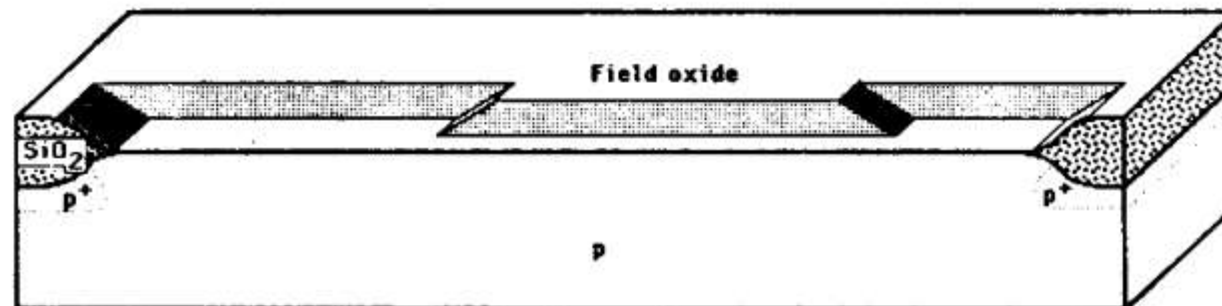
Local Oxidation

(Wet ox, Simultanously activation of ChanStp Impl.)



Etch Nitr/Padox (Kooi effect!)

Sequence:
Etch Nitr/Padox
Grow Sacrif. Ox.
Etch Sacrif. Ox



S.Wolf: Si Proc. VLSI ERA

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E/D N-MOS Prozess (4)

Mask2/Layout:

Def. Active Region for depletion Transistor

Res apply

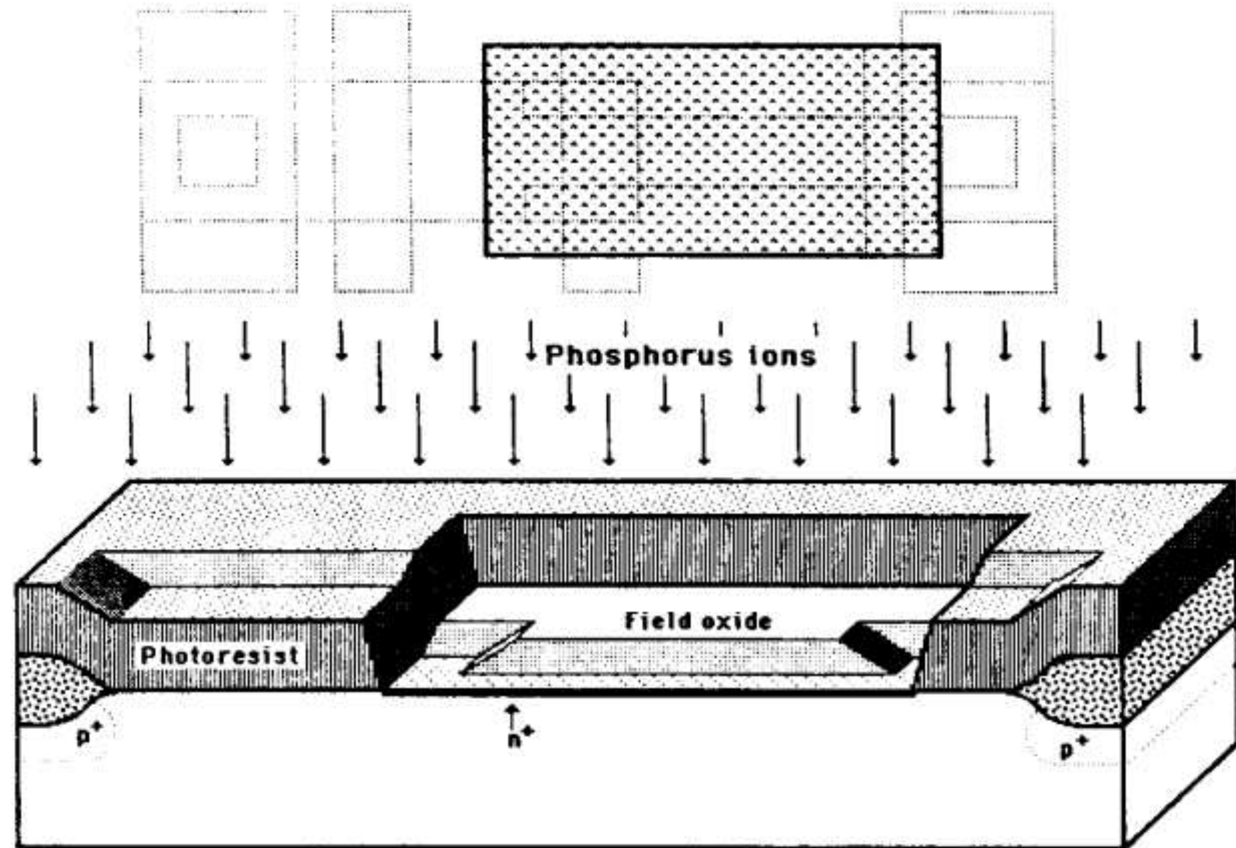
Expose

Develop

Implant

Strip

Gate Oxidation (Dry)



S.Wolf: Si Proc. VLSI ERA

E/D N-MOS Prozess (5)

Mask3/Layout:

Def. Burried contact

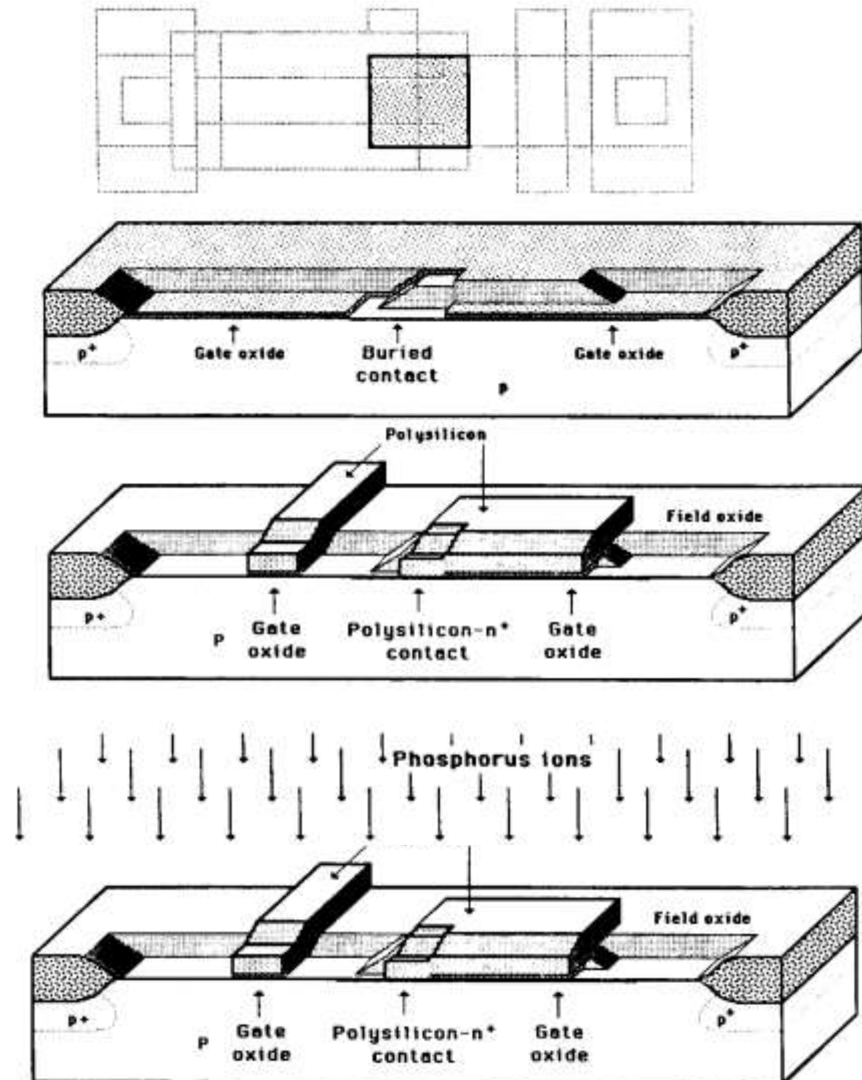
Poly-Si depo

Mask4: GateLine(s)

Poly etch

Gateox etch

S/D Implant



S.Wolf: Si Proc. VLSI ERA

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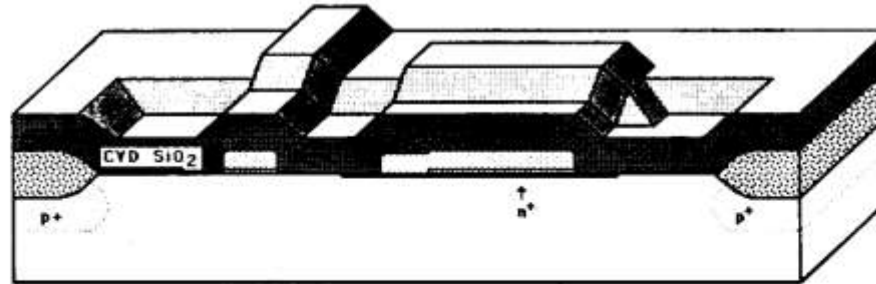
E/D N-MOS Prozess (6)

Depo of Insulation oxide (CVD Oxide)

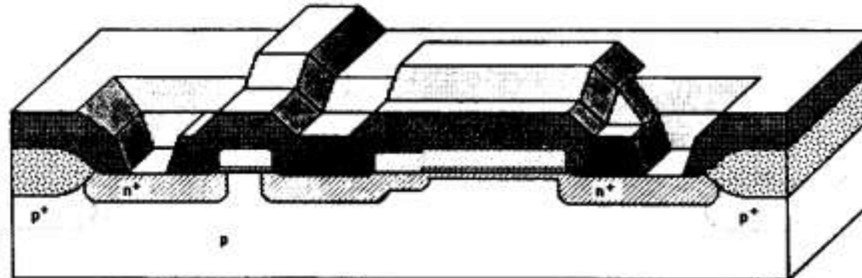


Ox - Reflow

Mask5: MetalContact

Contact etch

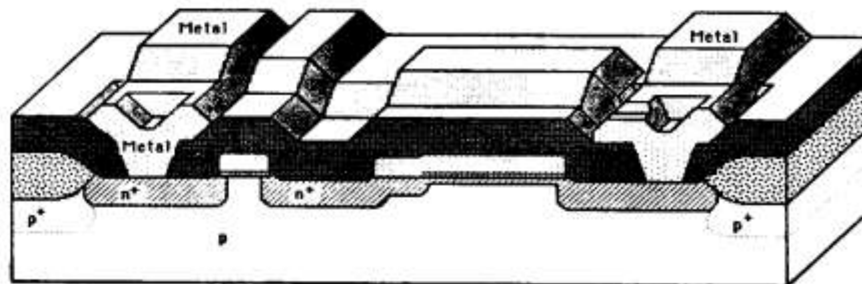
Reflow (Activation & diffusion of Implants)



Al Deposition

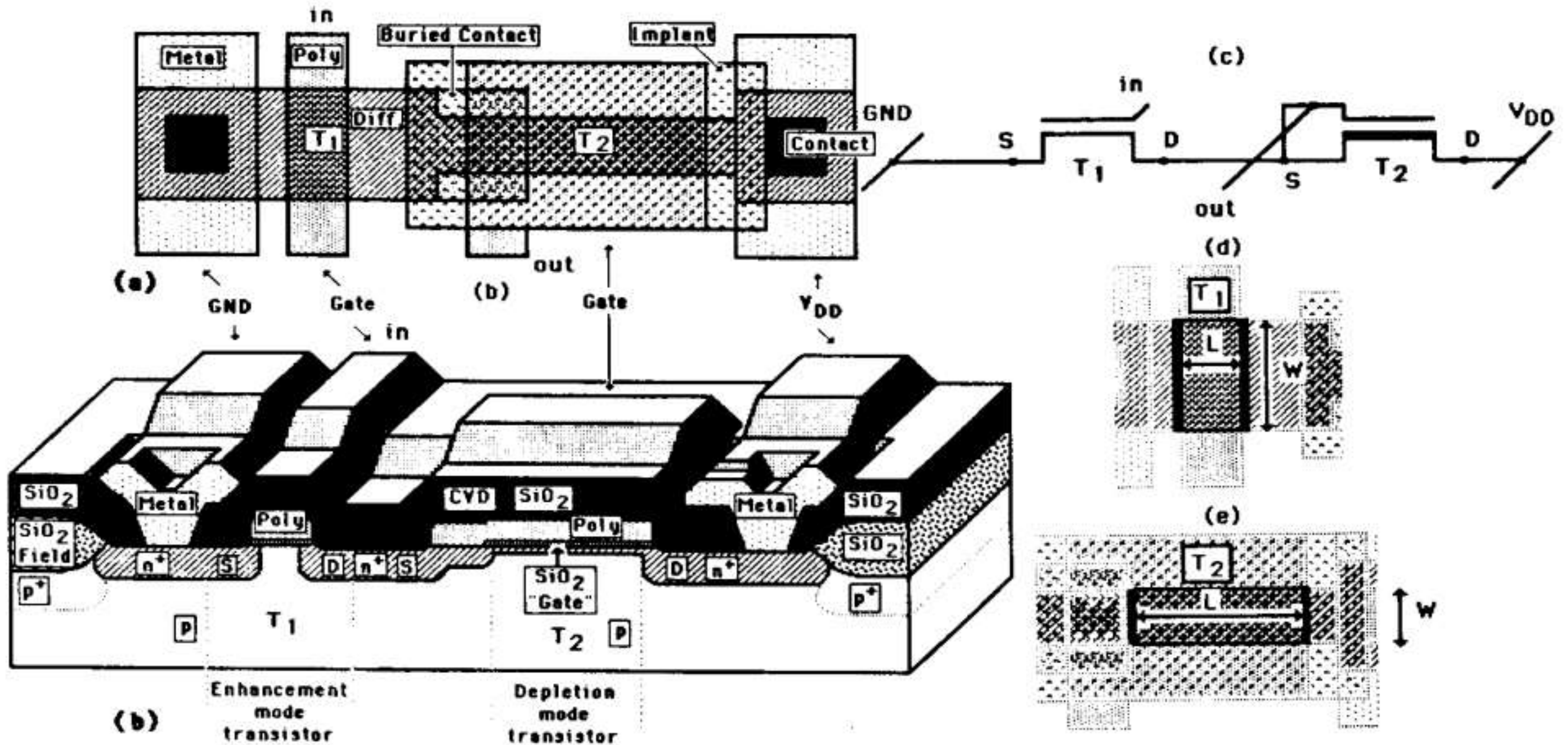
Mask6: Metal

Metal Etch



S.Wolf: Si Proc. VLSI ERA

E/D N-MOS Prozess (7)



S.Wolf: Si Proc. VLSI ERA

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TECHNISCHE UNIVERSITÄT DRESDEN

E/D N-MOS Prozess (7)

in
Metal
Poly
Buried Contact
Implant
Diff
T_1
T_2
Contact
GND
(a)
GND
Gate
(b)
out
Gate
V_{DD}
in

(c)
in
S
D
T_1
out
S
T_2
D
V_{DD}

SiO_2
Metal
Poly
CVD
SiO_2
Poly
Metal
SiO_2
SiO_2 Field
n^+
S
D
n^+
S
D
n^+
SiO_2
p^+
SiO_2 "Gate"
p^+
p
T_1
T_2
p
(b)
Enhancement mode transistor
Depletion mode transistor

(d)
T_1
L
W

(e)
T_2
L
W

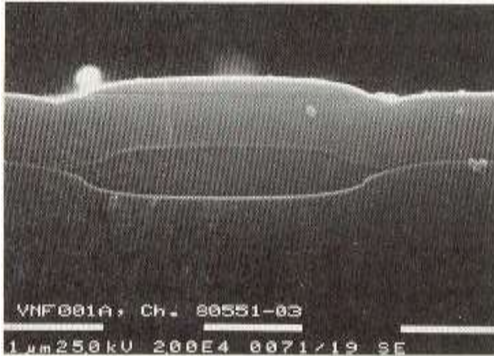
Continue

"SCT_SS20_10.03" 27:10

S.Wolf: Si Proc. VLSI ERA

3.2.2. LOCOS improvements

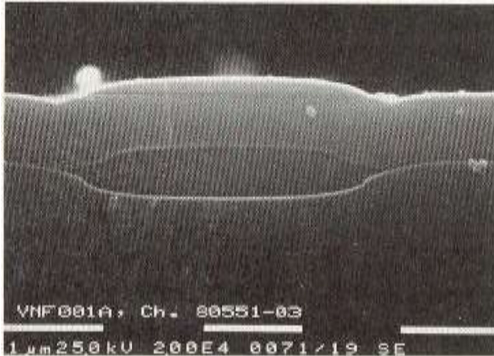
targeting DOF & scaling



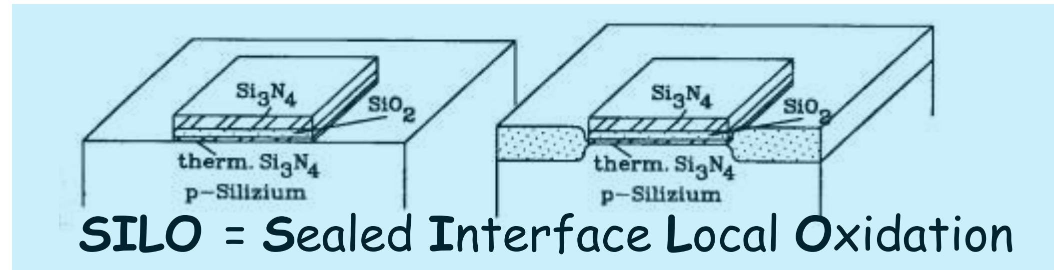
ROX = Recessed Oxide

3.2.2. LOCOS improvements

targeting DOF & scaling



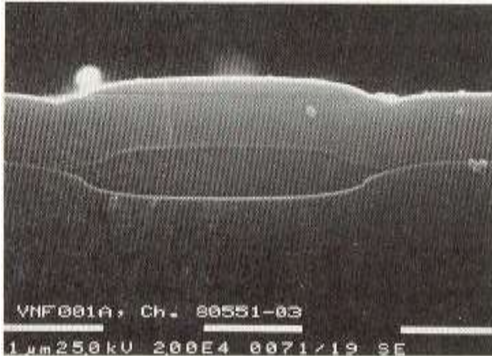
ROX = Recessed Oxide



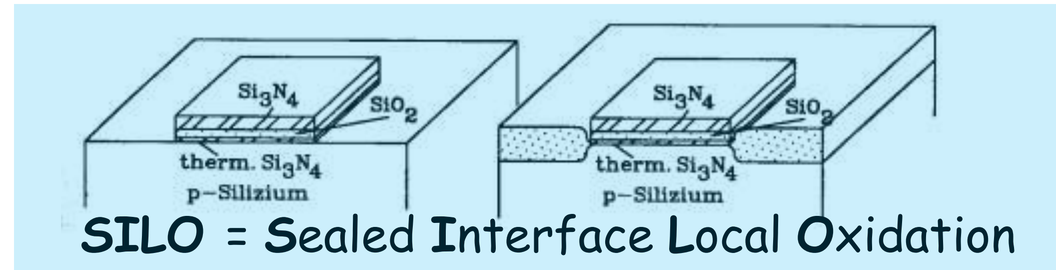
SILO = Sealed Interface Local Oxidation

3.2.2. LOCOS improvements

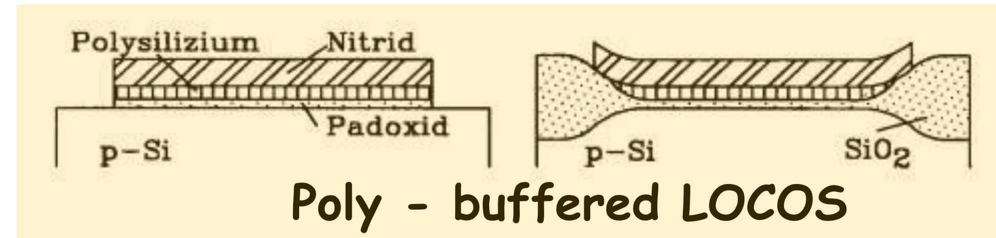
targeting DOF & scaling



ROX = Recessed Oxide



SILO = Sealed Interface Local Oxidation



Poly - buffered LOCOS

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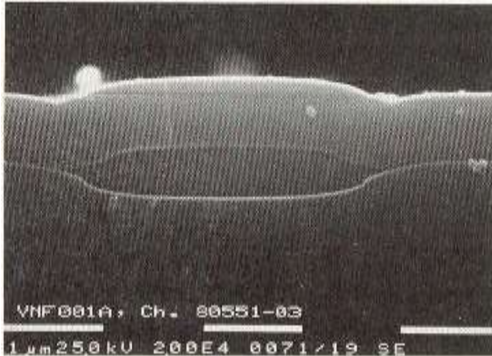
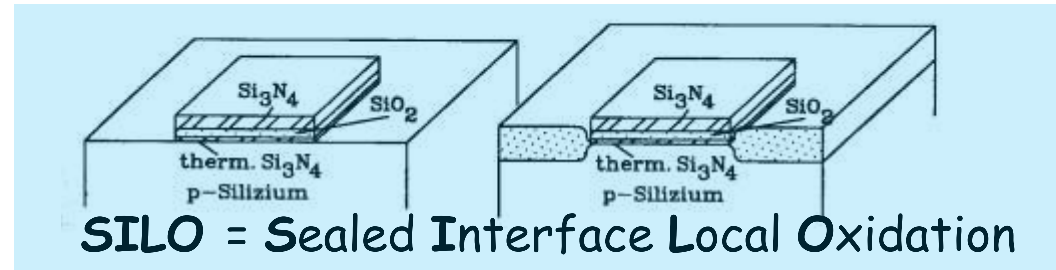
3.2.2. LOCOS improvements

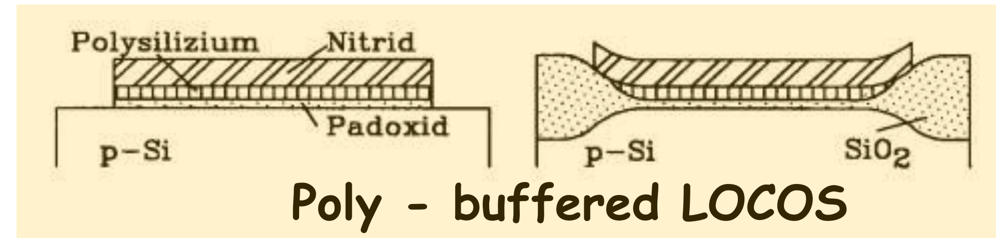
targeting DOF & scaling



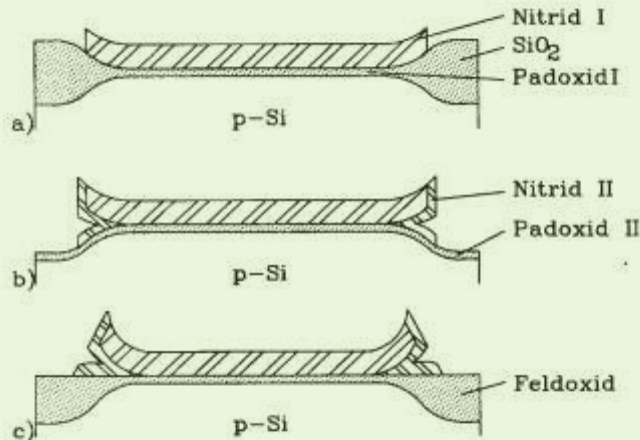
ROX = Recessed Oxide



SILO = Sealed Interface Local Oxidation



Poly - buffered LOCOS



SPOT = Super Planar Oxidation Techn.

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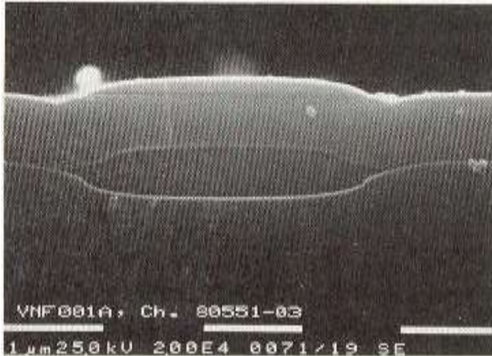
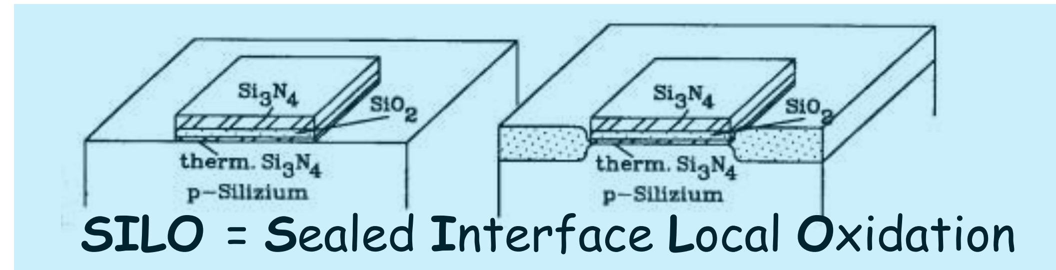
3.2.2. LOCOS improvements

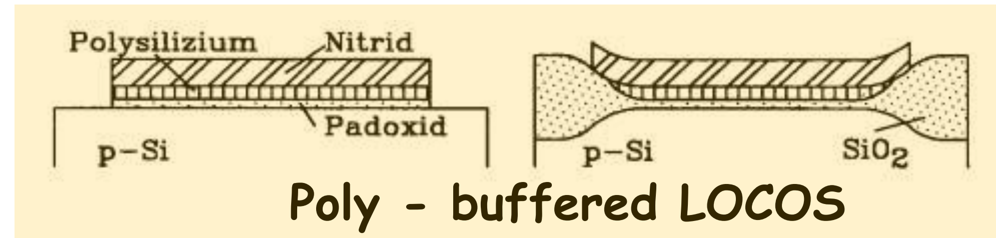
targeting DOF & scaling



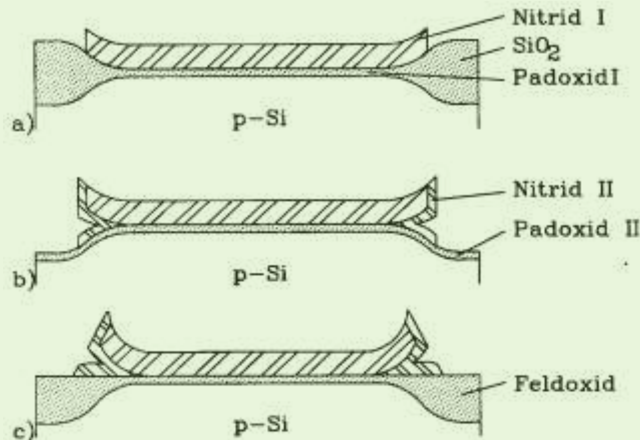
ROX = Recessed Oxide



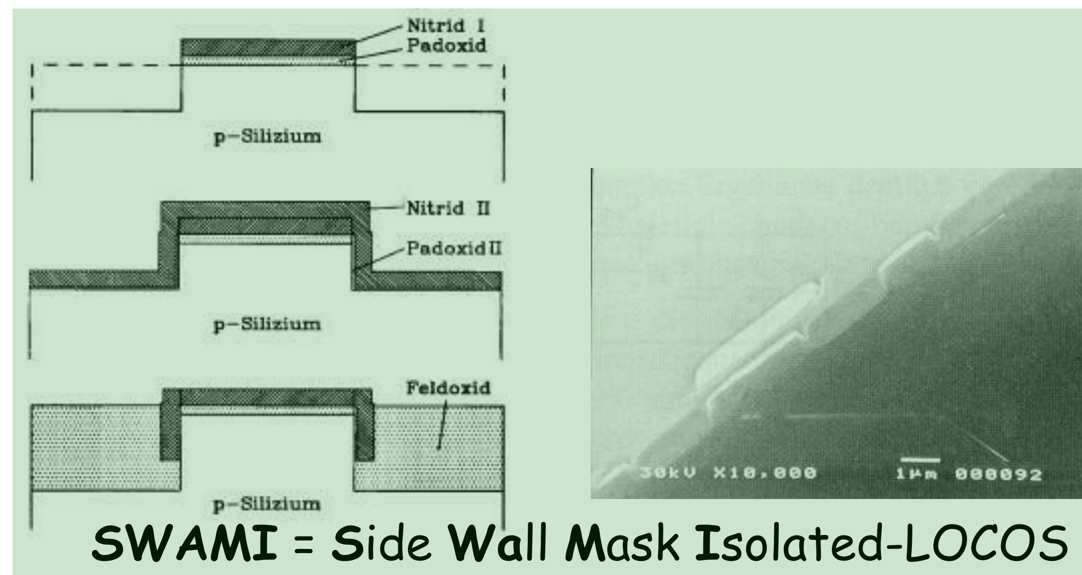
SILO = Sealed Interface Local Oxidation



Poly - buffered LOCOS



SPOT = Super Planar Oxidation Techn.



SWAMI = Side Wall Mask Isolated-LOCOS

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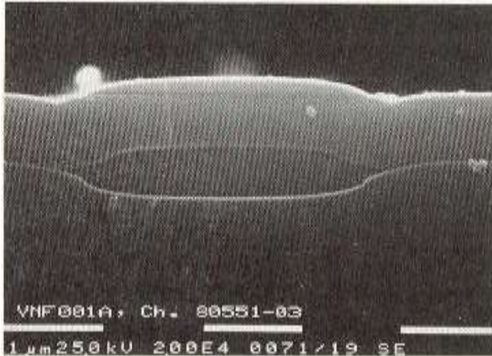
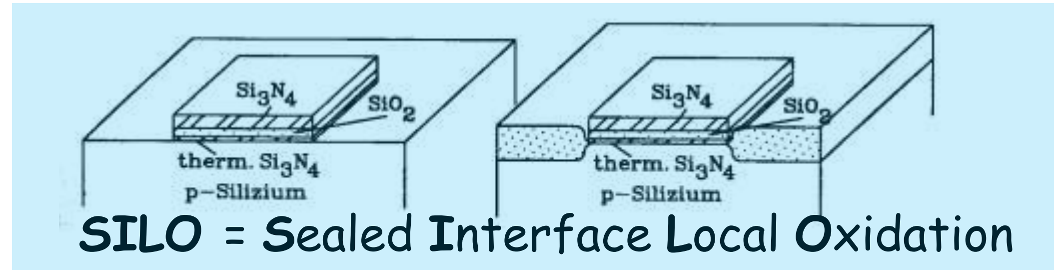
3.2.2. LOCOS improvements

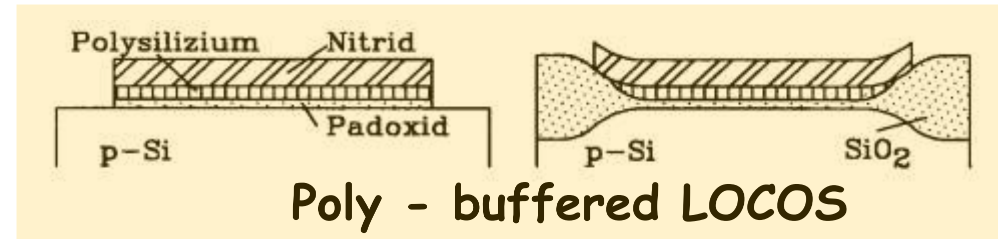
targeting DOF & scaling



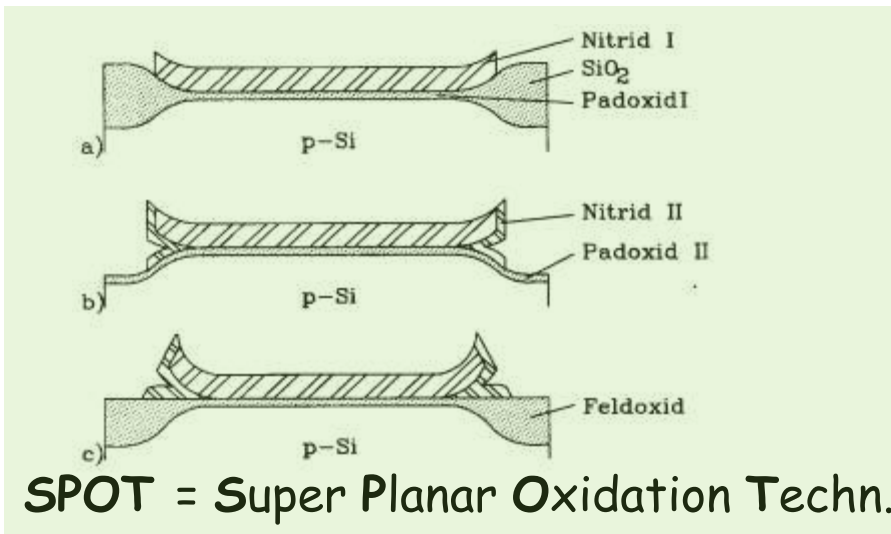
ROX = Recessed Oxide



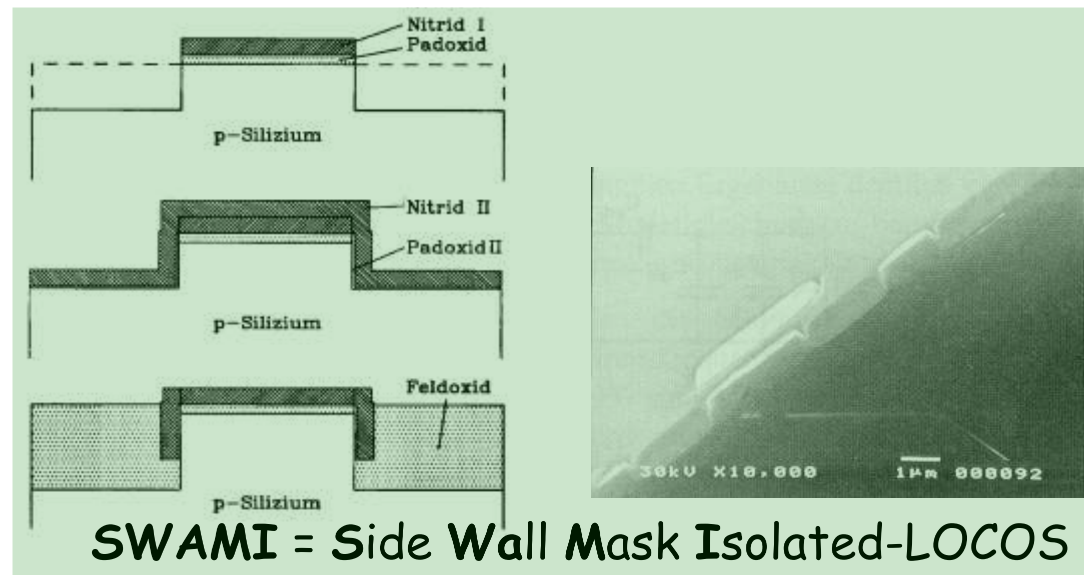
SILO = Sealed Interface Local Oxidation

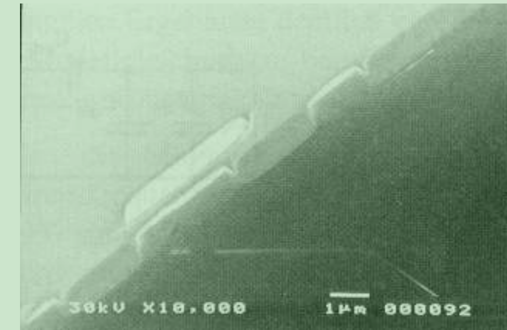


Poly - buffered LOCOS



SPOT = Super Planar Oxidation Techn.





SWAMI = Side Wall Mask Isolated-LOCOS

Ultimate concept: STI !

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3.2.3. Shallow Trench Isolation (STI)

- ☹ LOCOS creates significant topography
- ☹ LOCOS requires much floor space

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{Si} e N_A \left(2\Phi_F + V_{SB}\right)} + 2\Phi_F - \frac{Q_{eff}}{C_{ox}} + \frac{\Delta W_F}{e}$$

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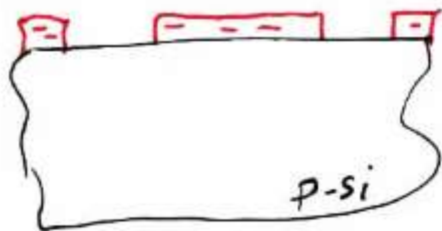

Def. Hard mask

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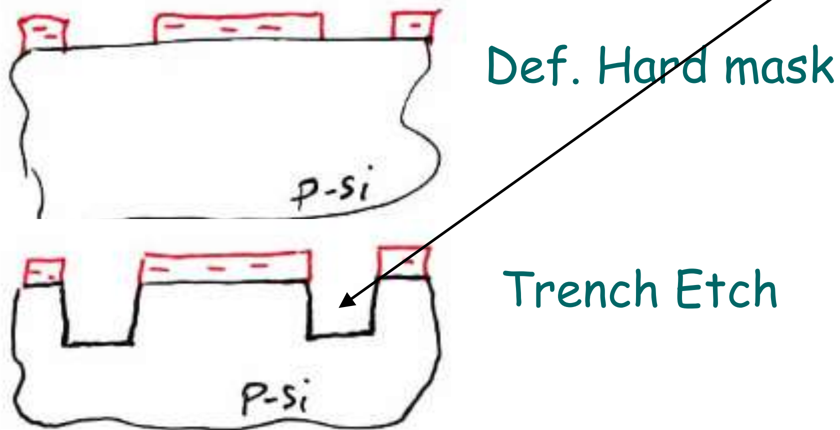

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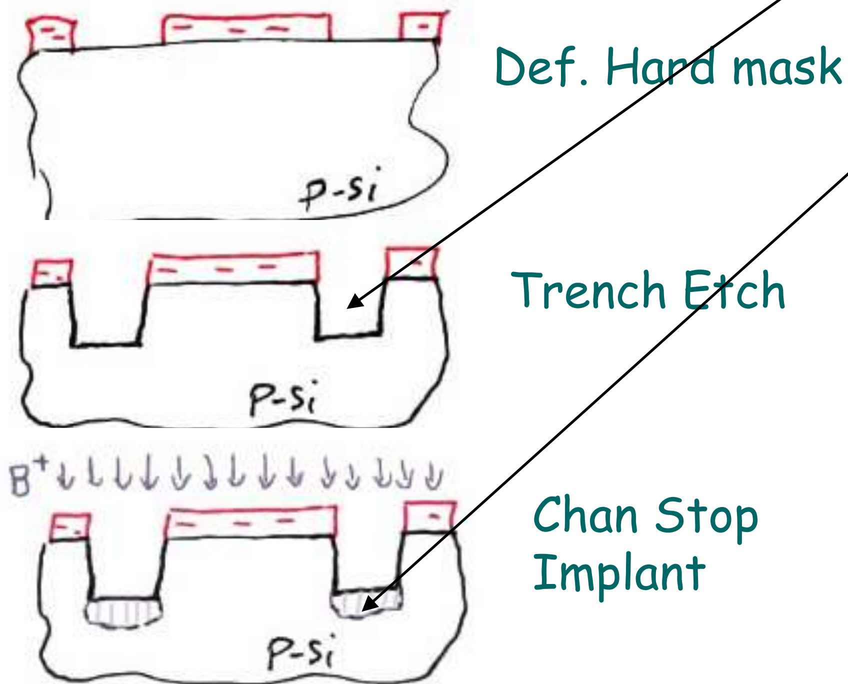

Def. Hard mask

Trench Etch

Chan Stop Implant

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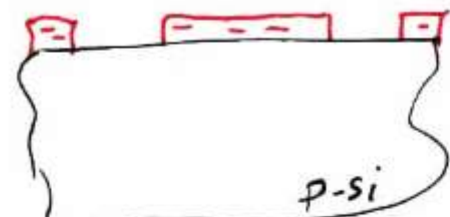

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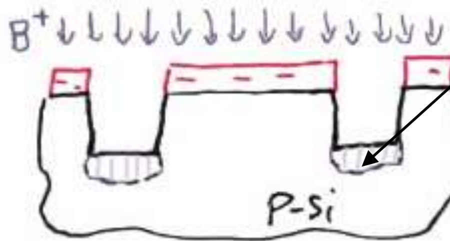
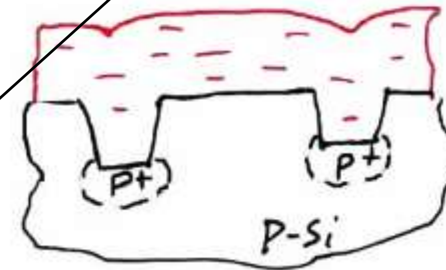
Trench Etch



Chan Stop Implant



CVD-SiO_2

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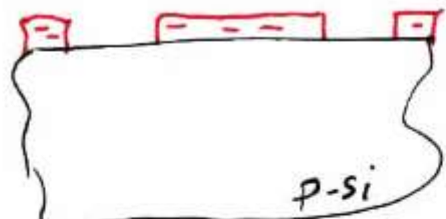
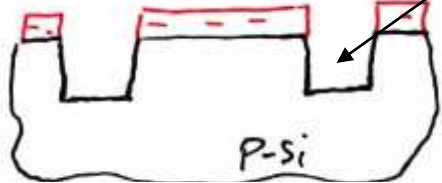
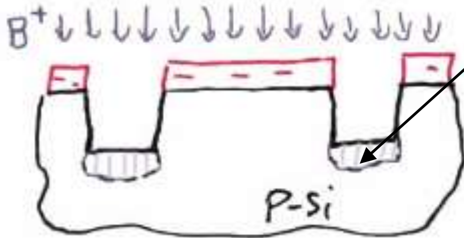


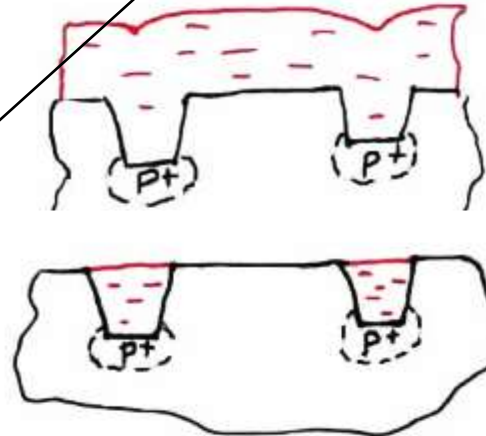
Def. Hard mask



Trench Etch



Chan Stop Implant



CVD-SiO_2

Etch back or CMP

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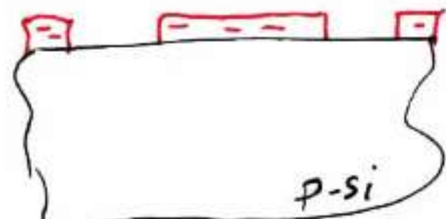
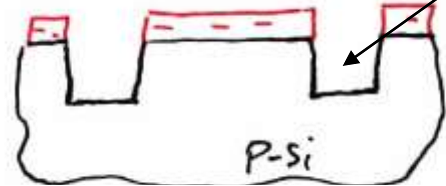
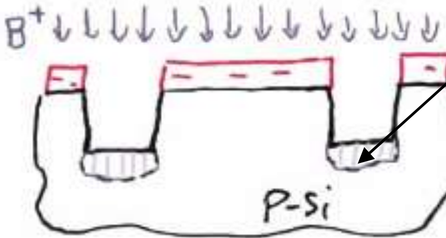


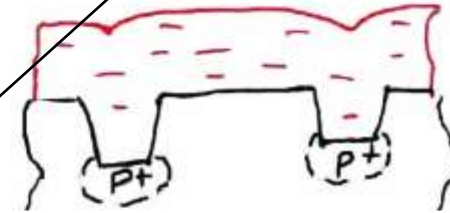
Def. Hard mask



Trench Etch

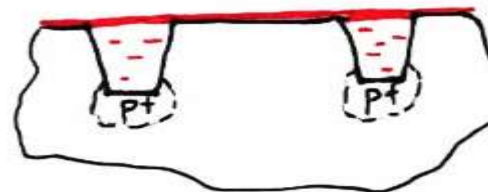


Chan Stop Implant



CVD-SiO_2

Etch back or CMP



Gate ox

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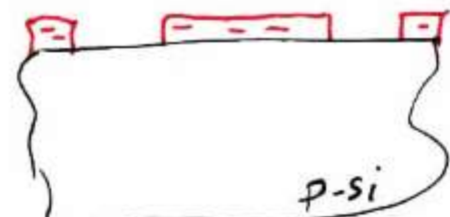
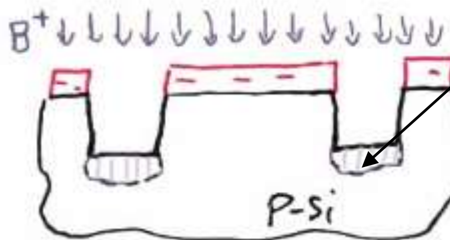
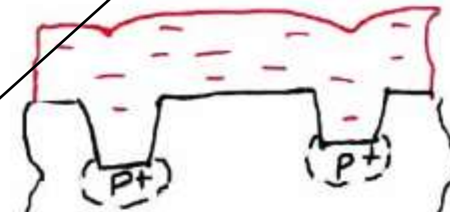


Def. Hard mask

Trench Etch

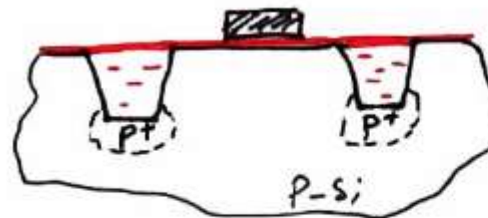


Chan Stop Implant



CVD-SiO_2

Etch back or CMP



Gate ox
Def. Gate

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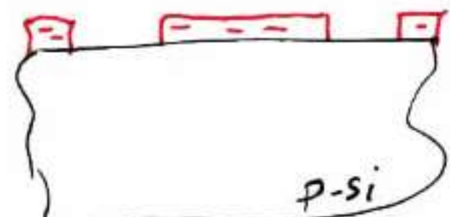
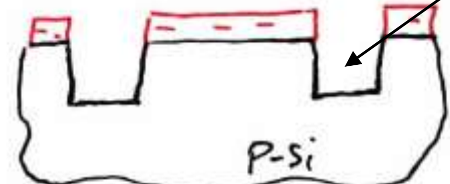
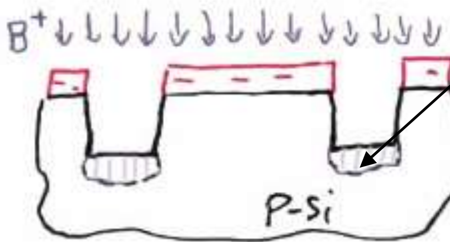


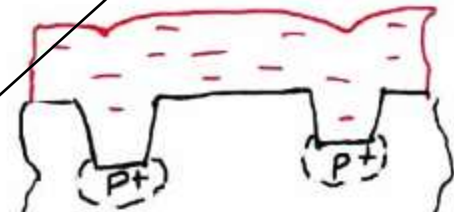
Def. Hard mask



Trench Etch

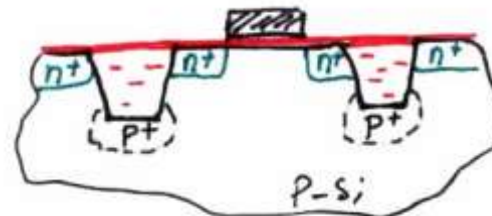


Chan Stop Implant



CVD-SiO_2

Etch back or CMP



Gate ox
Def. Gate
S/D Implant

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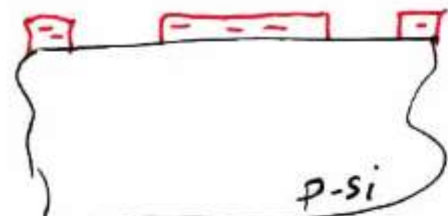
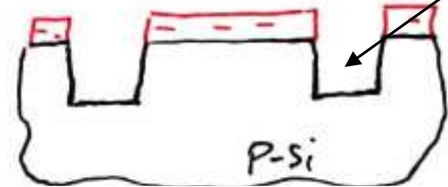
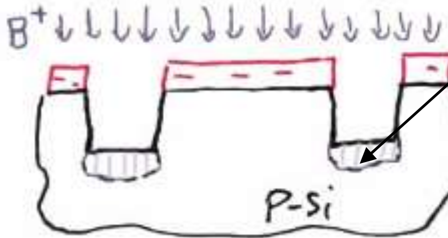


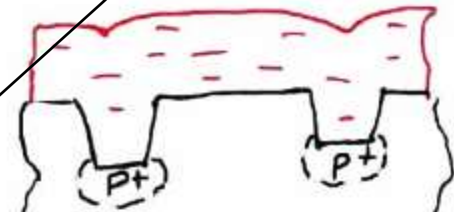
Def. Hard mask



Trench Etch

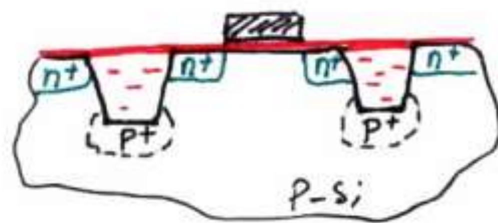


Chan Stop Implant
(can be skipped if trench is deep enough!)



CVD-SiO_2

Etch back or CMP



Gate ox
Def. Gate
S/D Implant

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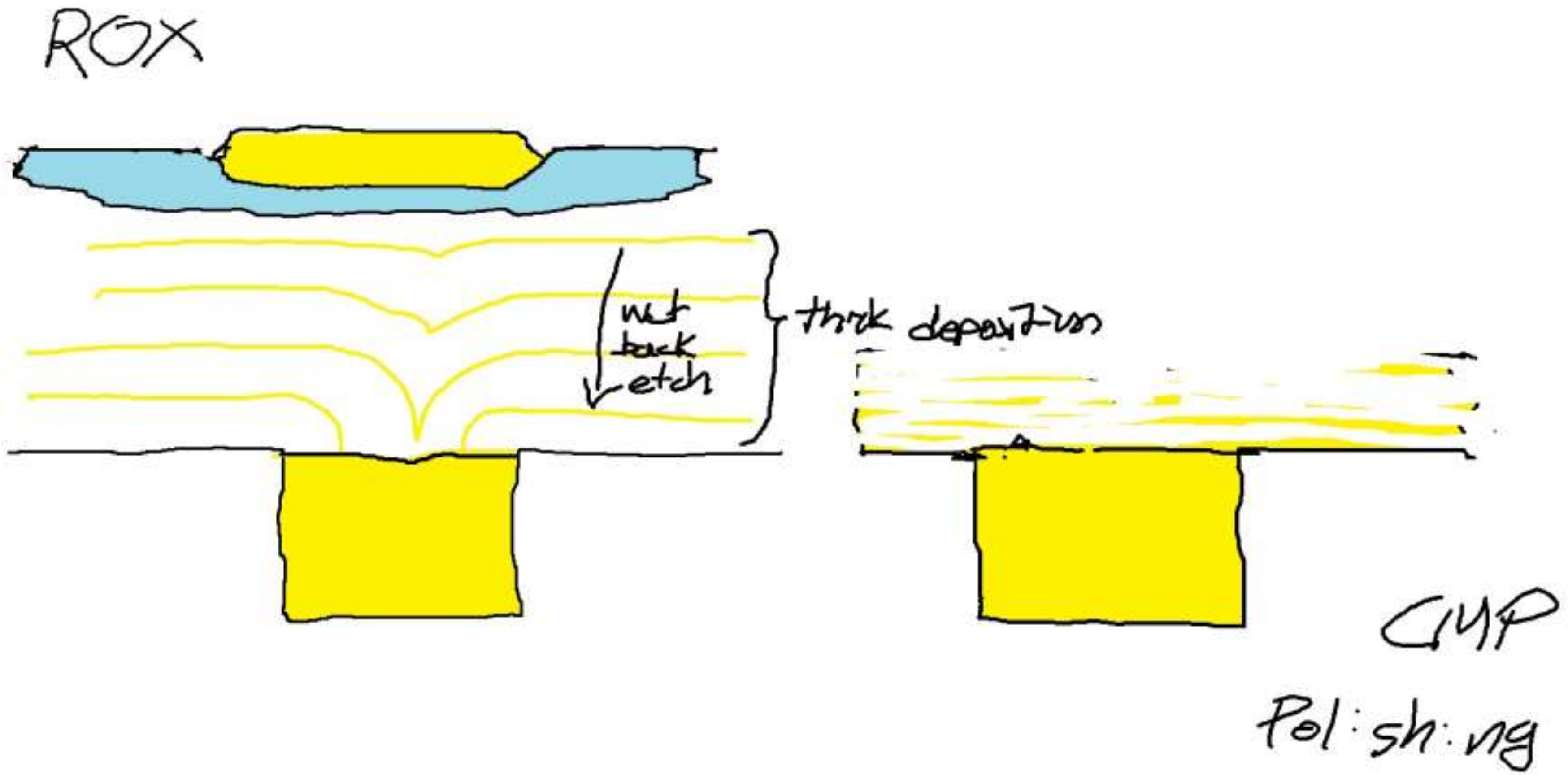
ROX
wet
back
etch
thick deposition
CMP
Polishing

»Wissen schafft Brücken.«