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select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

# Lecture SCT2 – Process Integration

## 11. Web-based virtual Lecture: July 01 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here

"SCT_SS21_11.1" 39:50

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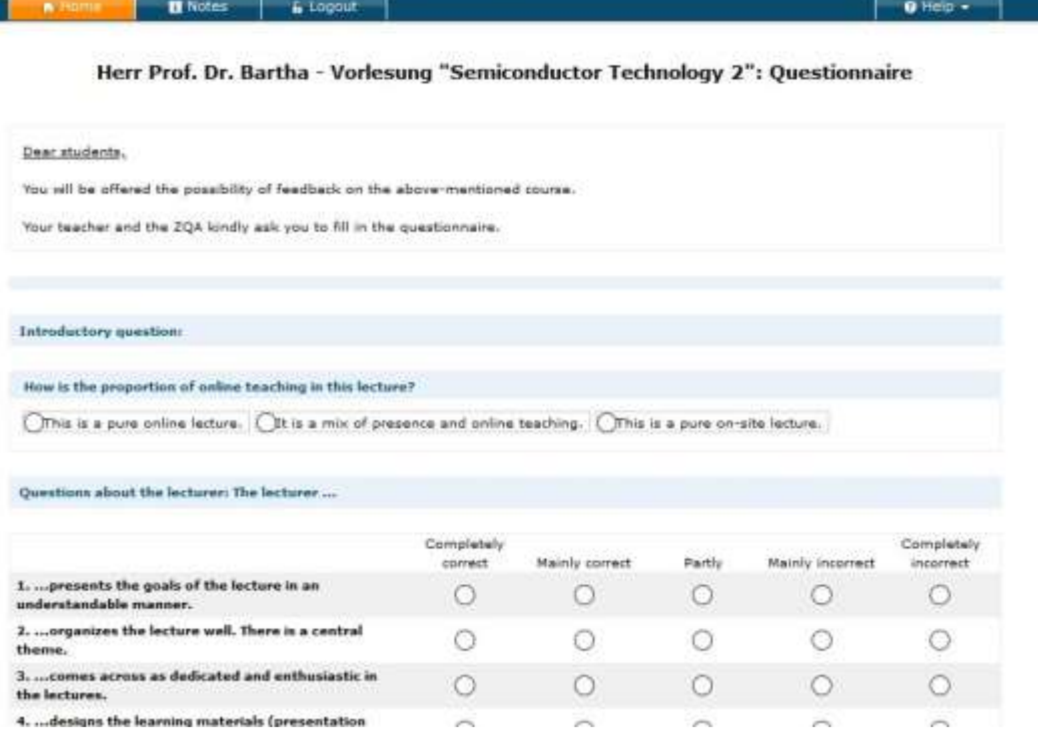


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# Written exam

**Faculty of Electrical and Computer Engineering**

21.06.2021

Examination office

**Exams Summer Semester 2021**

**Master´s Program Nanoelectronic Systems**

**examination period from 26.07.-21.08.2021**

Preliminary plan.
Changes are possible

| examination subject (Module name) | Module | duration and kind | professor | date/time |
|---|---|---|---|---|
| **Compulsory Modules** | | | | |
| Lab sessions<br>M1200-50040<br>Semicond. Techn. Lab | NES-11 06 01 | protocol 2 | Bartha | on appointment |
| Semiconductor Technology<br>M1212-50080 | NES-12 12 02 | **oral exam** of 30 min or written exam of 120 min (>20 students) | Prof. Bartha (Dr. Wenzel) | 07.10. |
| Radio Frequency Integrated Circuits<br>M1208-1I100 | NES-12 08 02 | written exam of 120 min | Prof. Ellinger (Dr. Schumann) | 27.07. |
| Hardware/Software Codesign<br>M1210-50030 | NES-12 10 03 | oral exam of 20 min or **written exam of 120 min** (> 16 students) | Prof. Fettweis (Dr. Matus) | 12.08. |
| **Optional Modules** | | | | |

https://tu-dresden.de/ing/elektrotechnik/ressourcen/dateien/studium/pruefungen/pruefungsplaene/pruefungsplaene-sose2021/2nes.pdf?lang=de

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# Outline

**SC-Basics**

Review:
- SCT Basics
- MOS Capacitor
- MOS-Cap-CV
- MOS-FET (N-FET enh.)
- Al-Gate FET
- SRAM product (E/E)
- $V_T$ adjust => Depl.
- E/D Logic
- Si Gate Process
- LOCOS => STI

Today: Further self aligned


0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1. MOS Structure, MOS Capacitor
    2. Structure of a MOSFET
    3. I/V behavior
2. Circuits in Metal-Gate FET Technology
    1. Process sequence of N-MOSFET in Metal Gate
    2. From inverter to memory cell
    3. SRAM in NMOS Metal Gate
    4. The threshold voltage of the MOSFET
        1. Parasitic FET
        2. Enhancement/Depletion Transistor
        3. N-MOS Logic by E/D Transitors
        4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1. Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1. Example: Process flow of E/D SiGate LOCOS Inverter
        2. LOCOS Variation
        3. Shallow Trench Isolation
    3. Lightly doped drain
    4. SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4. Transition to CMOS Technology
    1. MOS Transistor Types
    2. CMOS Inverter
        1. Consideration NMOS E/D Inverter
        2. Comparison CMOS Inverter
    3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1. Scaling
        1. Challenges
        2. Material Equivalent Scaling
        3. Further Concepts


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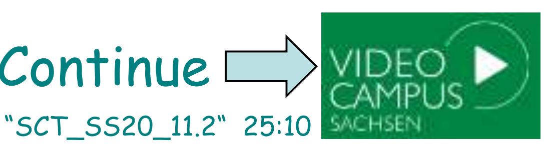

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http://www.computerhistory.org/siliconengine/timeline/

# Blackboard: Evolution of fieldox

DOF
Gateox
Poly-Si
Fieldox
n+
← L →
p-Si
Fieldoxide

Poly-Si Gate Process

Poly Gate
DOF
LOCOS
n+
← L →
P-Si
LOCOS
channel stopper

DOF
STI
L

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# 3.3 Lightly Doped Drain LDD

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# Where do we find the highest fieldstrength? ( E=-dΦ/dx )

Φ

BULK

SOURCE

DRAIN

Vg (V)

Vfb 1 2 3 4 5

Vds=4.9 V

3D (reset)

Azimuth=15 deg.

Elevation=13 deg.

2D

x - y diagram

E - y (lateral)

E - x (vertical)

DEMO ROTATIONS

3D->x-y

3D->E-y (lateral)

3D->E-x (vertical)

CLOSE

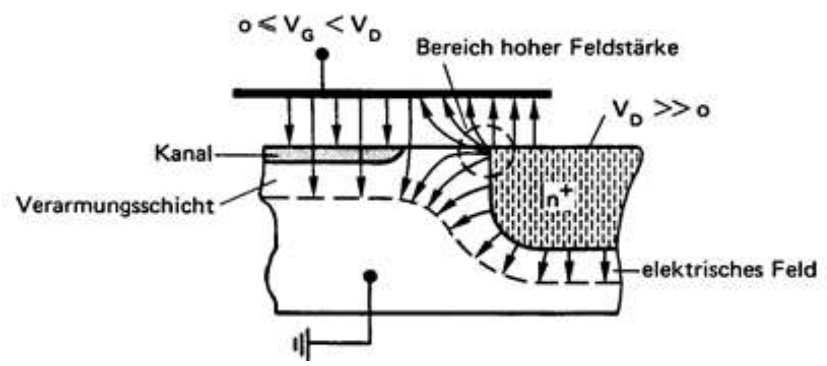
DRAIN CURRENT (mA)

DRAIN VOLTAGE (V)

GATE VOLTAGE (V)

# Double Diffused Drain, DDD and Lightly Doped Drain, LDD

## High electric field strength at the channel/drain edge!

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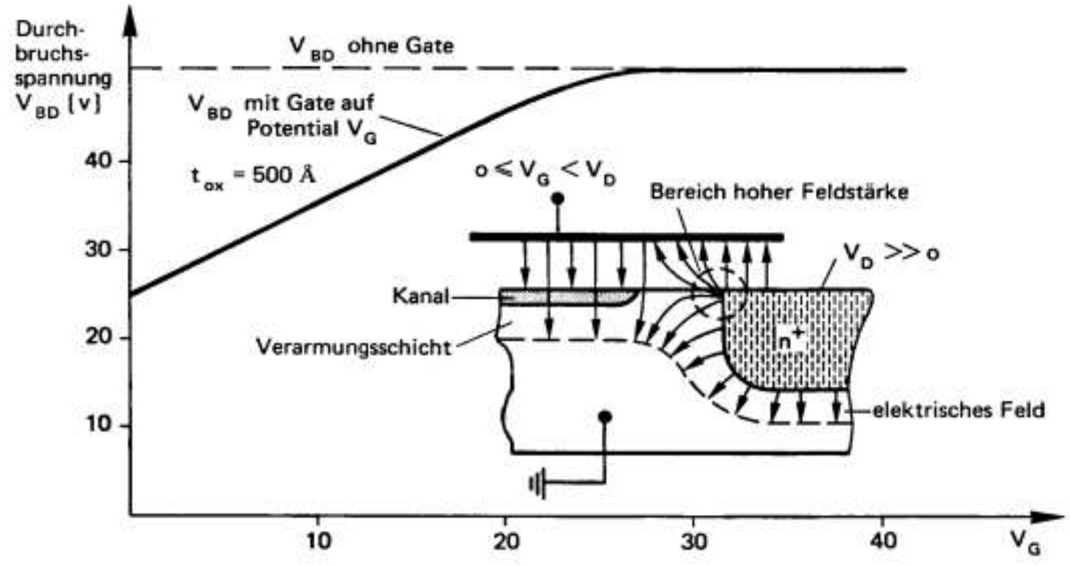
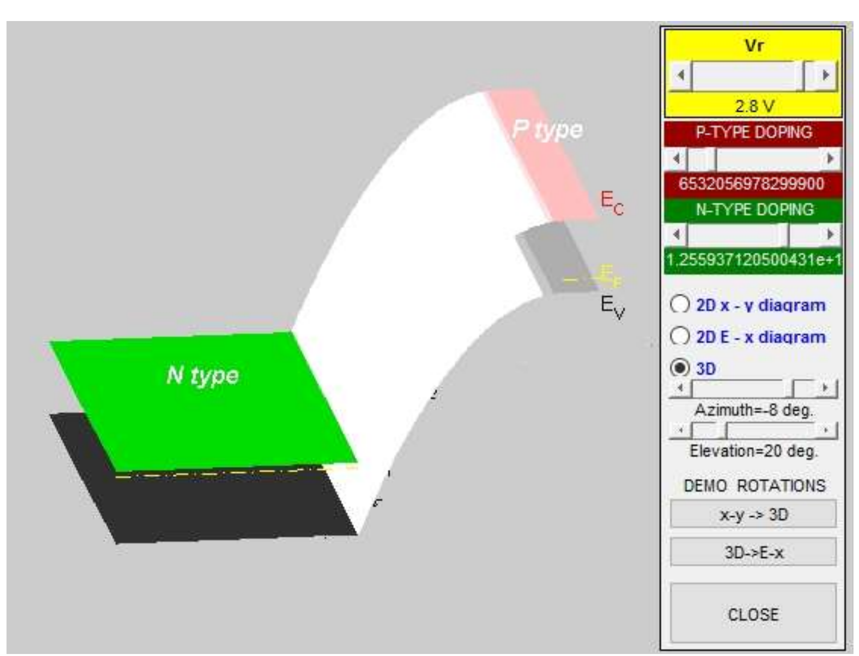
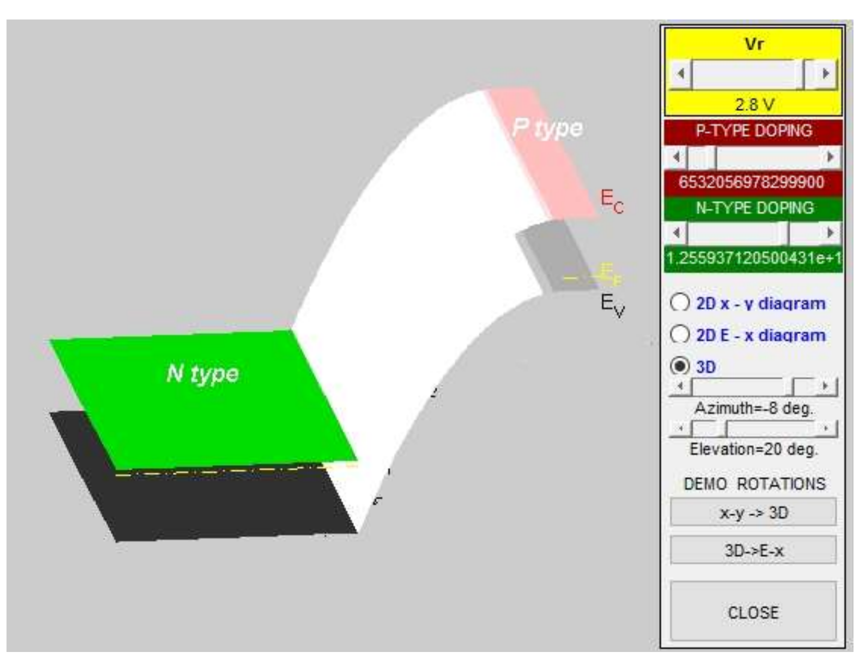


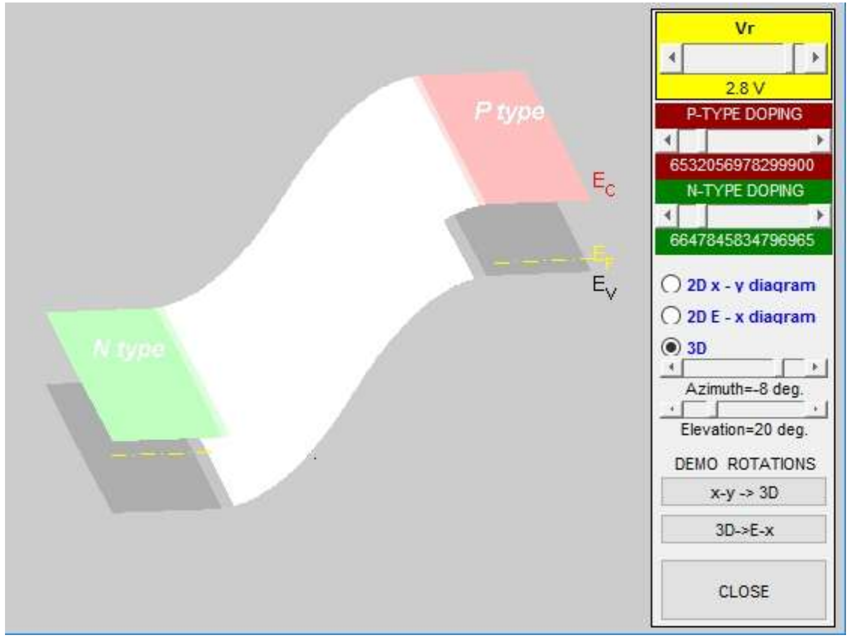

Abb. 36 Einfluss eines Gates über einem pn-Übergang auf die Durchbruchsspannung $V_{BD}$



P type
N type
$E_C$
$E_F$
$E_V$
Vr
2.8 V
P-TYPE DOPING
6532056978299900
N-TYPE DOPING
1.255937120500431e+1
2D x - y diagram
2D E - x diagram
3D
Azimuth=-8 deg.
Elevation=20 deg.
DEMO ROTATIONS
x-y -> 3D
3D->E-x
CLOSE

# Relaxation of the field strength by lowering n-doping



# Relaxation of the field strength by lowering n-doping

Compare the edge in Φ(x) for strong and lightly doped n at the junction

# High electric field strength at the channel/drain edge!

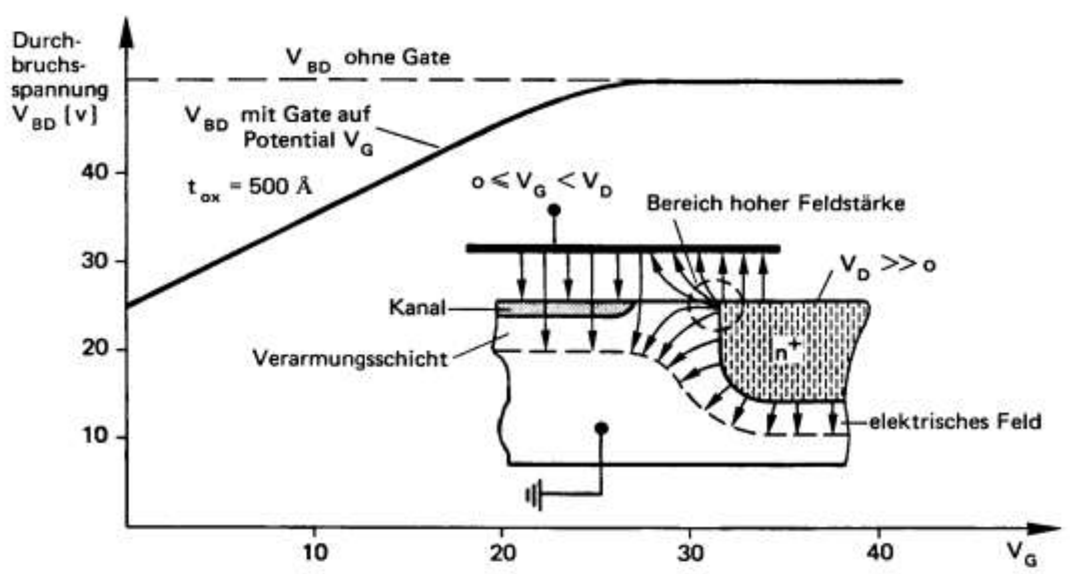



Abb. 36 Einfluss eines Gates über einem pn-Übergang auf die Durchbruchsspannung $V_{BD}$

# Double Diffused Drain, DDD and Lightly Doped Drain, LDD

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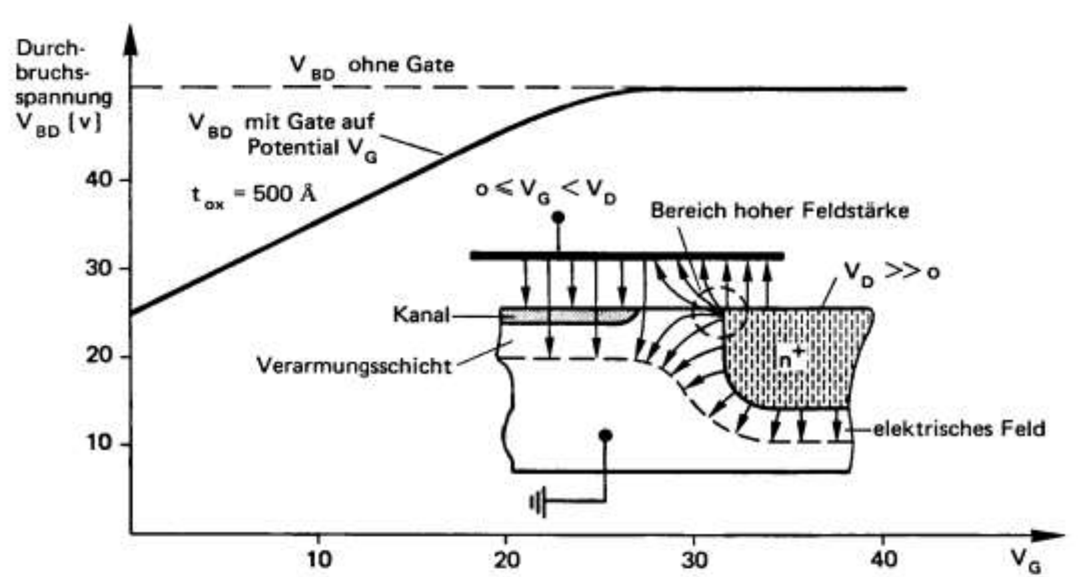
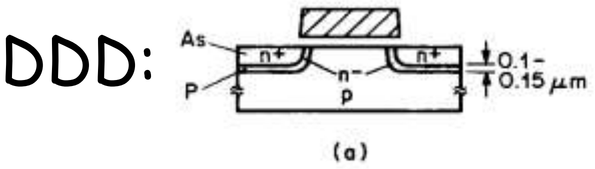
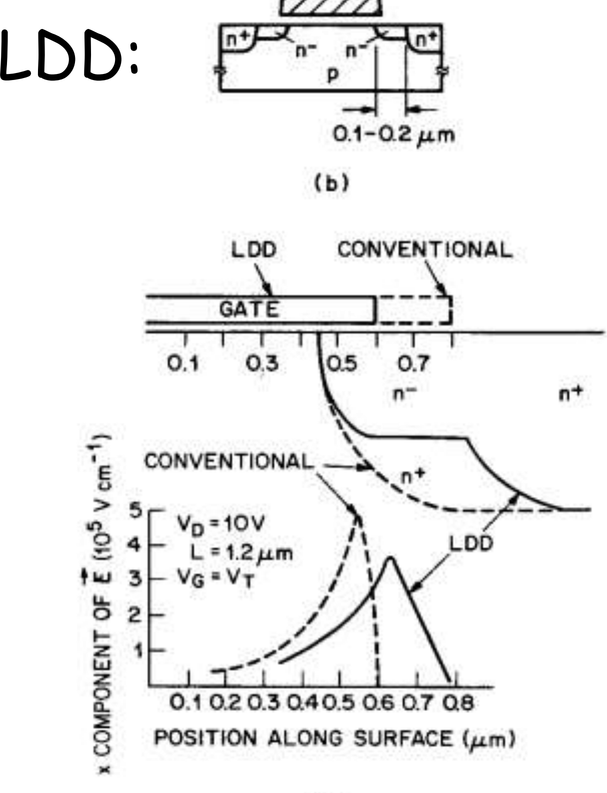



Abb. 36 Einfluss eines Gates über einem pn-Übergang auf die Durchbruchsspannung $V_{BD}$

DDD:




LDD:

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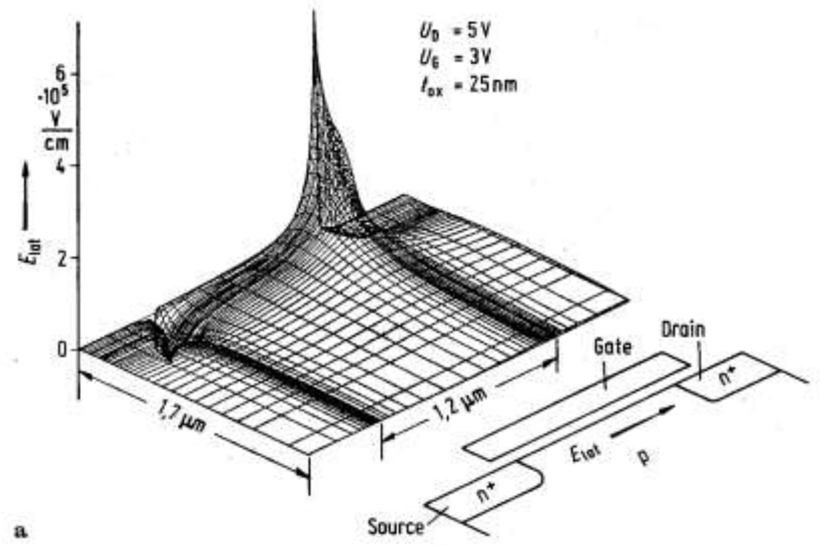
# Lightly Doped Drain, LDD



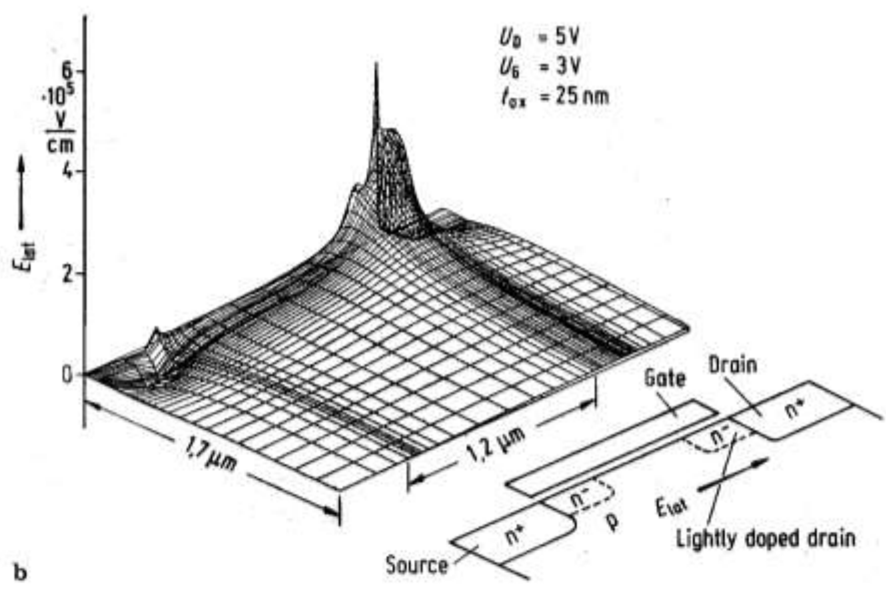




**Abb. 8.1.4.** Verteilung des elektrischen Feldes im MOS-Transistor (Simulation mit MINI-MOS [8.6]) **a** für einen N-Kanal-Transistor mit 1,2 µm-Kanallänge; **b** für die gleiche Transistorstruktur, jedoch mit LDD (*L*ightly *D*oped *D*rain) [8.7]

# Lightly Doped Drain LDD

The junction at the Drain side creates a peak in the electric field strength, creating "hot electrons", which may gain enough energy to penetrate into the gate oxide and degrade the device. A smooth junction relaxes this effect.

# Lightly Doped Drain LDD

To create this smooth junction (LDD) with the required accuracy, no photo alignment is necessary. It is done in a self aligned way utilizing the anisotropic behavior of reactive ion etching.

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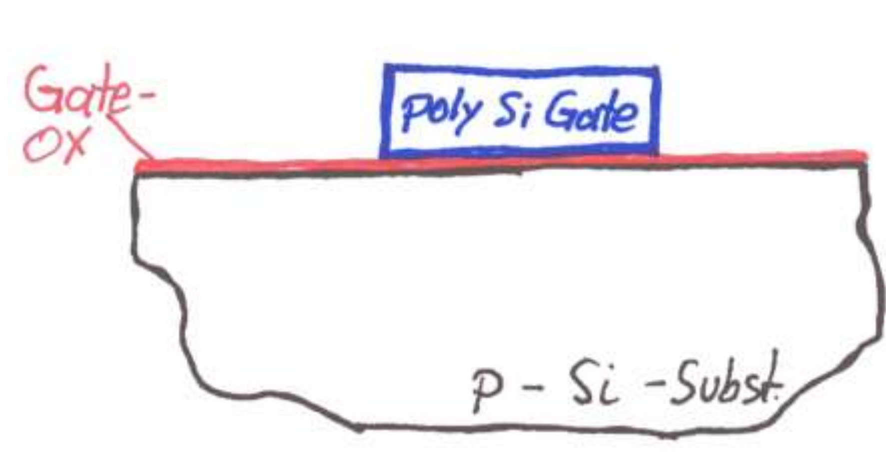


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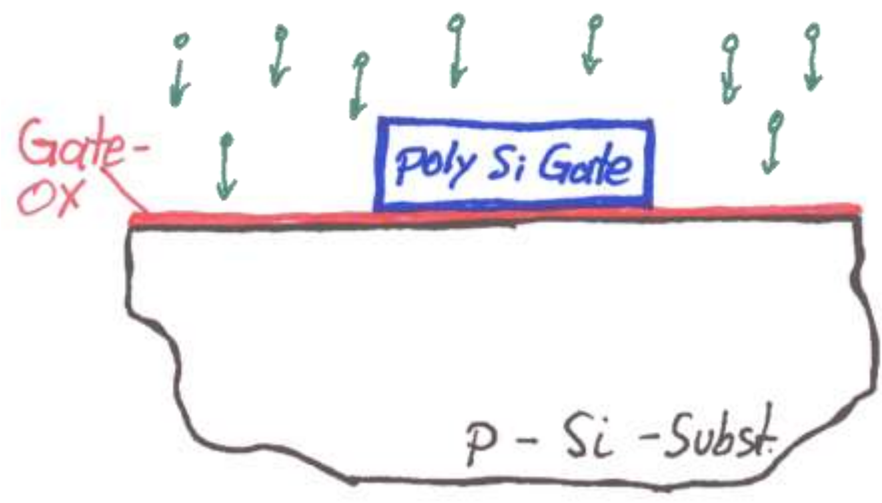


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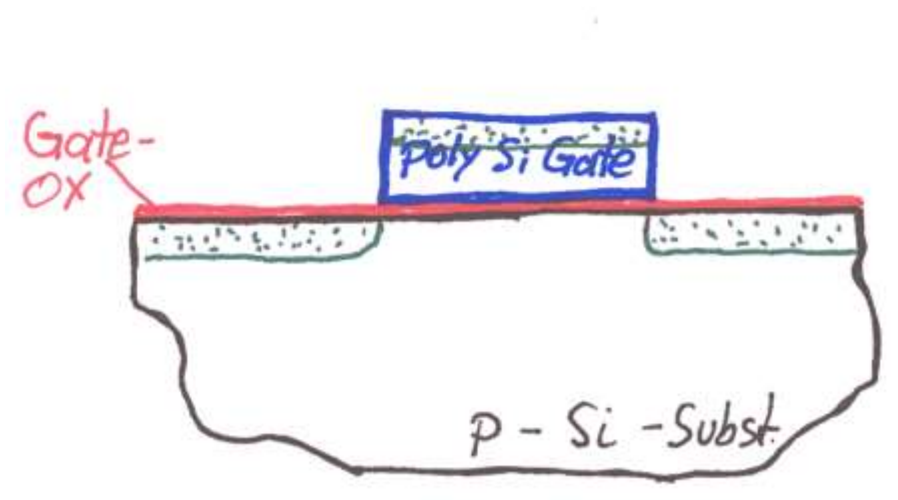


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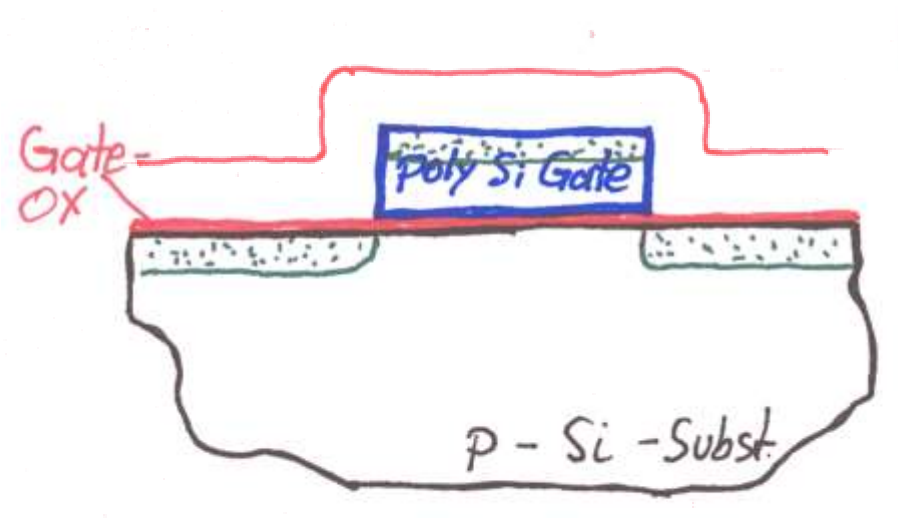

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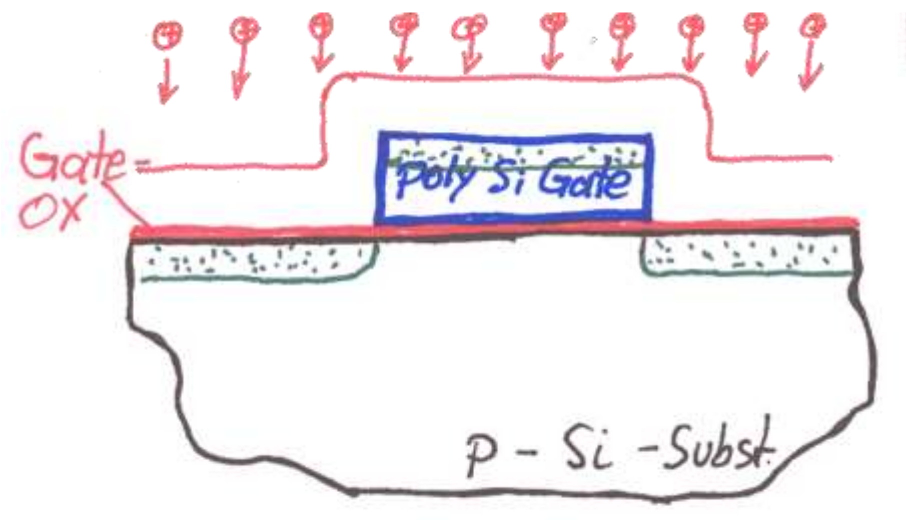


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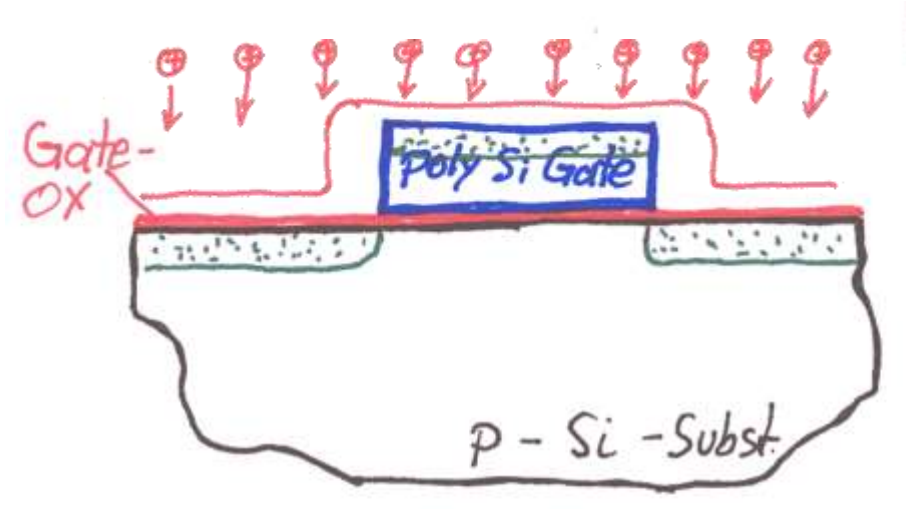


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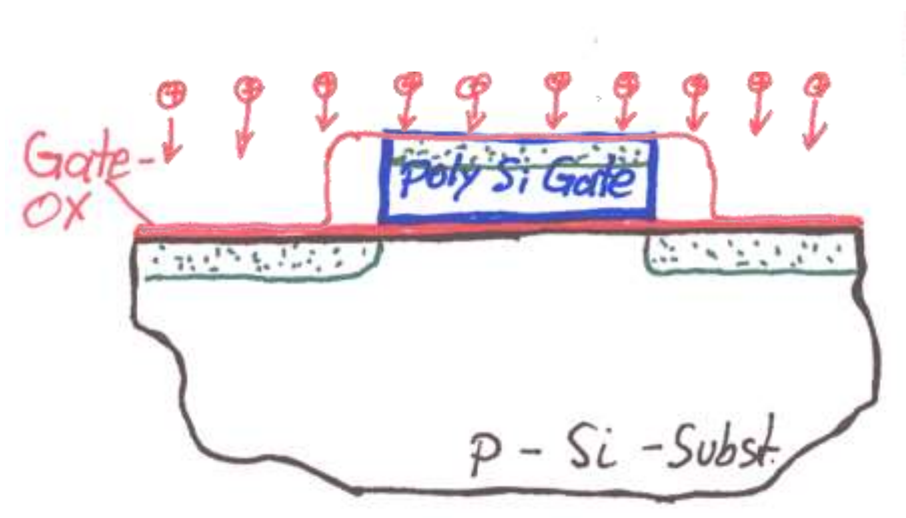


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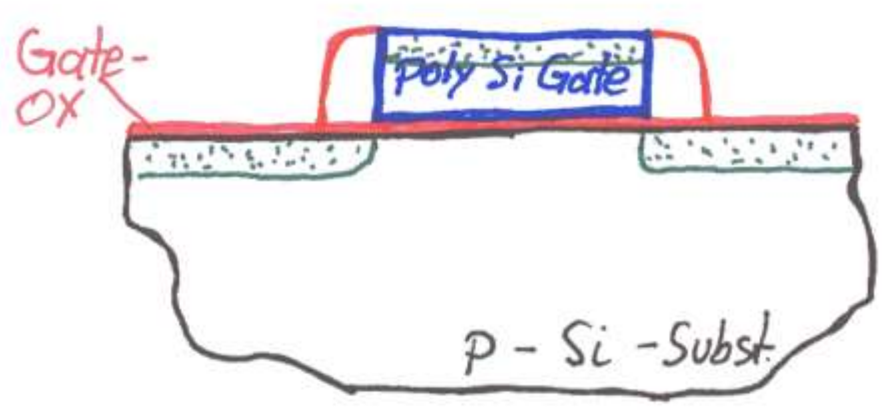

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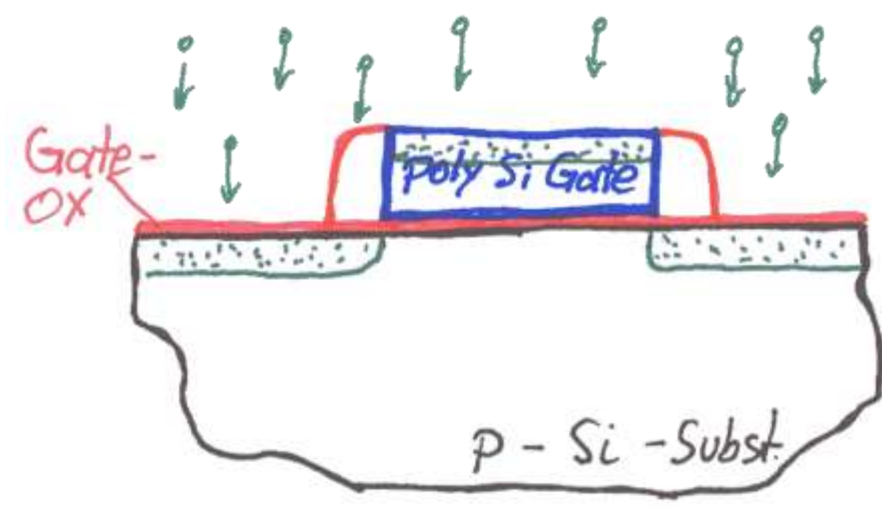


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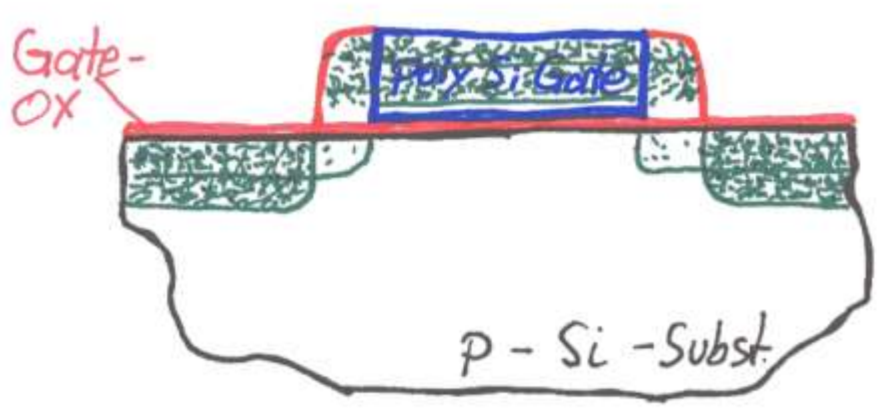


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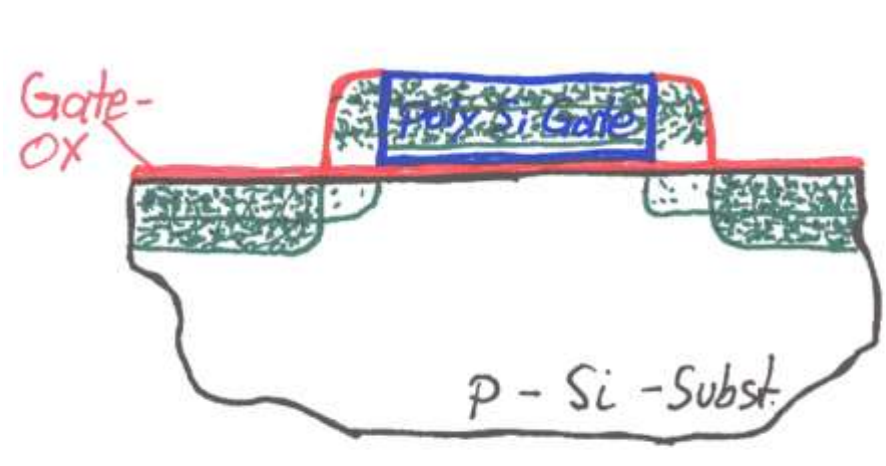


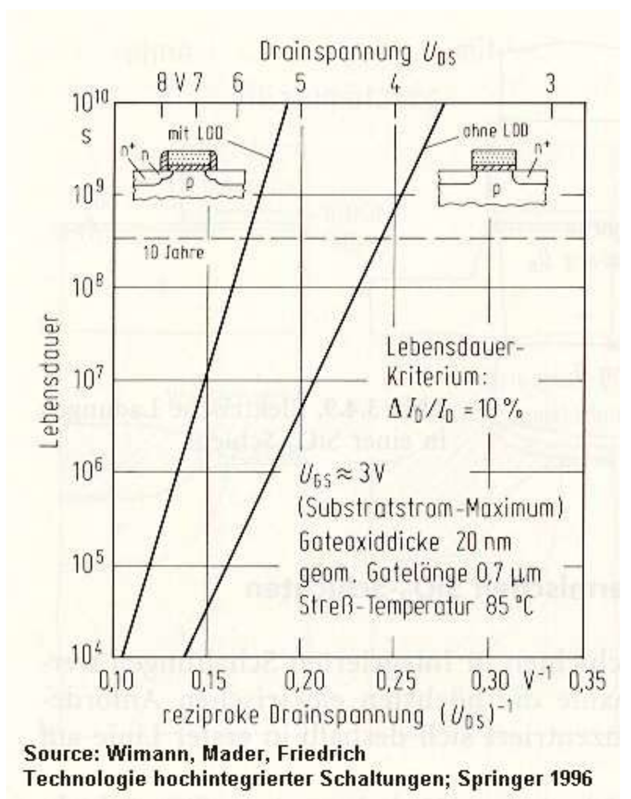

Source: Wimann, Mader, Friedrich
Technologie hochintegrierter Schaltungen; Springer 1996

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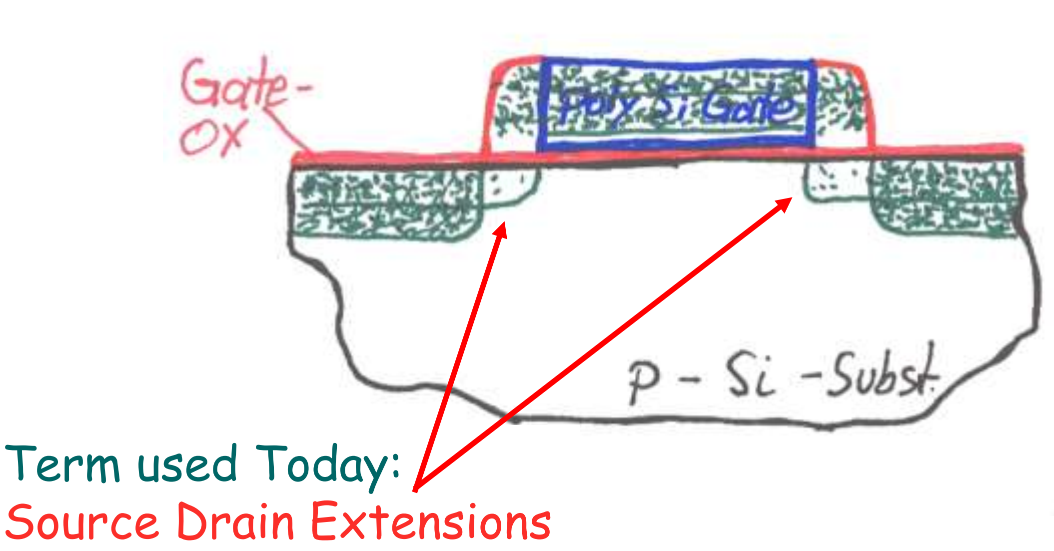
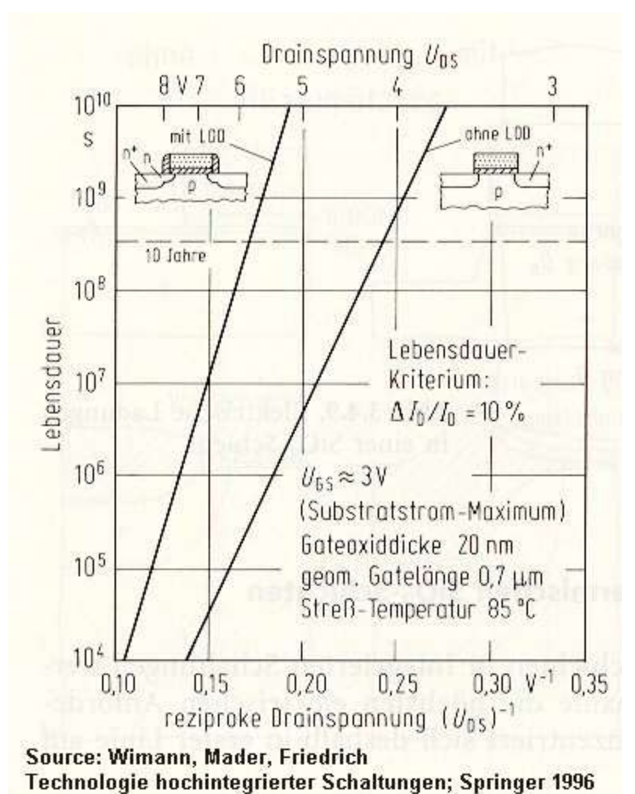



Term used Today:
Source Drain Extensions

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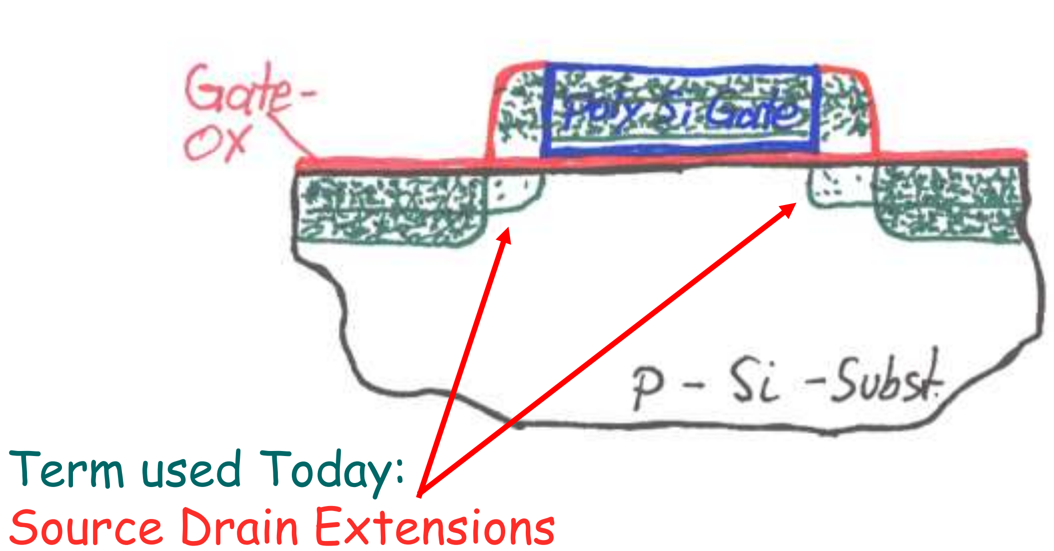


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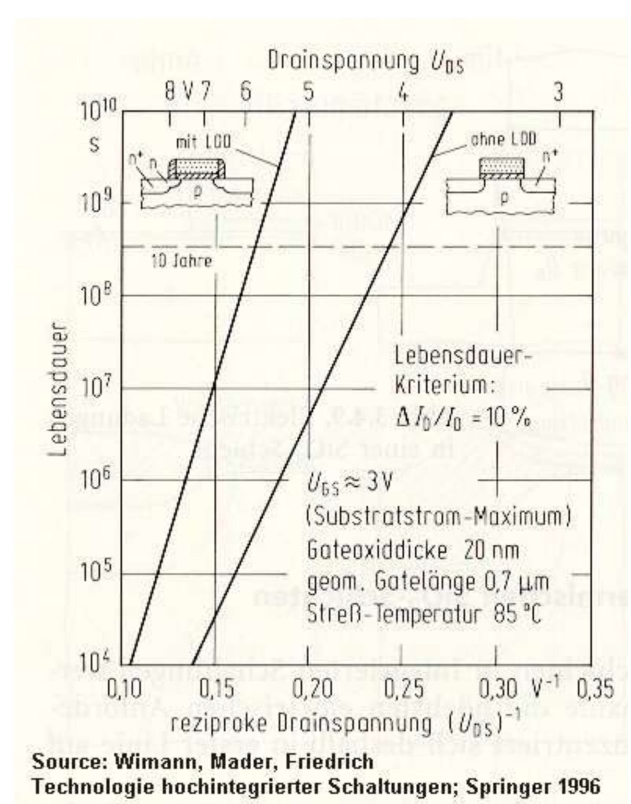


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Technologie hochintegrierter Schaltungen; Springer 1996

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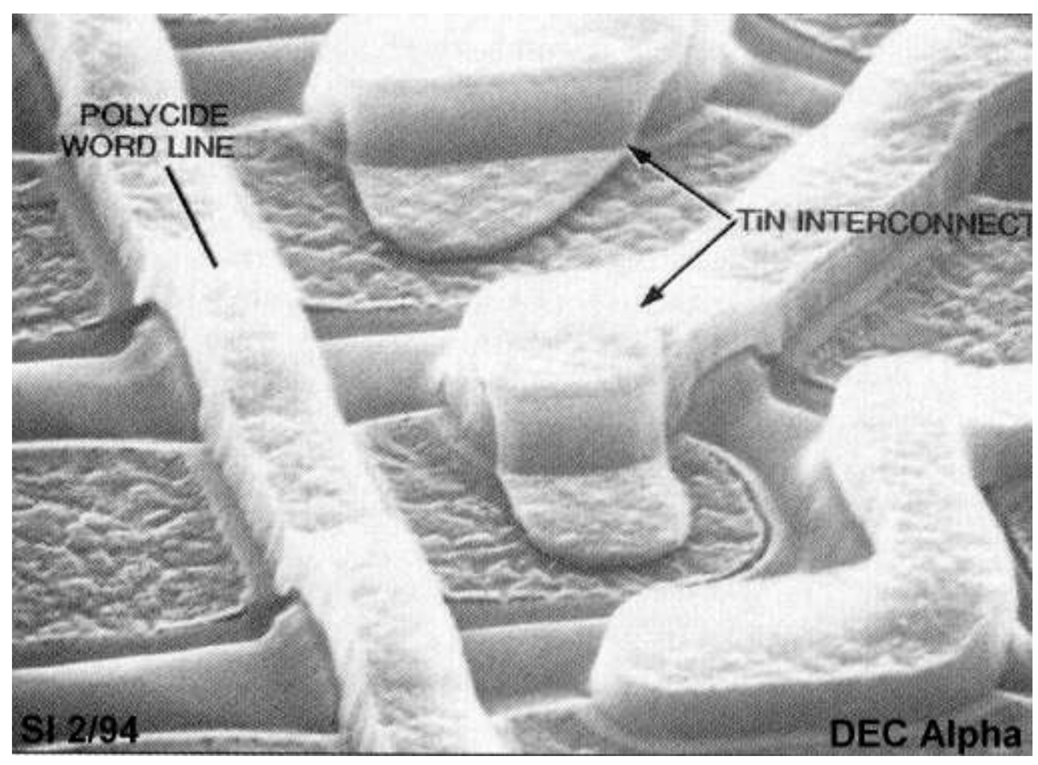
# 3.4. Self aligned Silicide = SALICIDE

Poly Si Gate Process boosted scaling but the decreasing dimensions generated new problems associated with

a) the line resistance of the poly Si gate
b) the contact resistance to S/D



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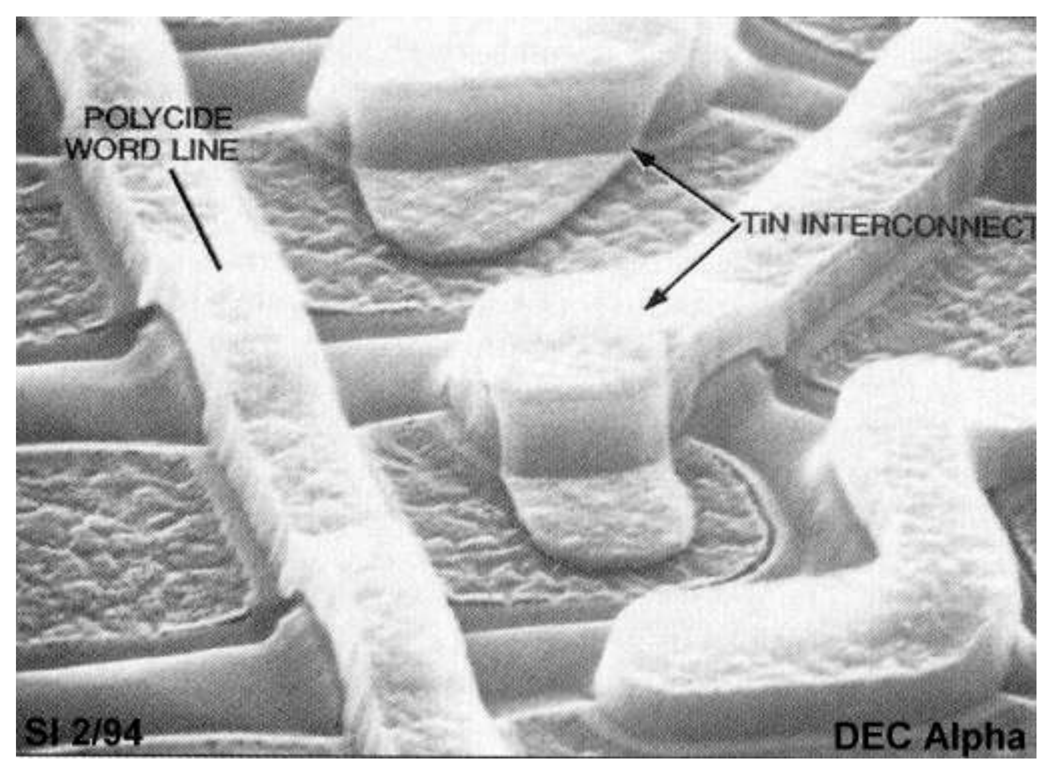
Poly Si Gate Process boosted scaling but the decreasing dimensions generated new problems associated with

a) the line resistance of the poly Si gate
b) the contact resistance to S/D

A class of materials combining low resistance and thermal stability are "silicides", which are binary compounds of metals and silicide.



# 3.4. Self aligned Silicide = SALICIDE

To optimize the performance of the MOSFET the resistivity of the gate line, as well as the resistivity of the source/drain contact should be as low as possible. This is obtained by using silicides ($WSi_2$, $TiSi_2$, $CoSi_2$).

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# 3.4. Self aligned Silicide = SALICIDE

Again this is done in a self aligned way utilizing the selective wet etch behavior between the refractive metal and the silicide.

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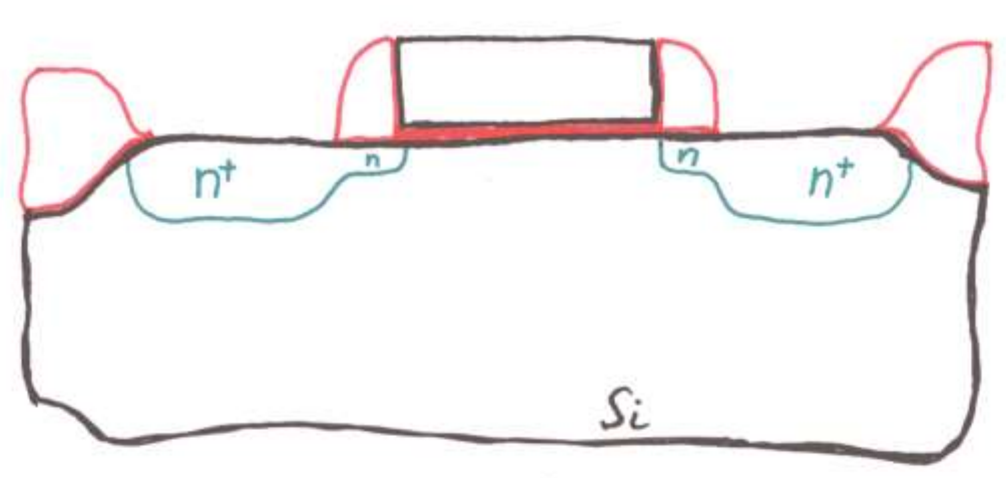

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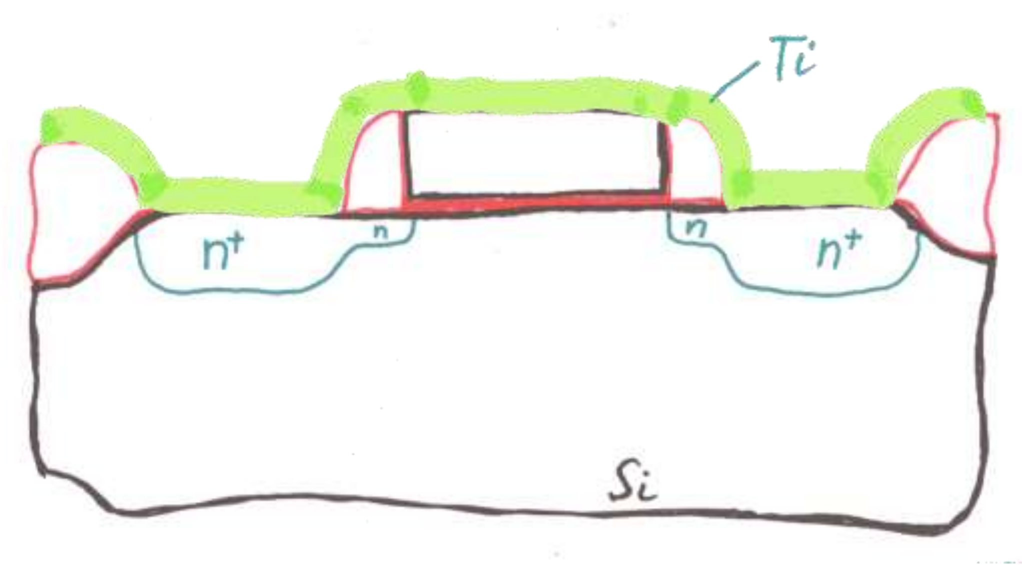


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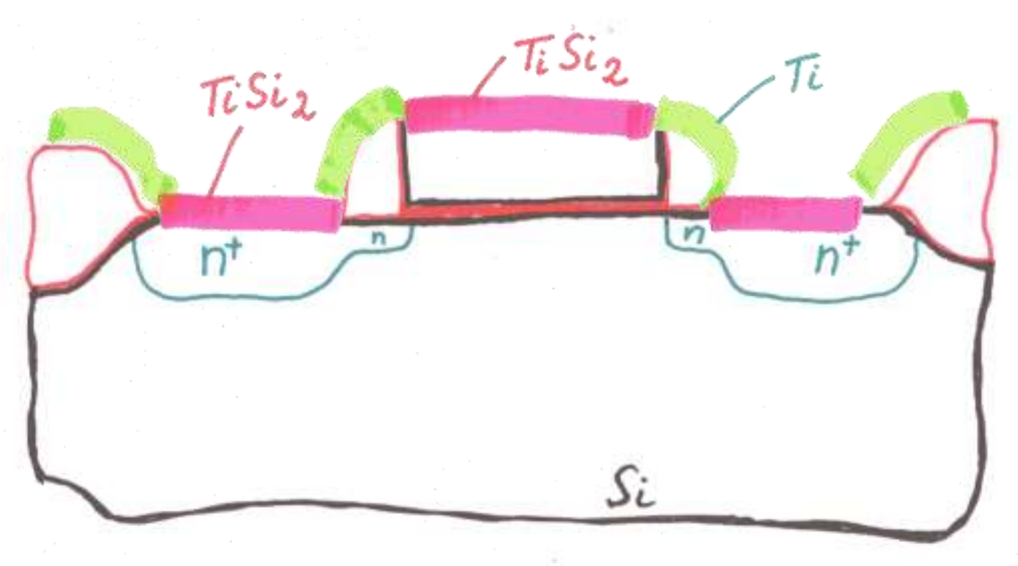

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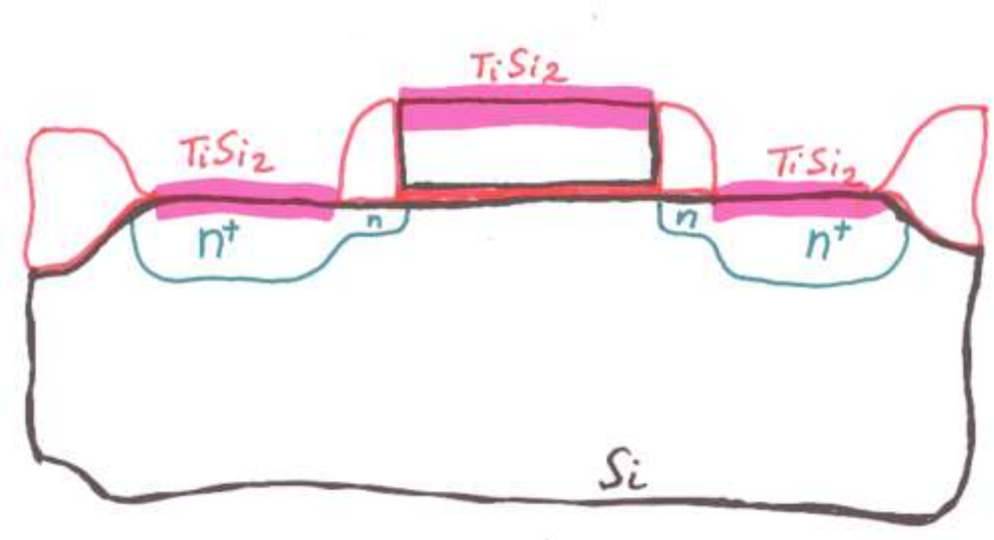


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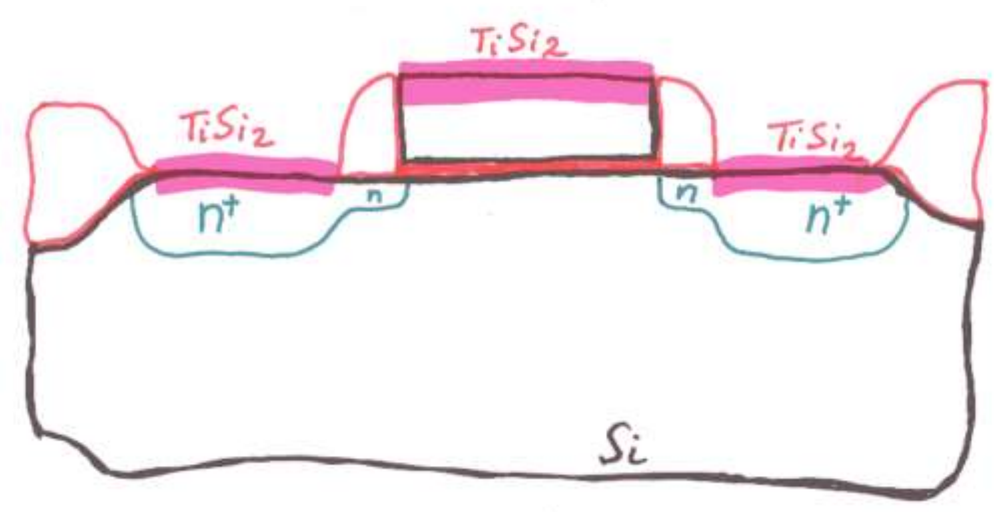
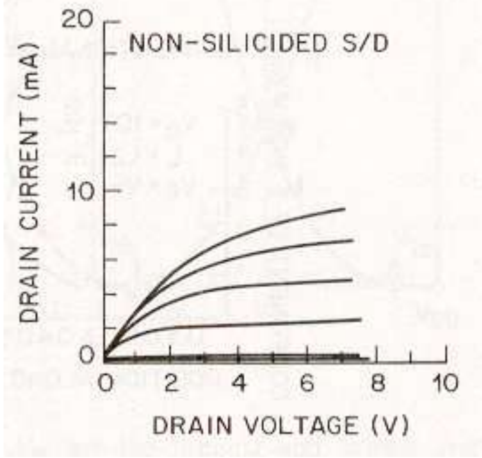
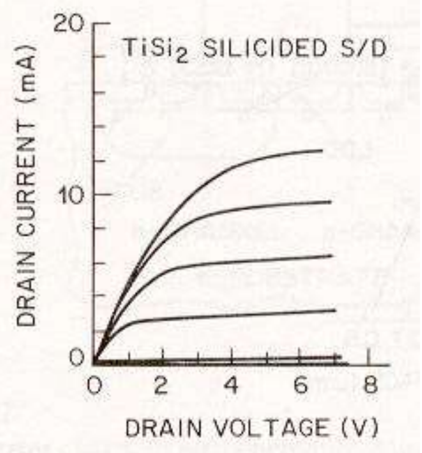



Taken from S. M. Sze, VLSI Technology McGraw-Hill 1988 →

# Source/Drain contact

L
S
Kontakt Fenster
Gate
$r_j$
Metallurgischer Übergang
$R_{ac}$
$R_{co}$
$R_{Diff}$
$R_{sp}$

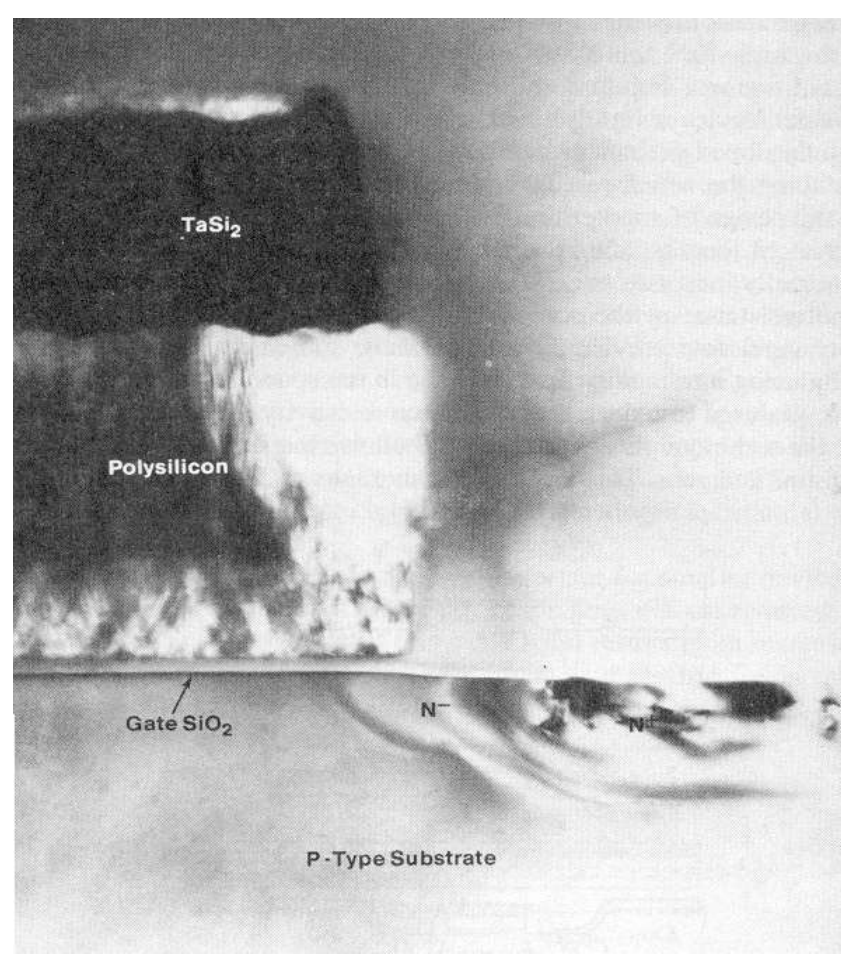
$R_{ac}$: R(Accumulation layer)
$R_{sp}$: R(spreading Resistance)
$R_{diff}$: R(Diffusion well)
$R_{co}$: R(Contact)

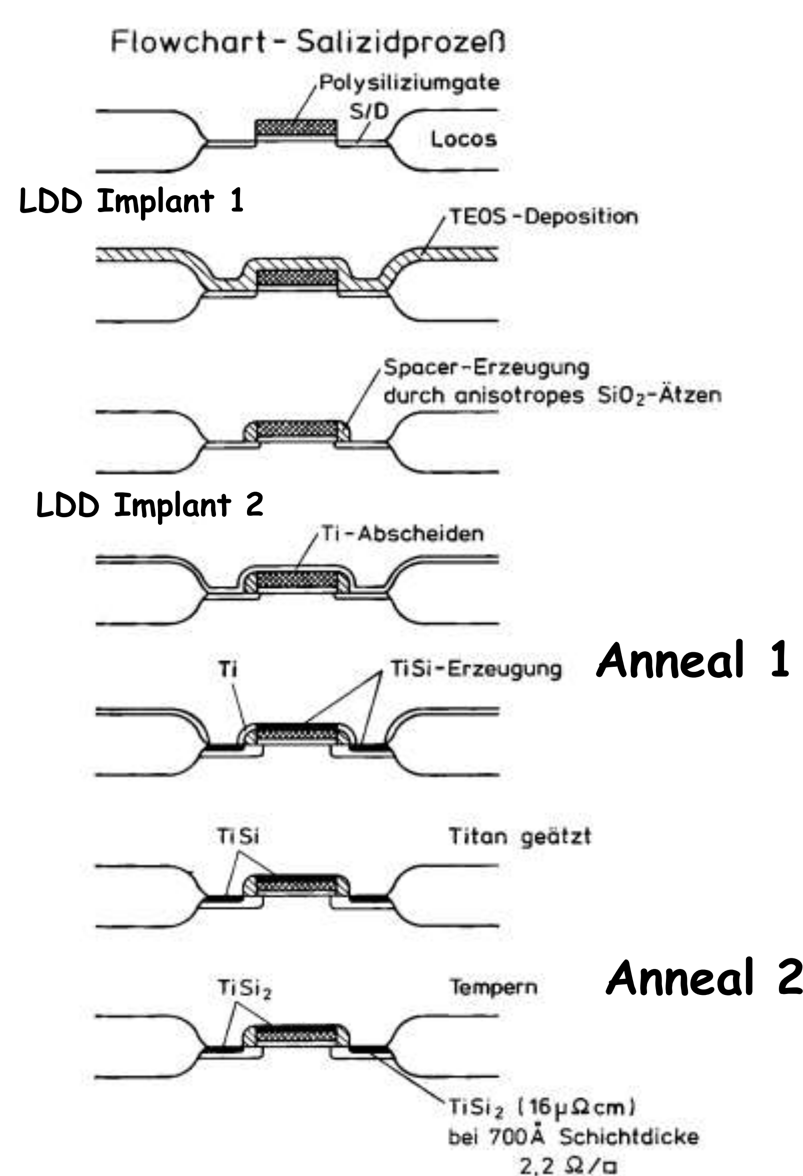
$TiSi_2$ SILICIDED S/D
DRAIN CURRENT (mA)
DRAIN VOLTAGE (V)
20
10
0
0 2 4 6 8

NON-SILICIDED S/D
DRAIN CURRENT (mA)
DRAIN VOLTAGE (V)
20
10
0
0 2 4 6 8 10

SZE VLSI

# LDD / SALICIDE

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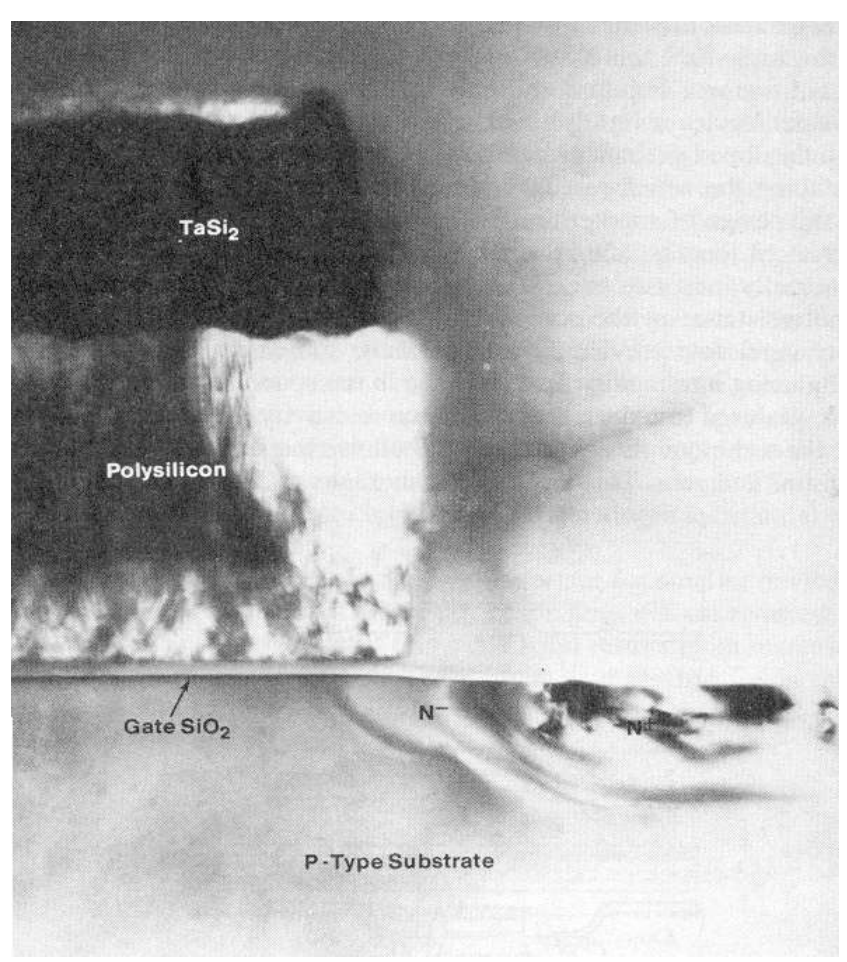
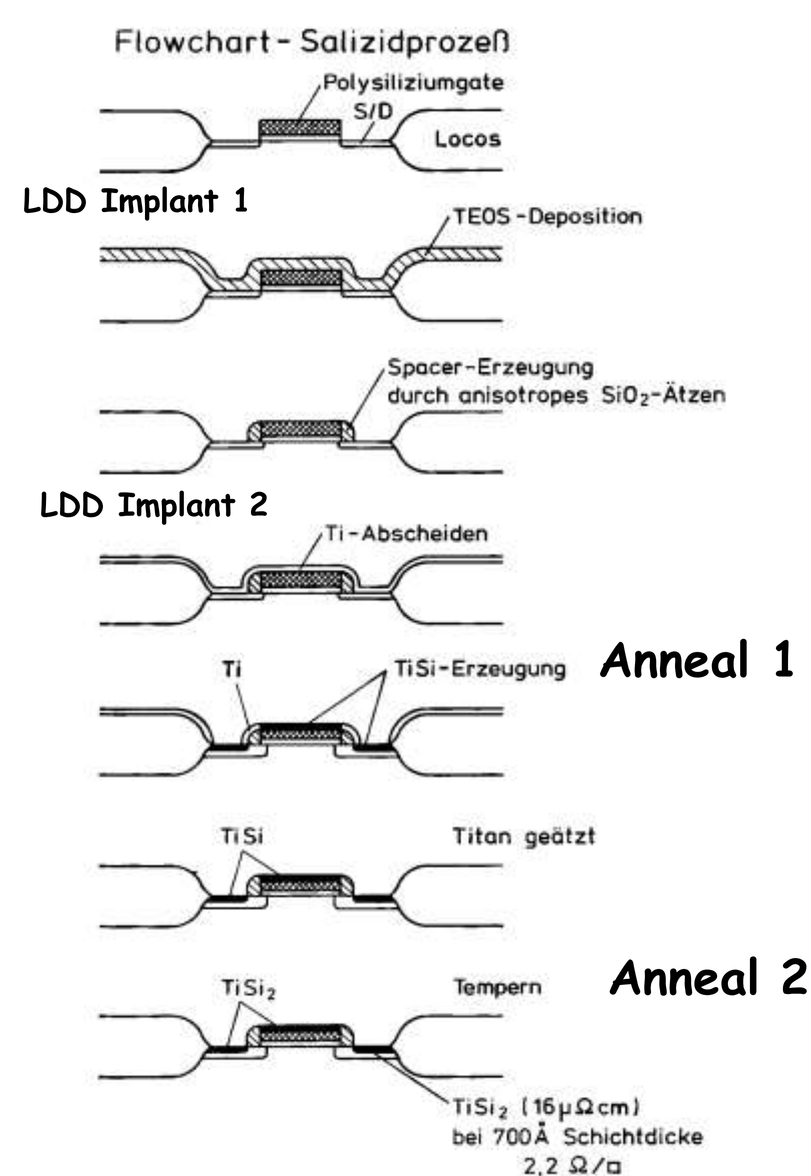
# LDD / SALICIDE



"SCT_SS20_11.04" 12:43

# 3.5. Self aligned contacts (SAC)

# 3.5. Self aligned contacts (SAC)

Oxide

Nitride cap
and liner

Gate stack

Contact to doped silicon

**Figure 2**

SEM cross-section micrograph of a self-aligned contact (SAC) structure.

(C) IBM

# Self-Aligned Contact (SAC)

% die passing

100
80
60
40
20
0

-25 -20 -15 -10 -5 0 5 10 15 20 25

Gate - Contact Shift (nm)

SAC
Non-SAC

Misalignment ←

- "Infinite" CTG window demonstrated

https://nanohub.org/resources/20935/download/2014.04.08-Mistry-NEEDS.pdf

# 3.6. Resist trimming

Shrinking (Trimming) of a structure:

Isotropic etch!

Figure 10-17

Resist trimming: resist lines made narrower by isotropic etching of the resist in oxygen plasma. In both cases the resolution (line + space) remains constant.

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# Outline


0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1. MOS Structure, MOS Capacitor
    2. Structure of a MOSFET
    3. I/V behavior
2. Circuits in Metal-Gate FET Technology
    1. Process sequence of N-MOSFET in Metal Gate
    2. From inverter to memory cell
    3. SRAM in NMOS Metal Gate
    4. The threshold voltage of the MOSFET
        1. Parasitic FET
        2. Enhancement/Depletion Transistor
        3. N-MOS Logic by E/D Transitors
        4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1. Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1. Example: Process flow of E/D SiGate LOCOS Inverter
        2. LOCOS Variation
        3. Shallow Trench Isolation
    3. Lightly doped drain
    4. SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4. Transition to CMOS Technology
    1. MOS Transistor Types
    2. CMOS Inverter
        1. Consideration NMOS E/D Inverter
        2. Comparison CMOS Inverter
    3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1. Scaling
        1. Challenges
        2. Material Equivalent Scaling
        3. Further Concepts


SC-Basics

http://www.computerhistory.org/siliconengine/timeline/

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