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Lecture SCT2 – Process Integration

12. Web-based virtual Lecture: July 08 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here  

"SCT_SS21_12.1" 37:08

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Lecture evaluation open until July 08!

Please participate in the lecture evaluation!

Deutsch English

TECHNISCHE UNIVERSITÄT DRESDEN

ZQA

ZENTRUM FÜR QUALITÄTSANALYSE

Portal der Lehrveranstaltungsevaluation der TU Dresden

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Herr Prof. Dr. Bartha - Vorlesung "Semiconductor Technology 2": Questionnaire

Dear students,

You will be offered the possibility of feedback on the above-mentioned course.

Your teacher and the ZQA kindly ask you to fill in the questionnaire.

Introductory question:

How is the proportion of online teaching in this lecture?

○ This is a pure online lecture. ○ It is a mix of presence and online teaching. ○ This is a pure on-site lecture.

Questions about the lecturer: The lecturer ...

	Completely correct	Mainly correct	Partly	Mainly incorrect	Completely incorrect
1. ...presents the goals of the lecture in an understandable manner.	○	○	○	○	○
2. ...organizes the lecture well. There is a central theme.	○	○	○	○	○
3. ...comes across as dedicated and enthusiastic in the lectures.	○	○	○	○	○
4. ...designs the learning materials (presentation					

Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

Review:
- SCT Basics
- MOS-Cap-CV
- MOS-FET (N-FET enh.)
- Al-Gate FET
- SRAM product (E/E)
- V_T adjust => Depl.
- E/D Logic
- Self aligned process
  Si-Gate, LOCOS, STI, LDD, SALICIDE, SAC, Resist Trimming

Today: CMOS

http://www.computerhistory.org/siliconengine/timeline/

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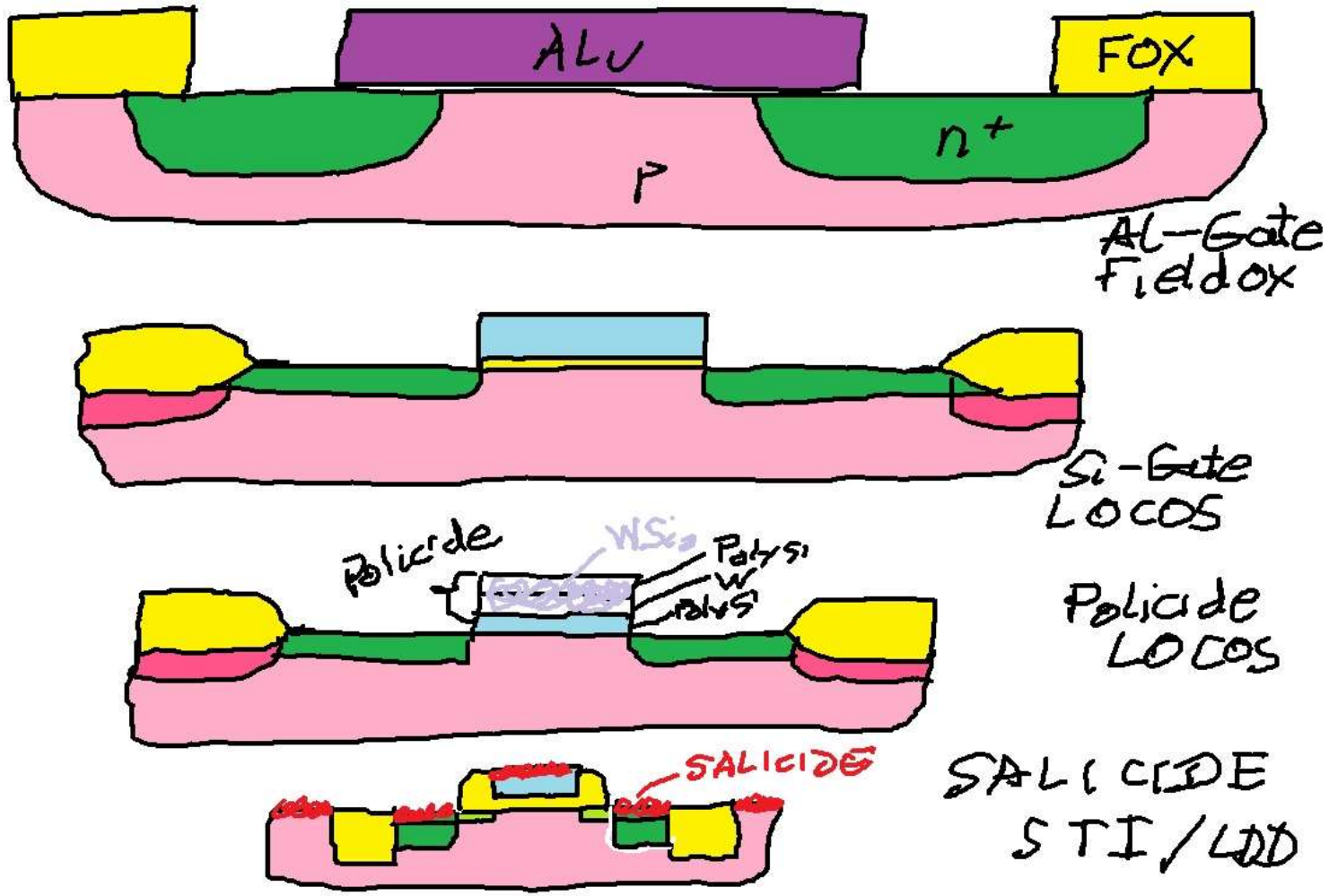
Today: CMOS

Continue ➡ VIDEO CAMPUS SACHSEN

"SCT_SS20_12.2" 21:00

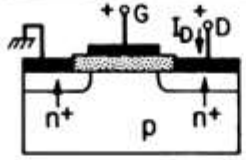
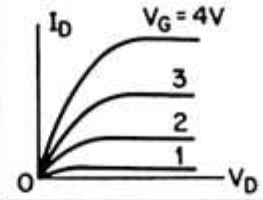
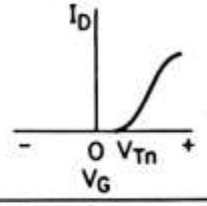
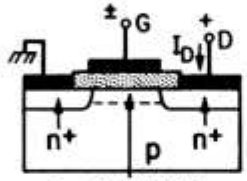
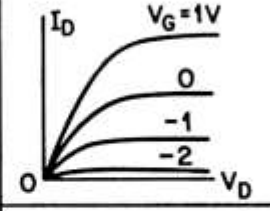
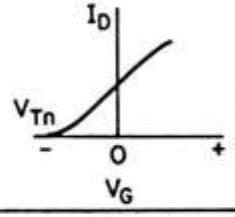
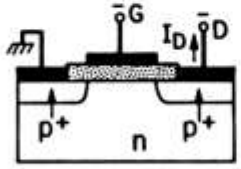
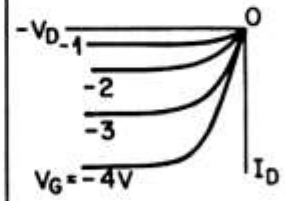
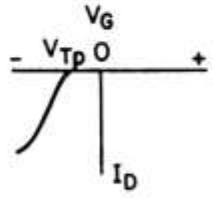
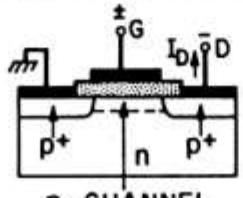
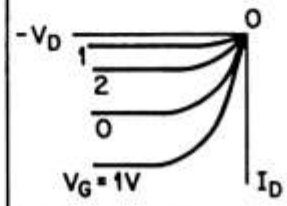
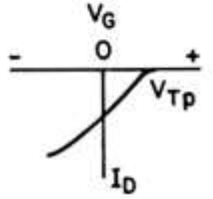
http://www.computerhistory.org/siliconengine/timeline/

Blackboard 12.1



4. Transition to CMOS Technology

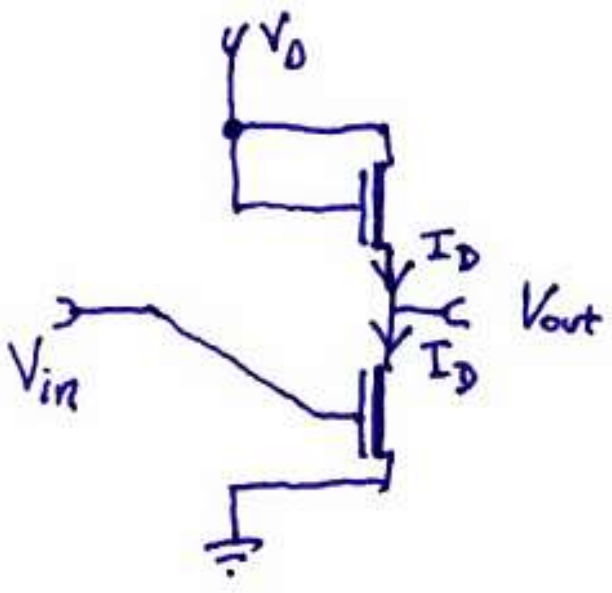
4.1 Different Types of MOSFET

TYPE	CROSS SECTION	OUTPUT CHARACTERISTICS	TRANSFER CHARACTERISTICS
n-CHANNEL ENHANCEMENT (NORMALLY OFF)			
n-CHANNEL DEPLETION (NORMALLY ON)			
p-CHANNEL ENHANCEMENT (NORMALLY OFF)			
p-CHANNEL DEPLETION (NORMALLY ON)			

4.2 Transition to the CMOS inverter

4.2.1 Remember: E/E inverter

Remember
the N-MOS Inverter!



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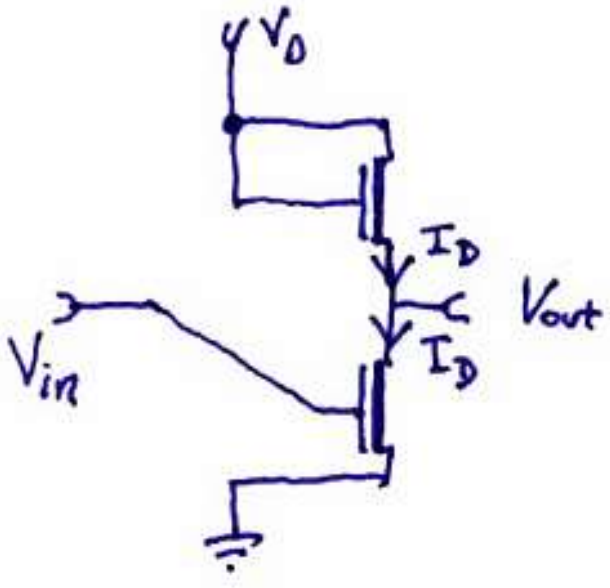
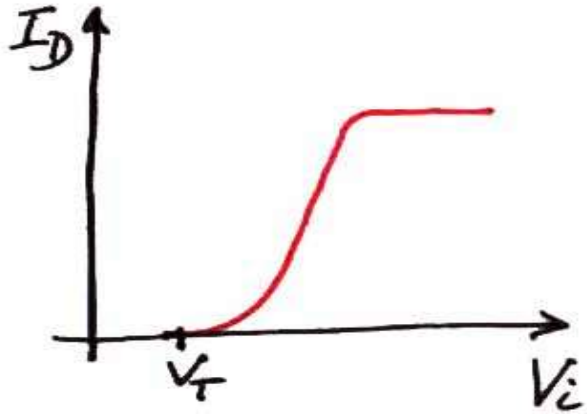


When V_i is increased from zero to V_D, a current flows through the load transistor for $V_i > V_T$ and reaches a saturation value controlled by the load transistor.



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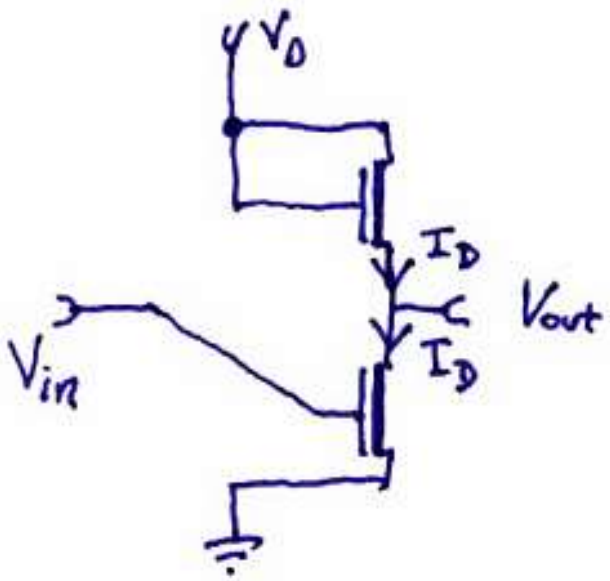

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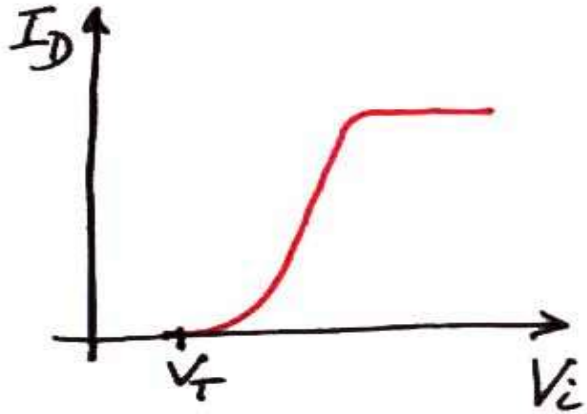


☹ When the input is high, the inverter consumes continuously power!

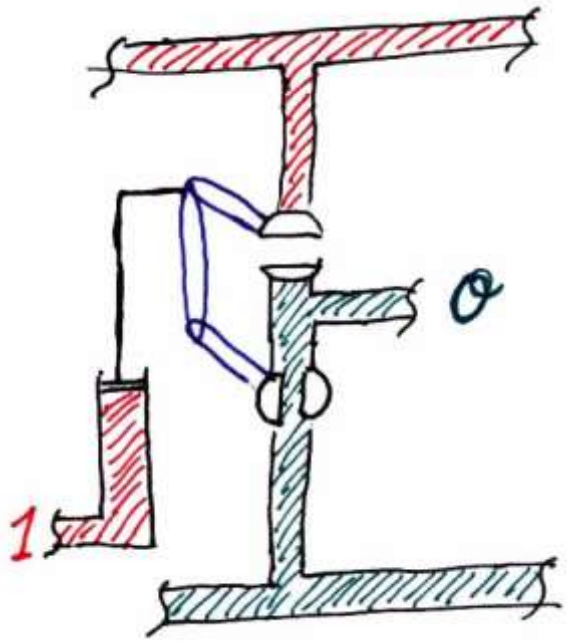
4.2.2. Hydrodynamic analogy: CMOS Inverter

Instead of the load device it would be much nicer to have a switching device that operates complementary!

4.2.2. Hydrodynamic analogy: CMOS Inverter

Instead of the load device it would be much nicer to have a switching device that operates complementary! Like the two valves controlled by the piston.

Operation state 1



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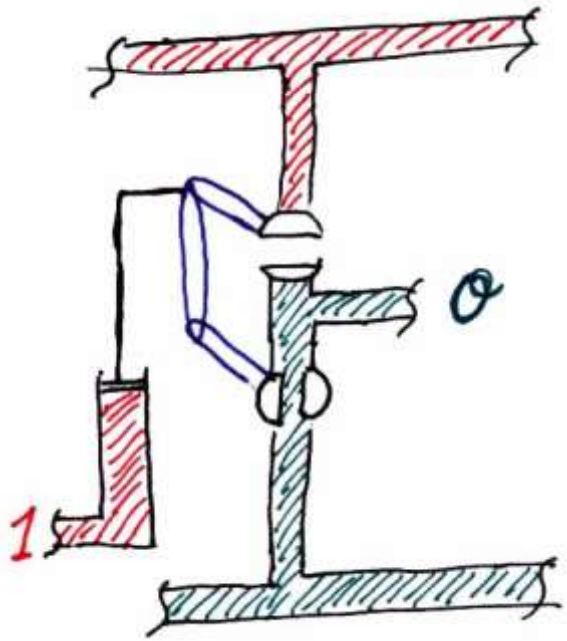
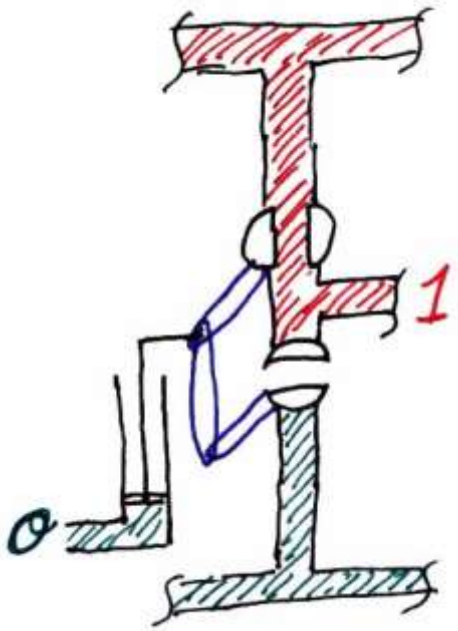


Operation state 2



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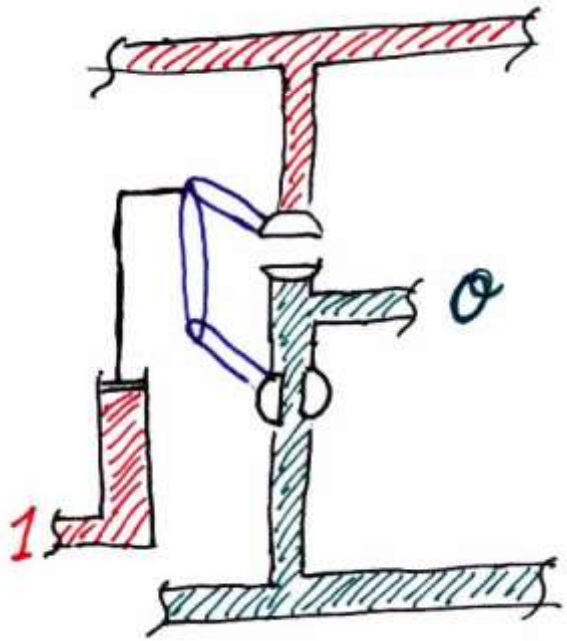
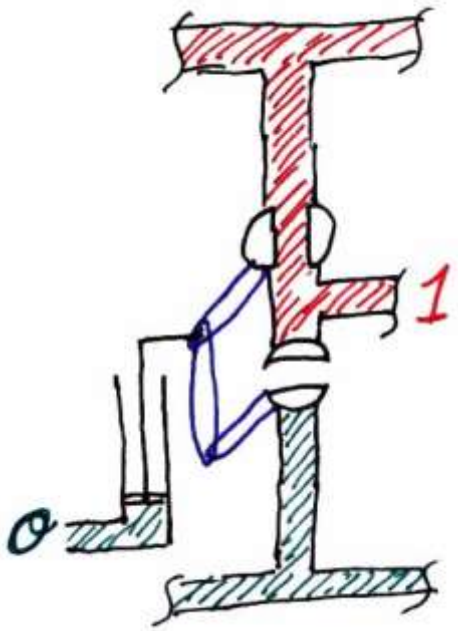
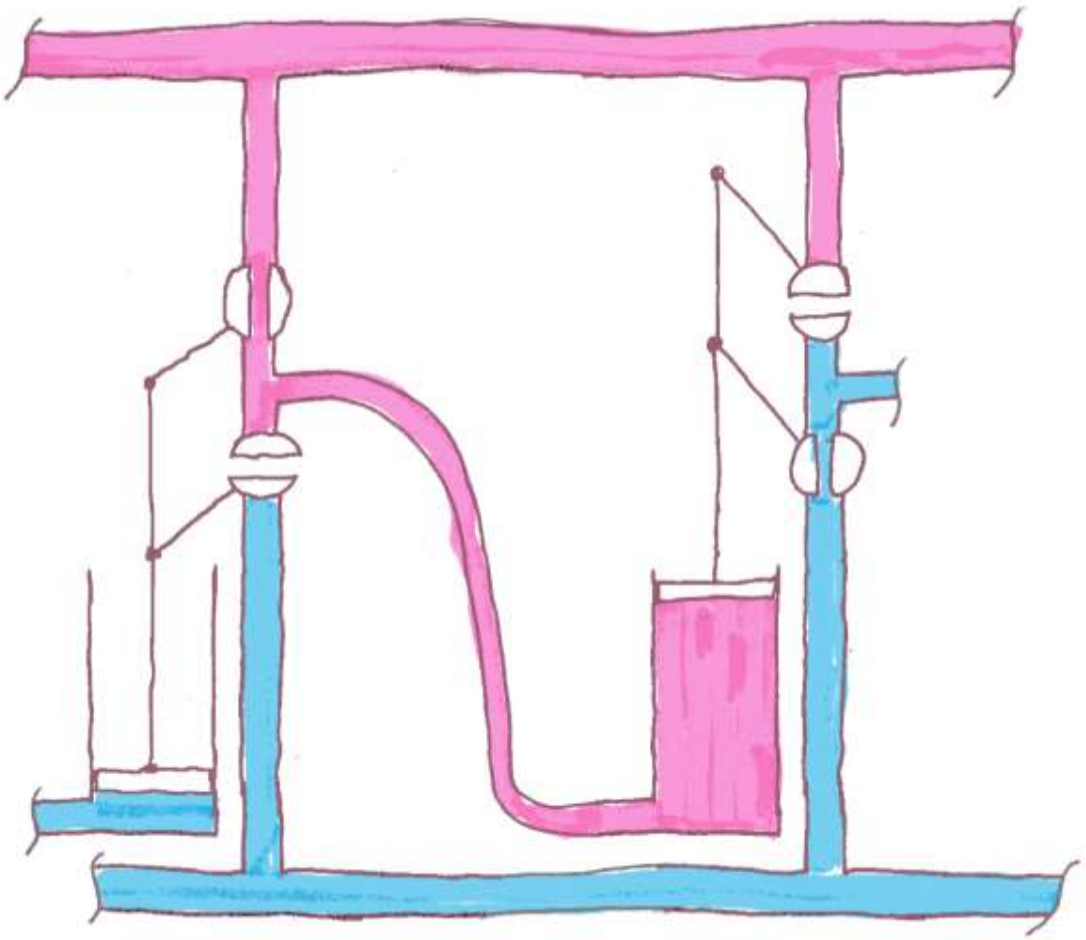


Operation state 2



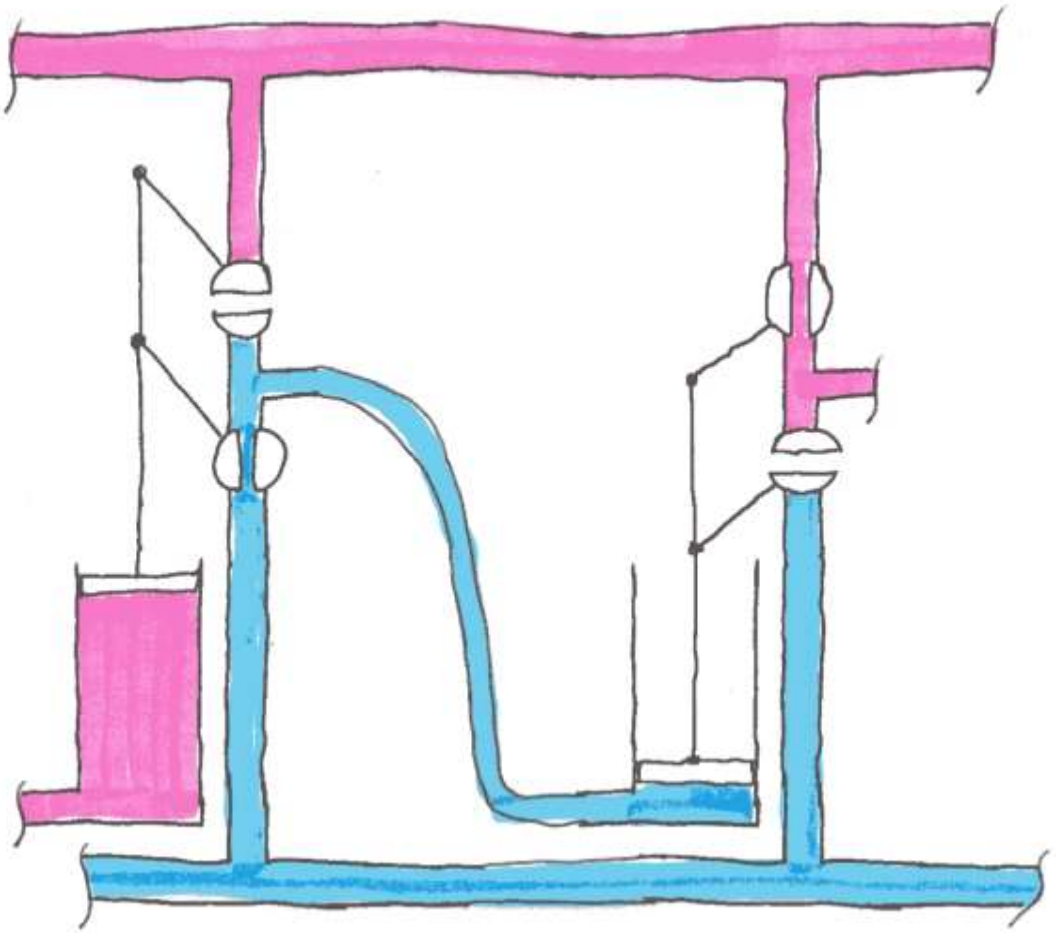
Something like this can be done by combining a N-MOS and a P-MOS FET:

Process - integration



Application example:
Ring Oscillator

Process - integration



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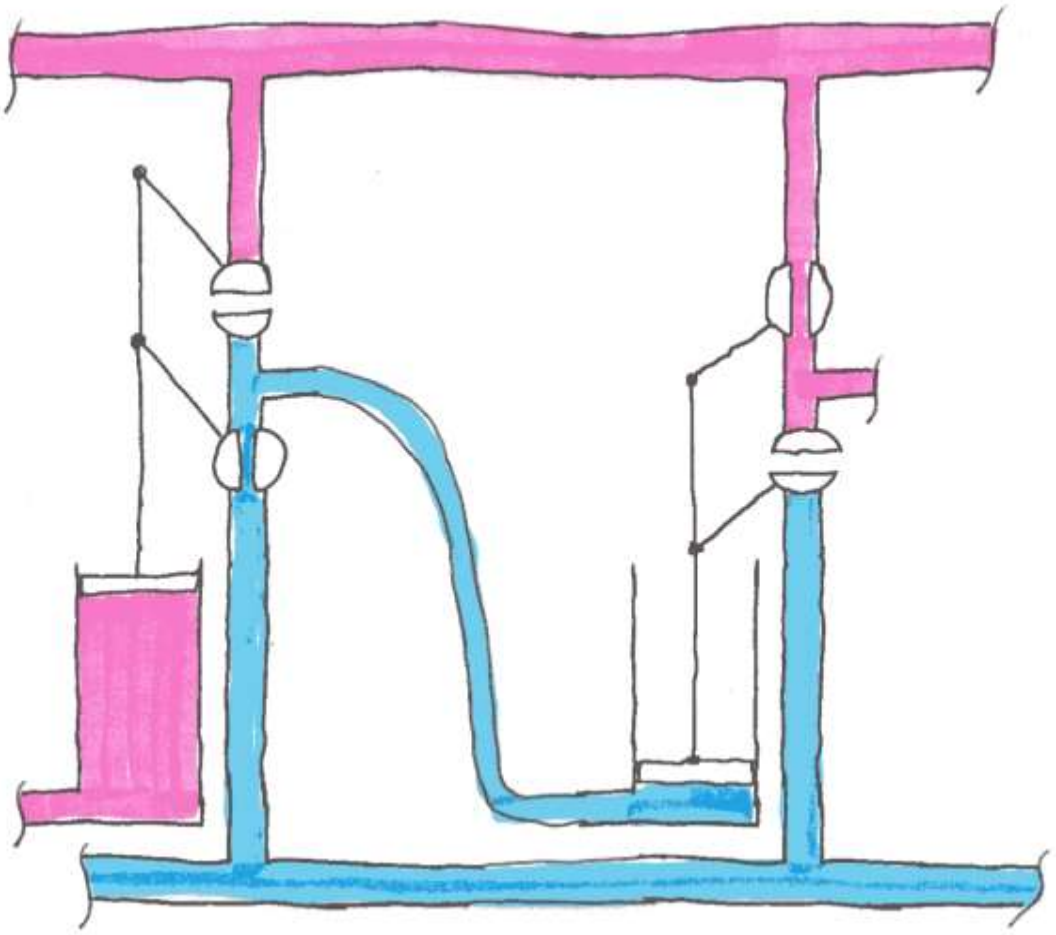
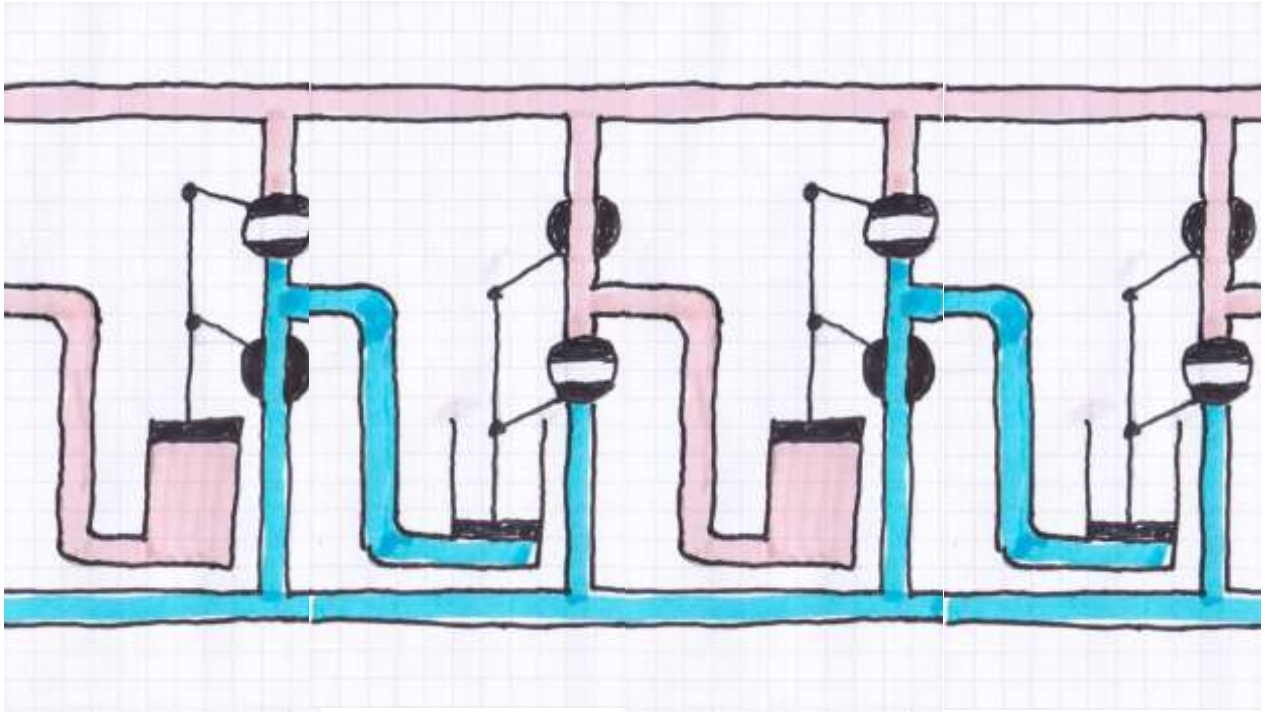


Application example:
Ring Oscillator

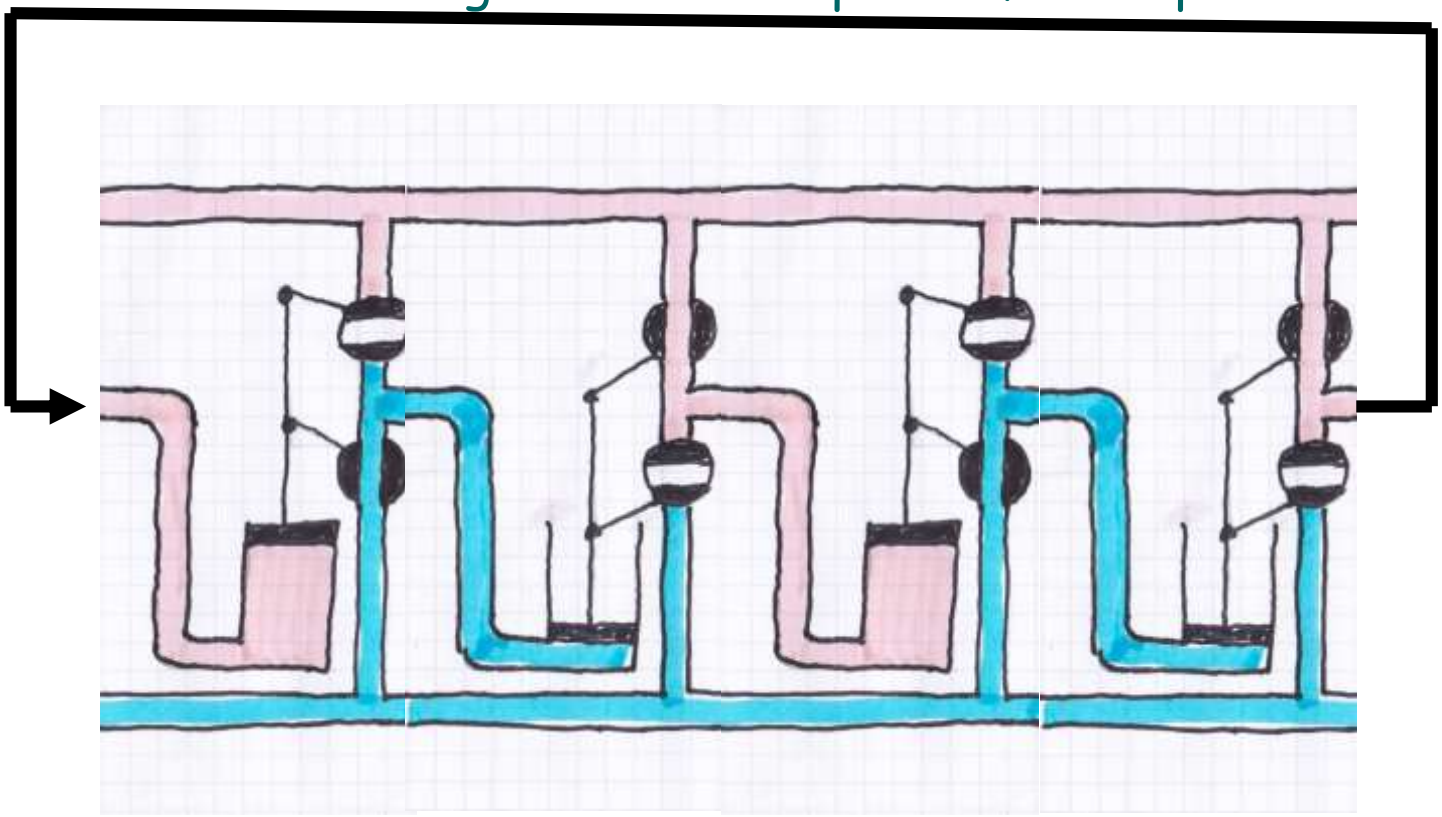
Multiple stage ring oscillator can be nicely used to determine the switching speed of a circuit technology. The more stages the more easy to measure.

Application example: Ring Oscillator



Application example: Ring Oscillator

Feeding back last output to first input:



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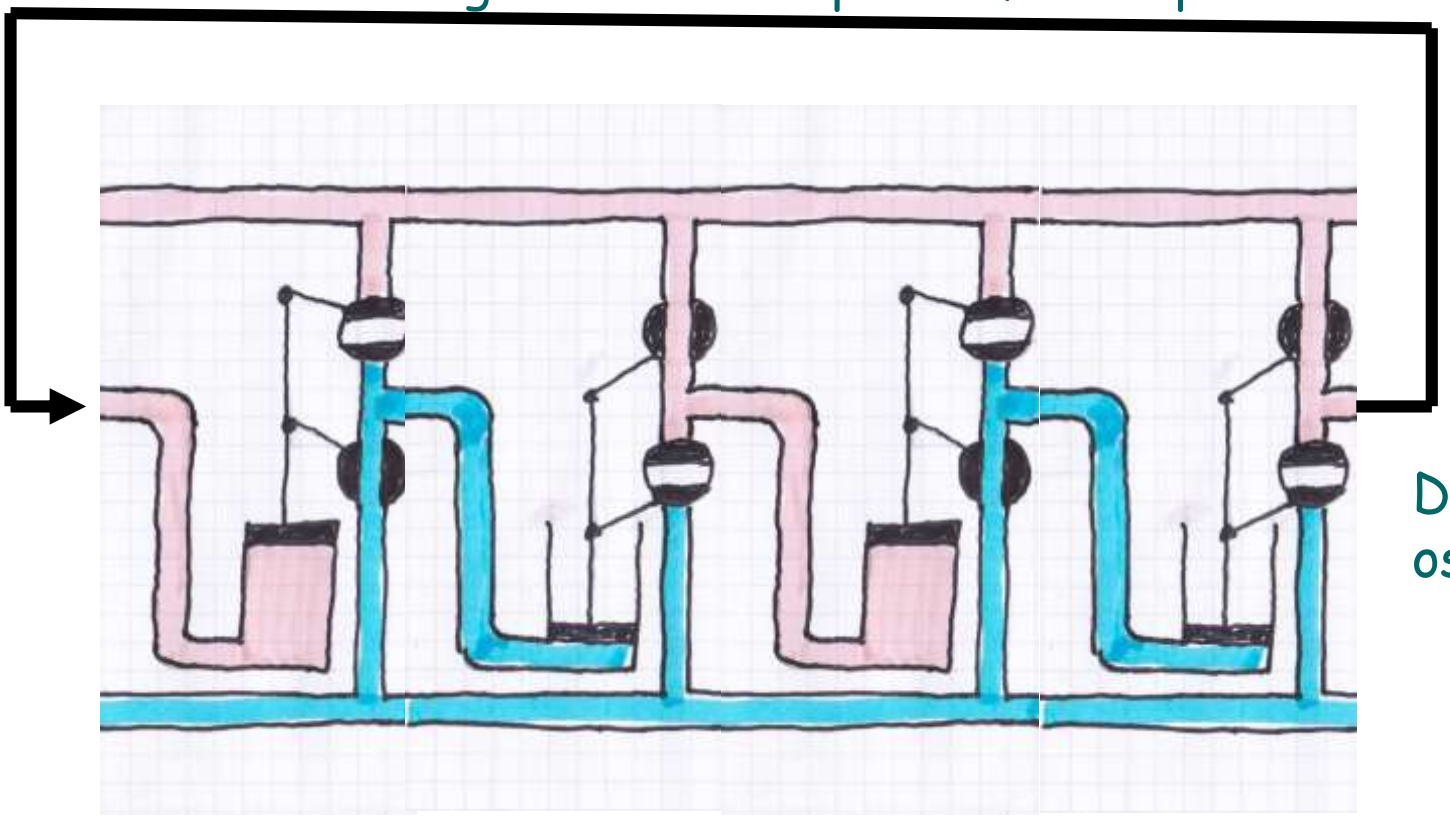

Does this circuit oscillate ?

Application example: Ring Oscillator

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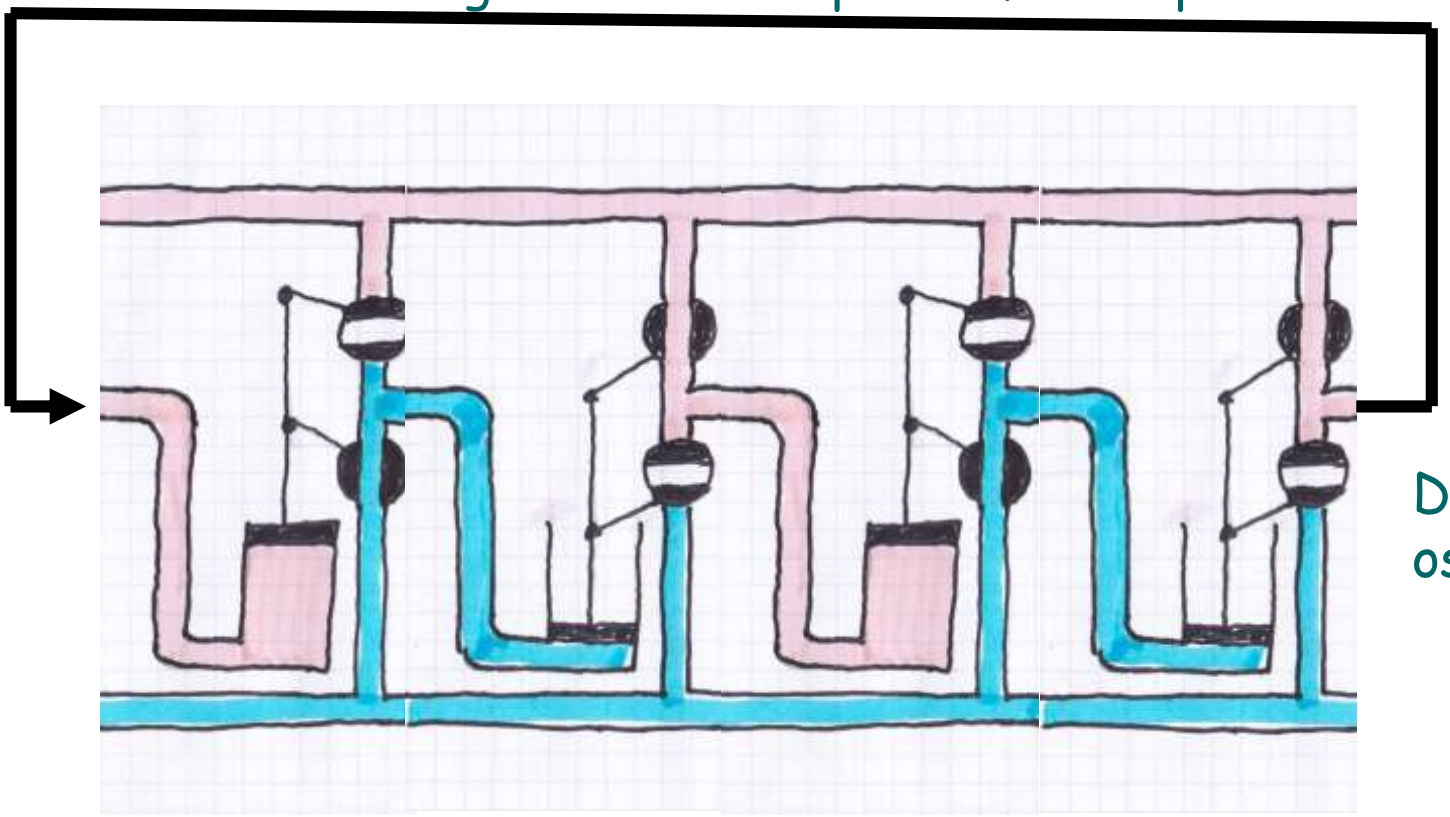
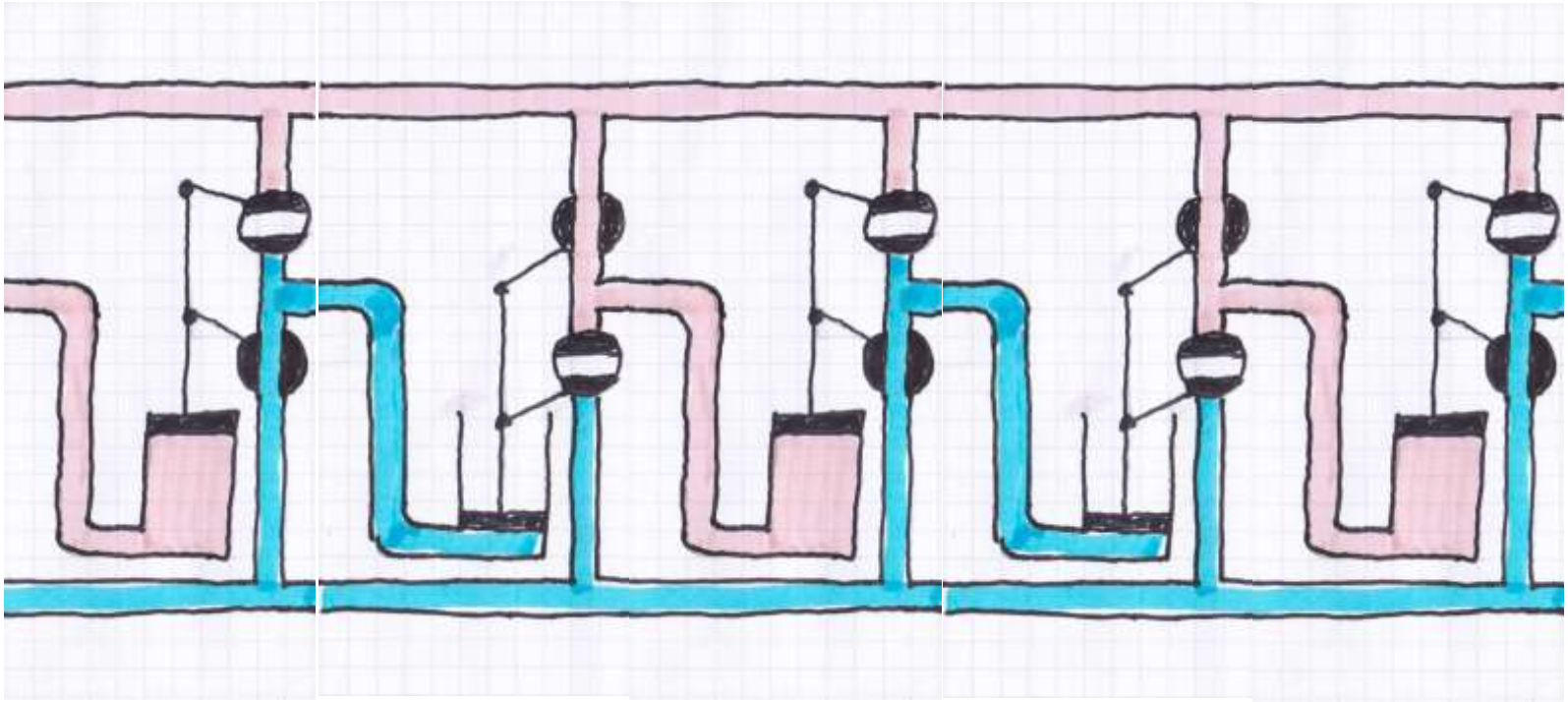
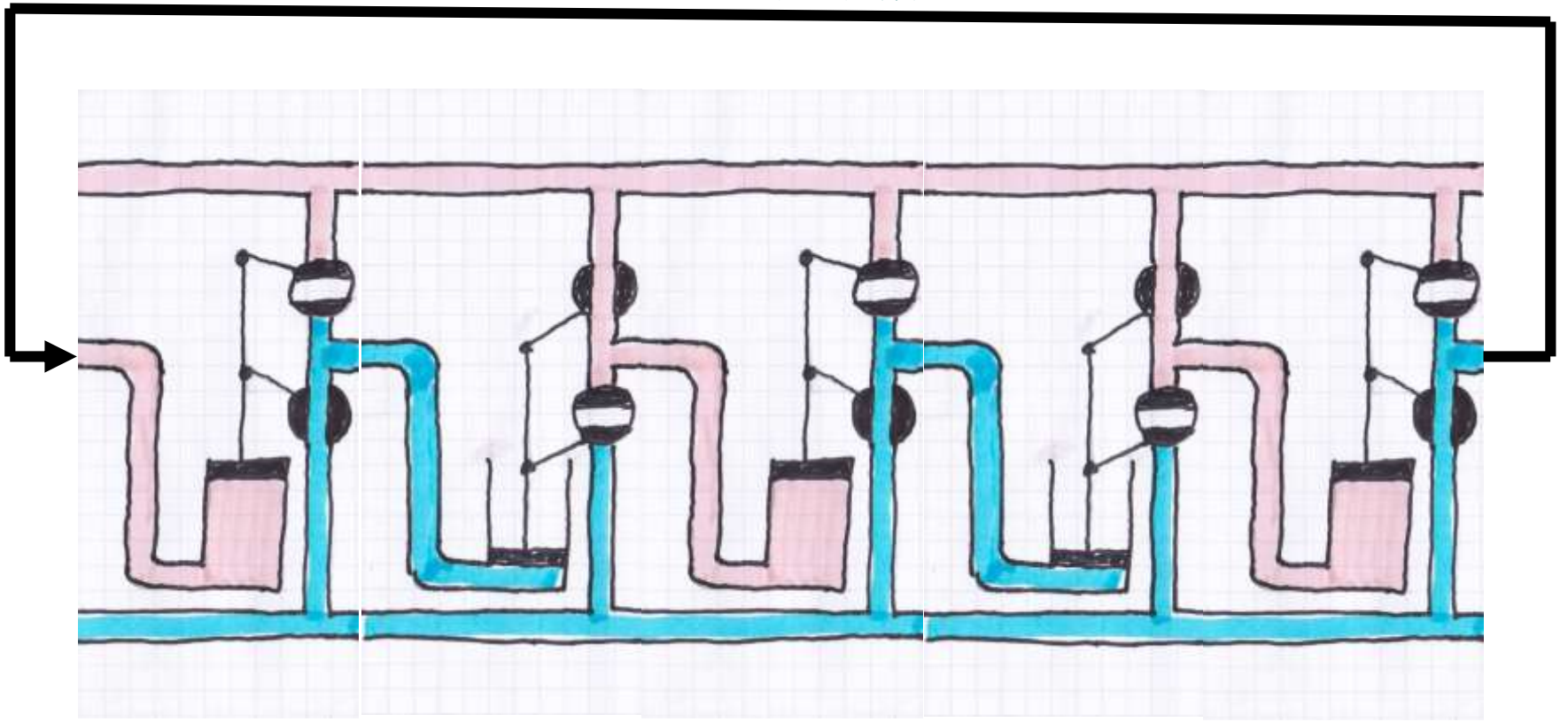


Does this circuit oscillate ?

No! Last output and first input are both on high.
No reason to change the state!

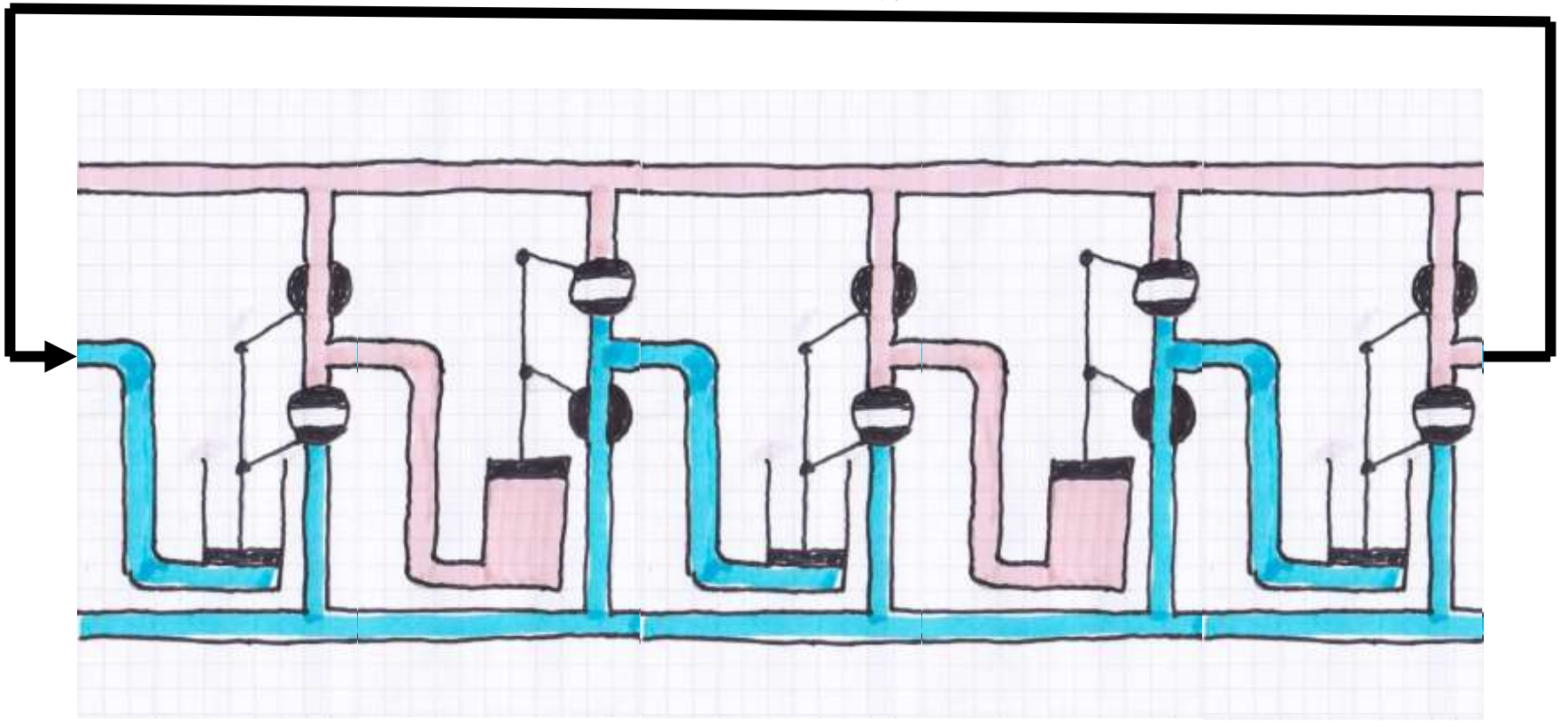


And now?



Odd number of inverters required!

And now?



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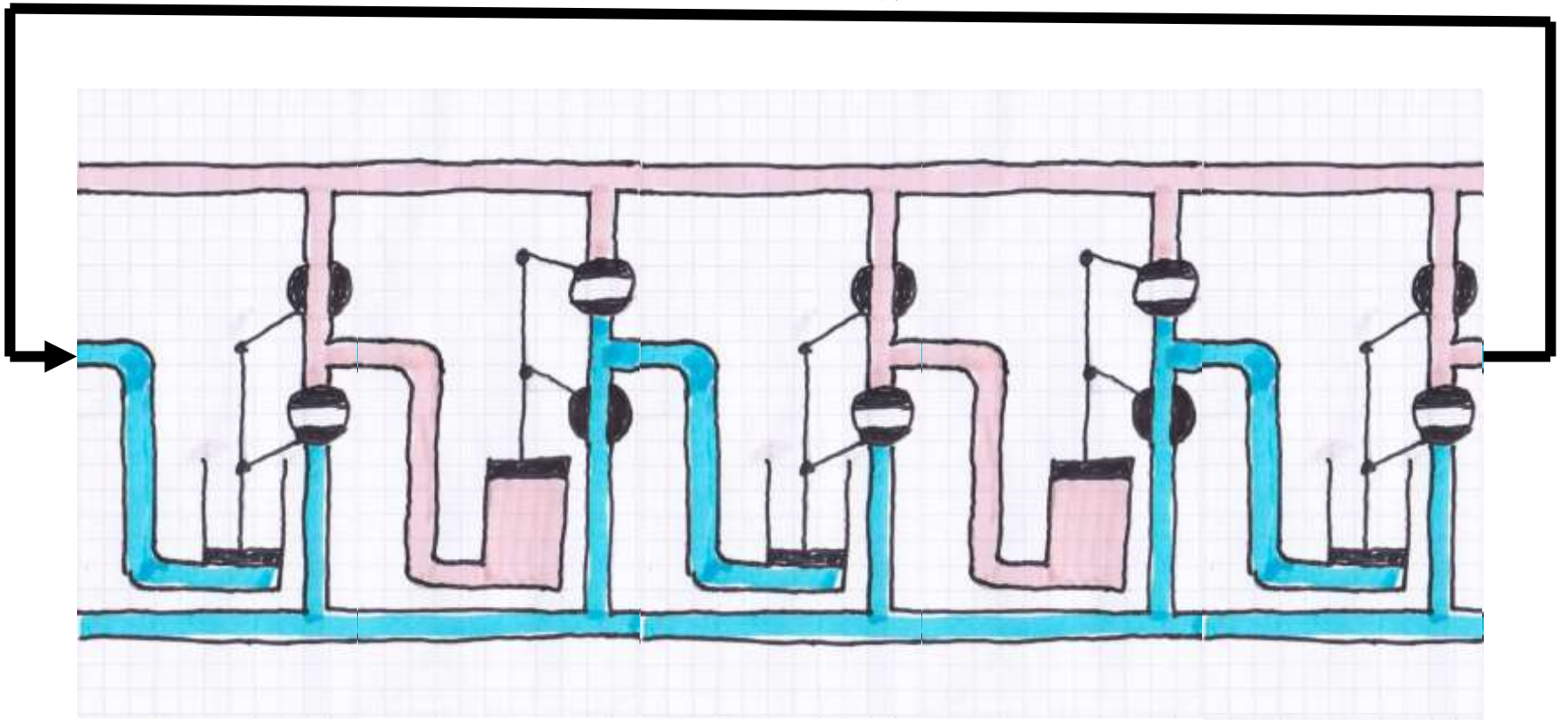

Back to realization of an inverter with an active load by using N-MOS and P-MOS FET

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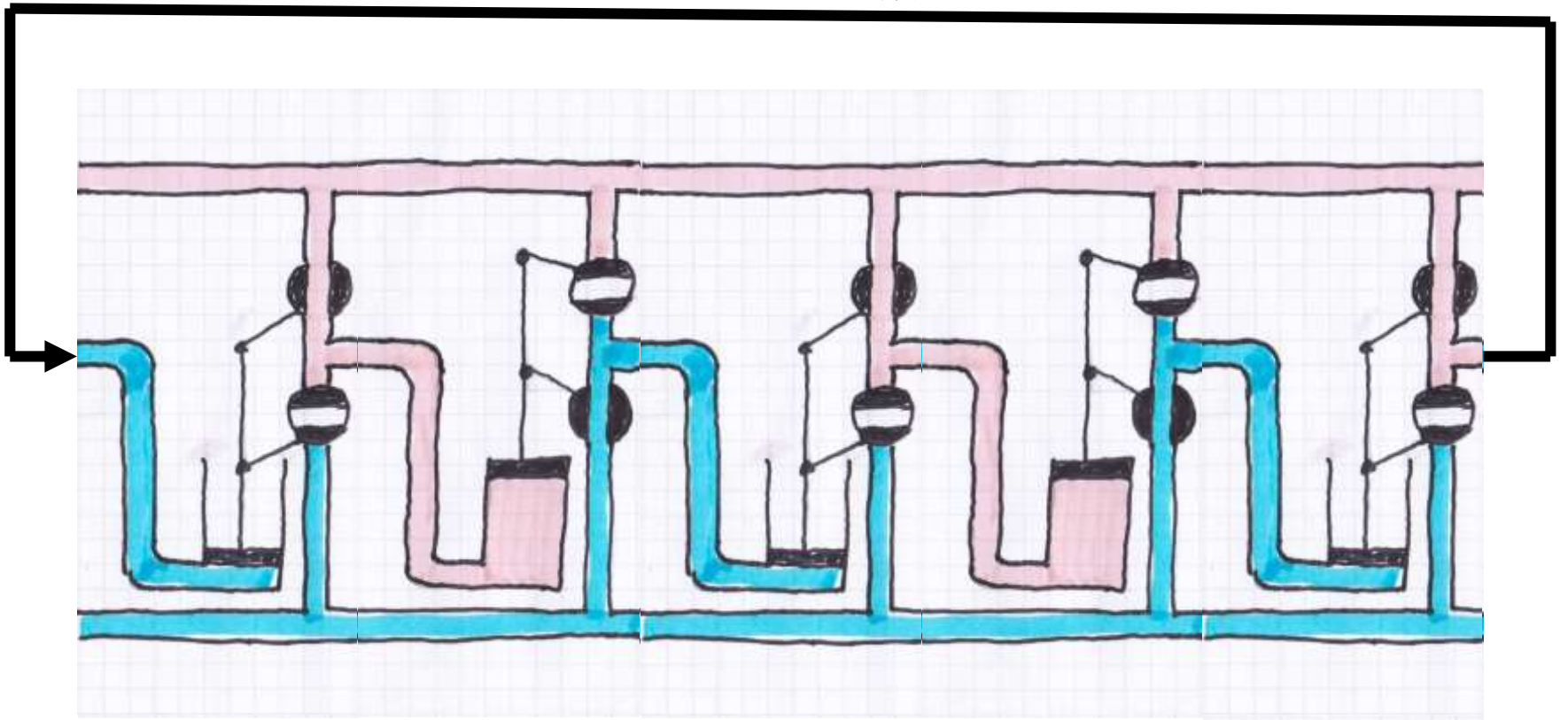

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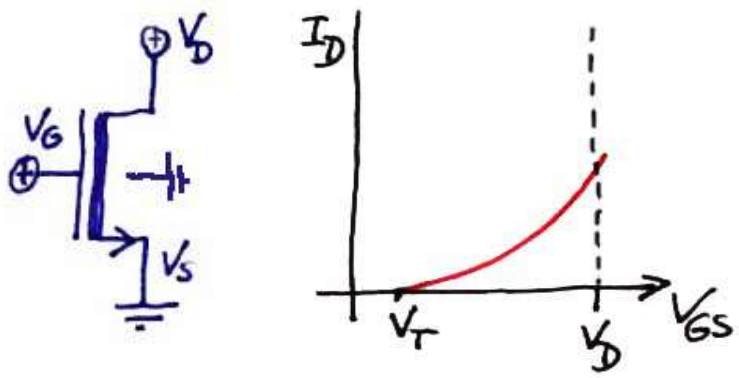
Back to realization of an inverter with an active load by using N-MOS and P-MOS FET

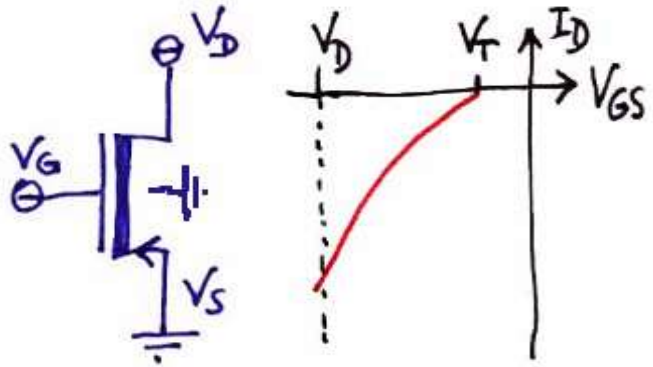
Functioning of the CMOS Inverter

Remember the N-MOS characteristic.



Functioning of the CMOS Inverter

Remember the P-MOS characteristic.



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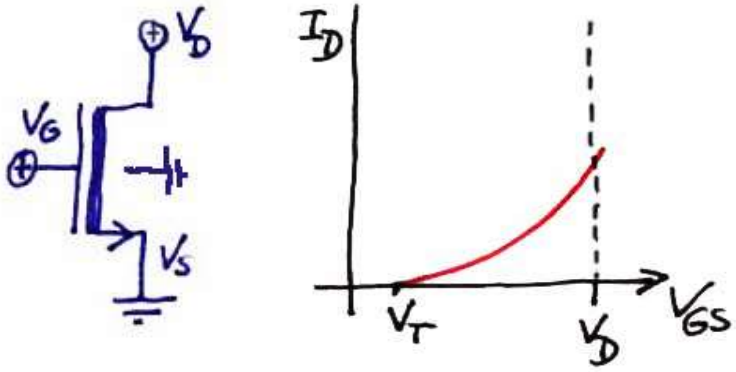

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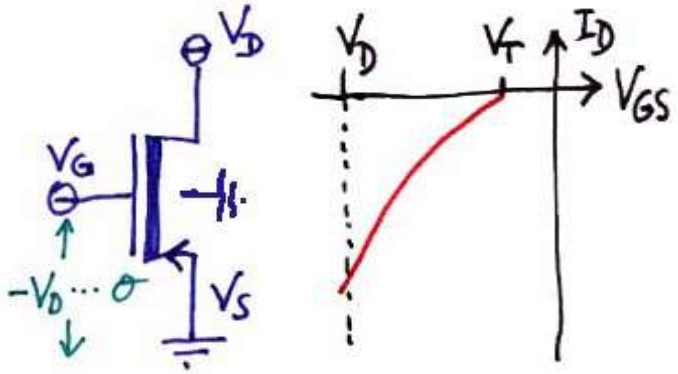

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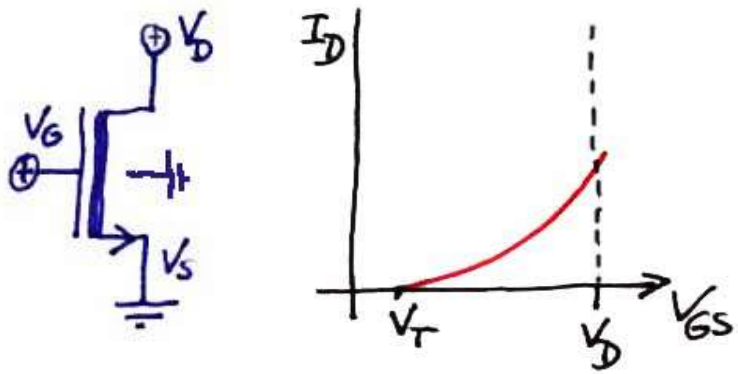

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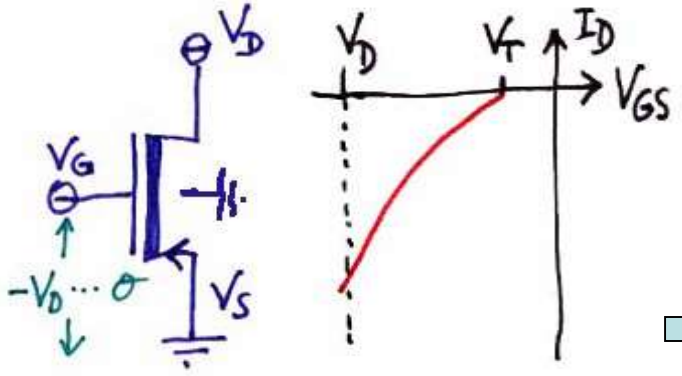
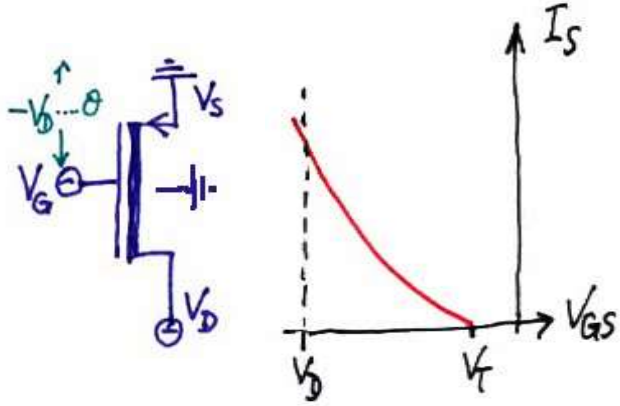
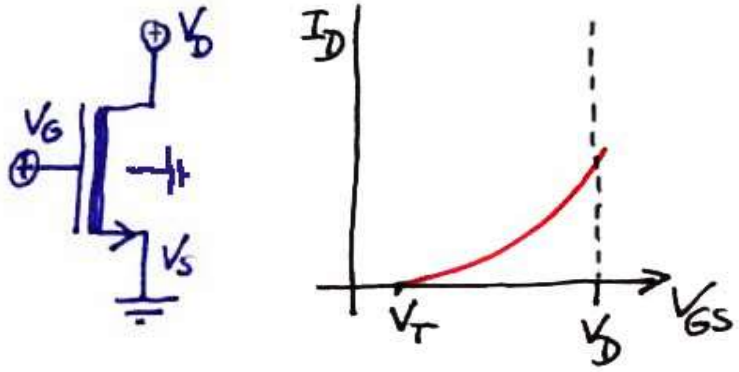


Let's turn the transistor around and plot I_S instead of I_D.

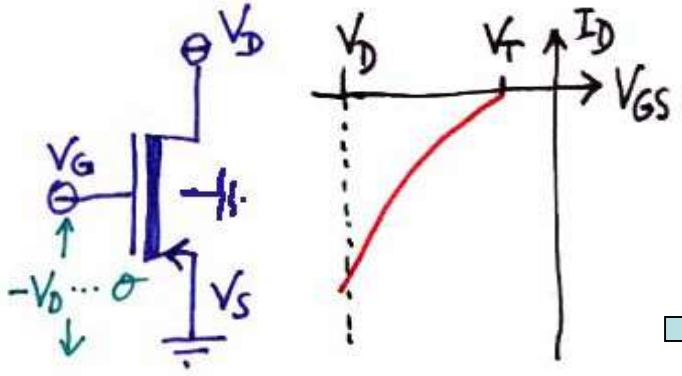


Remember the N-MOS characteristic.

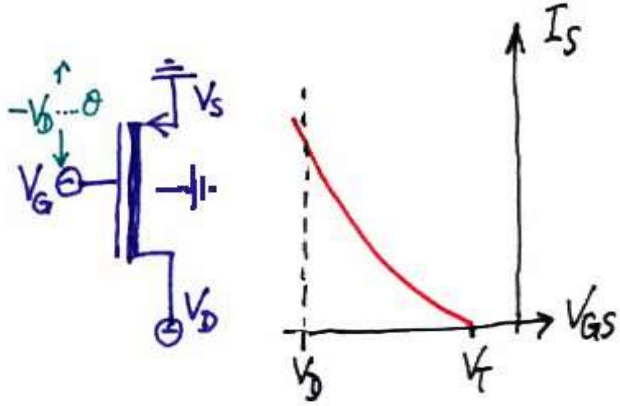


Functioning of the CMOS Inverter

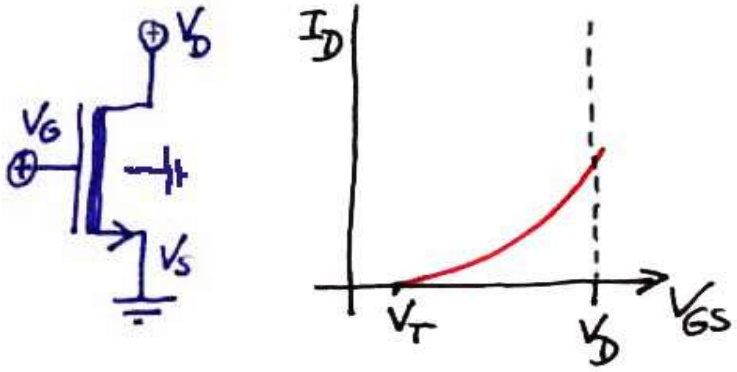
Remember the P-MOS characteristic.



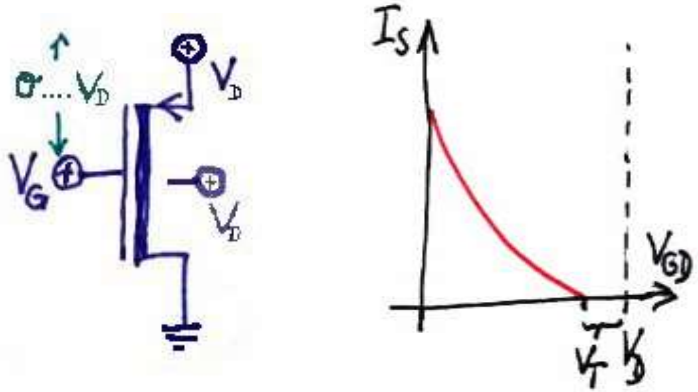
Let's turn the transistor around and plot I_S instead of I_D.



Remember the N-MOS characteristic.

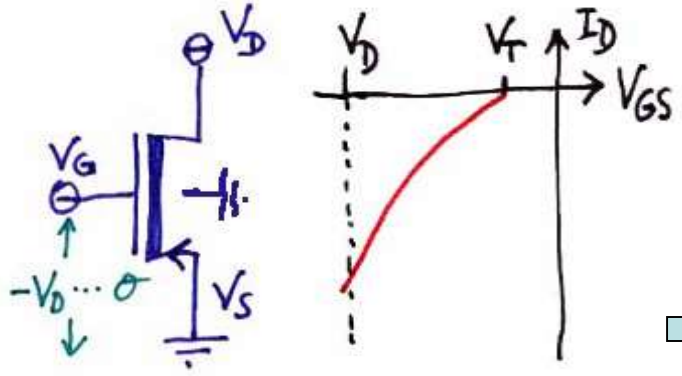


Now we shift each terminal by V_D!

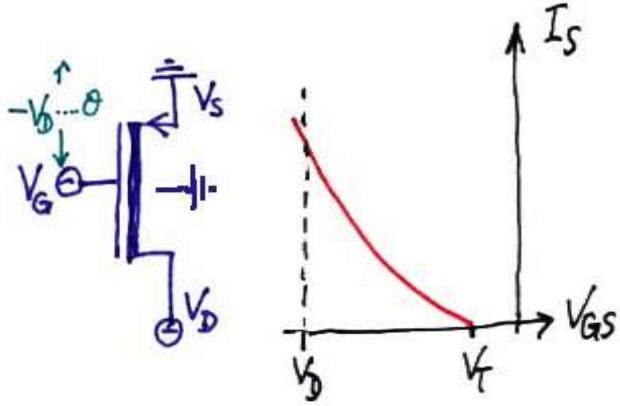


Functioning of the CMOS Inverter

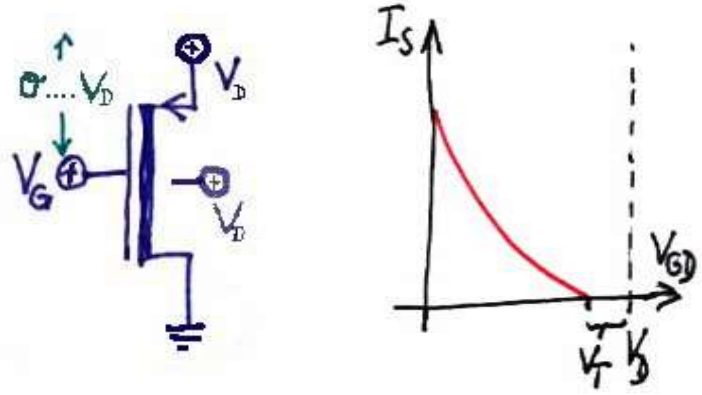
Remember the P-MOS characteristic.



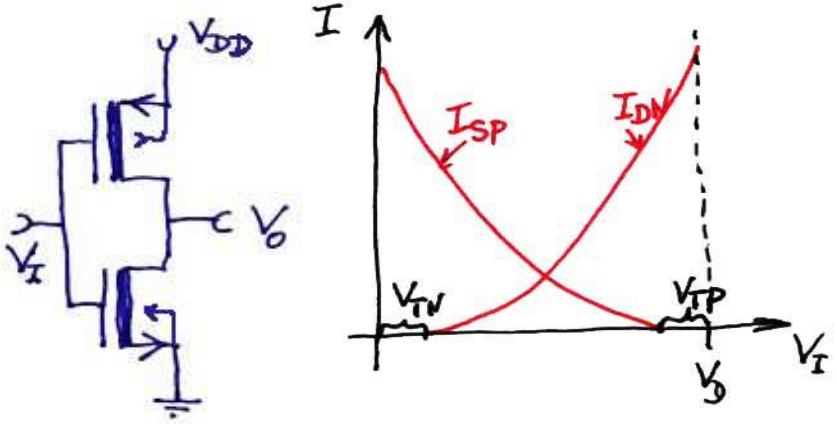
Let's turn the transistor around and plot I_S instead of I_D.



Now we shift each terminal by V_D!

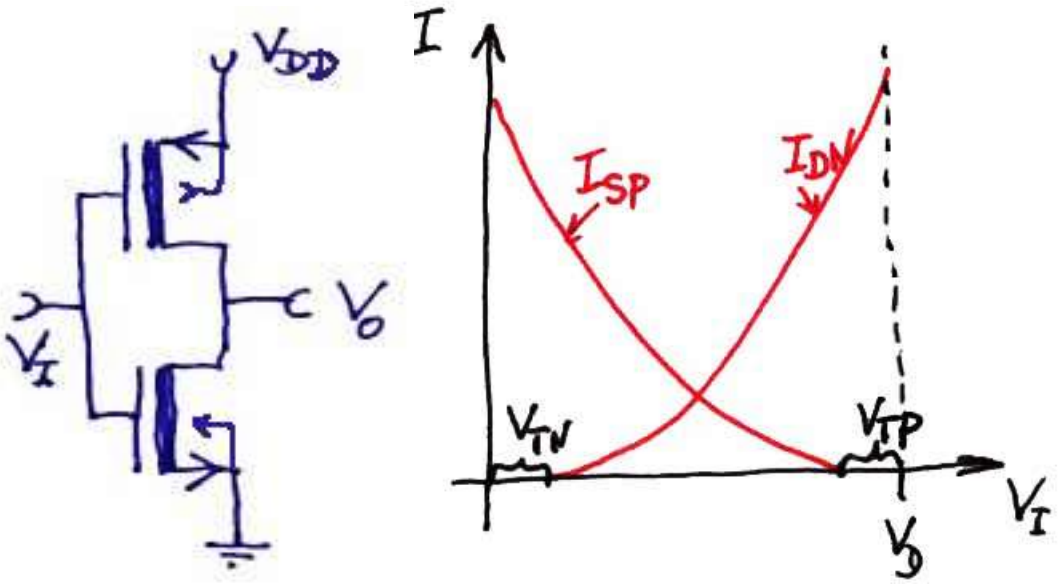


We assemble this to the CMOS inverter:



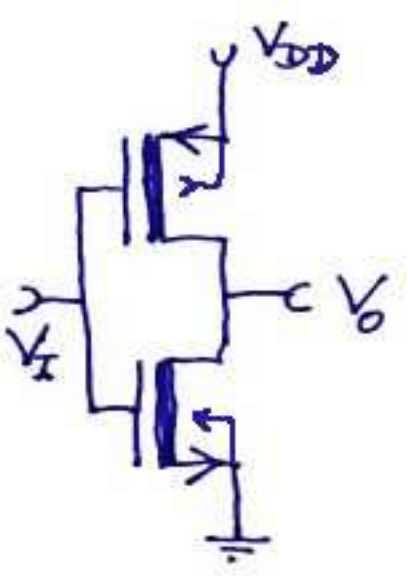
Process - integration

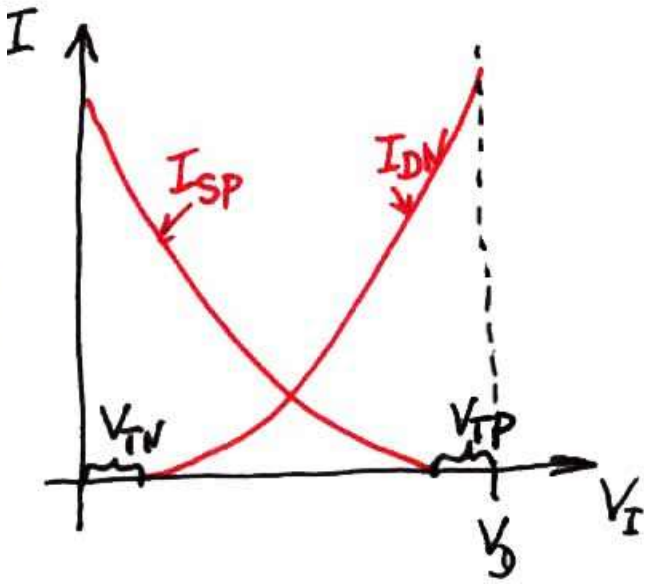
Perfect transfer curve

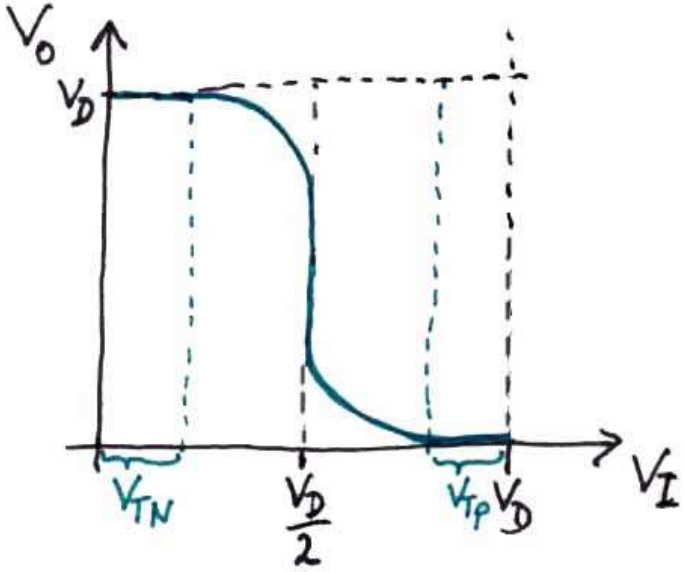


Process - integration

Perfect transfer curve



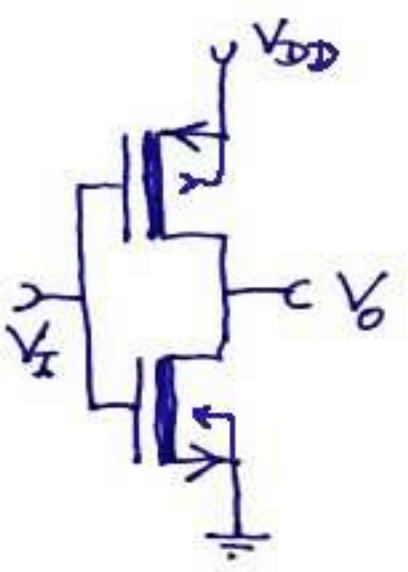


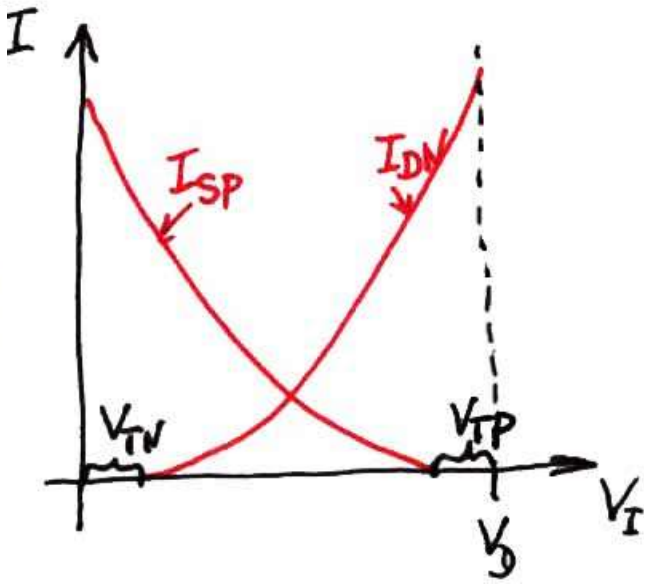


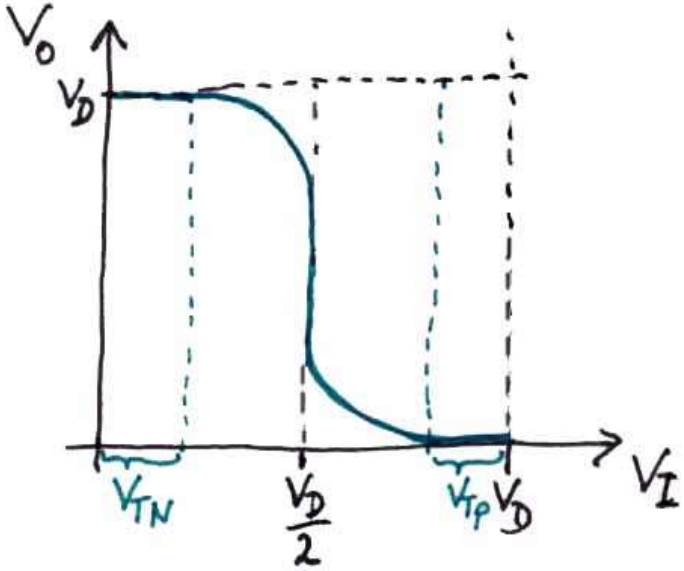
Transfer curve: ☺ Very steep
☺ $V_{o\,max} = V_D$, $V_{o\,min} = 0$
☺ Static power consumption = 0

Process - integration

Perfect transfer curve







Transfer curve: ☺ Very steep
☺ $V_{o\,max} = V_D$, $V_{o\,min} = 0$
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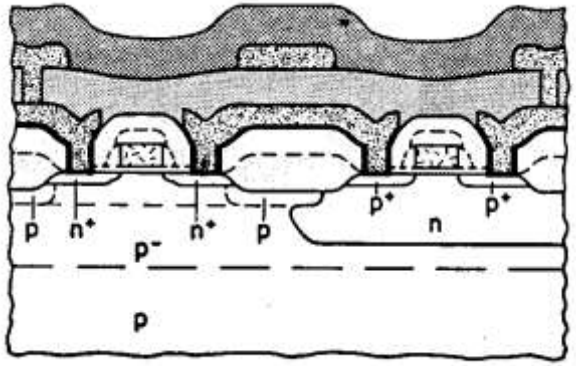
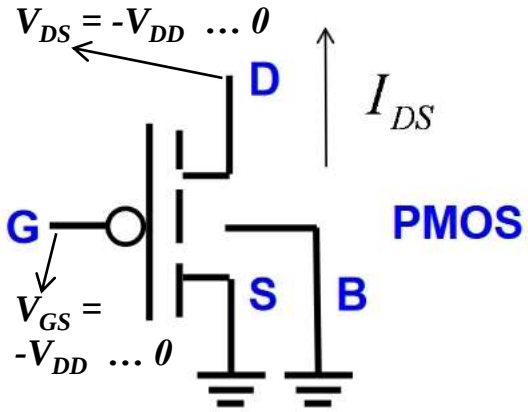
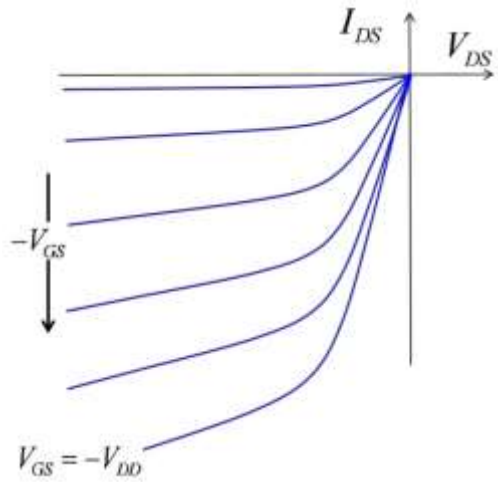
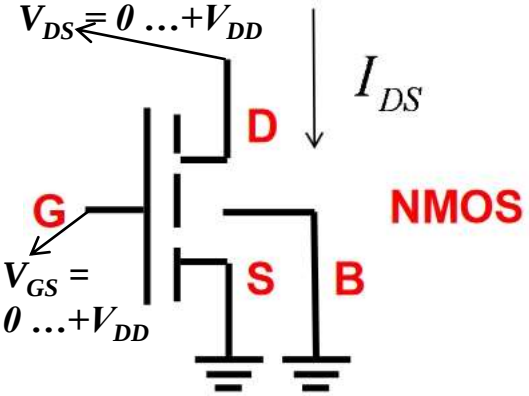


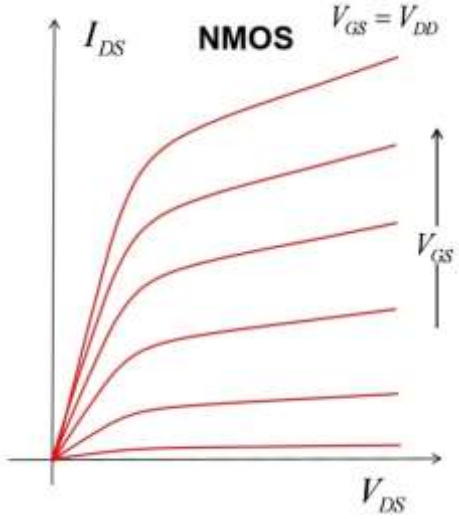
Higher process complexity necessary!

CMOS Concept discovered by $I_{DS}=f(V_{DS})$

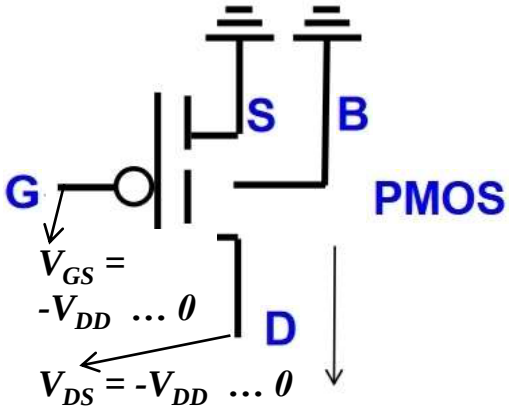


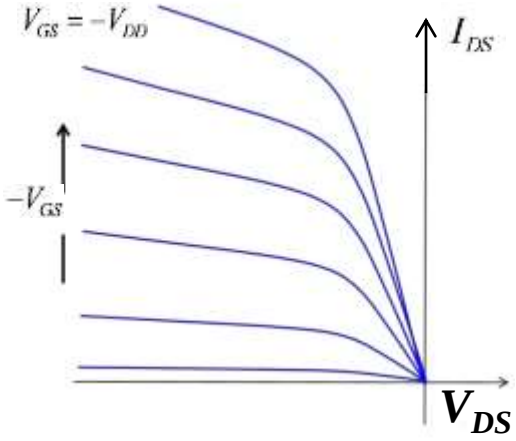


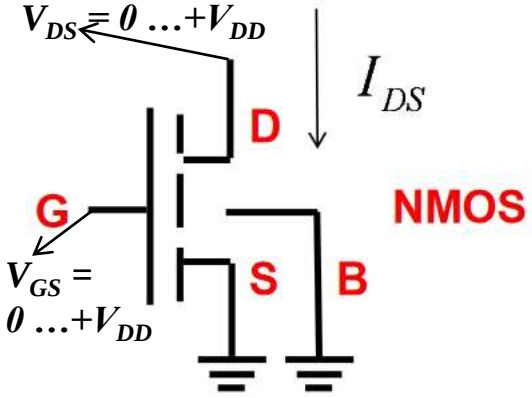


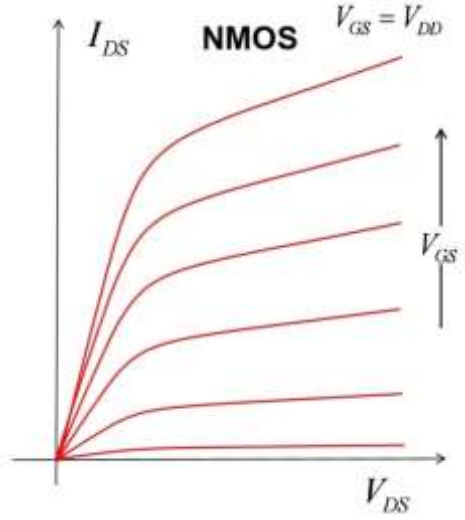


CMOS Concept discovered by $I_{DS}=f(V_{DS})$









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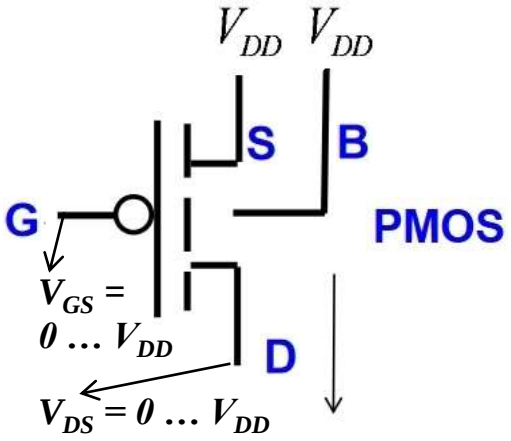

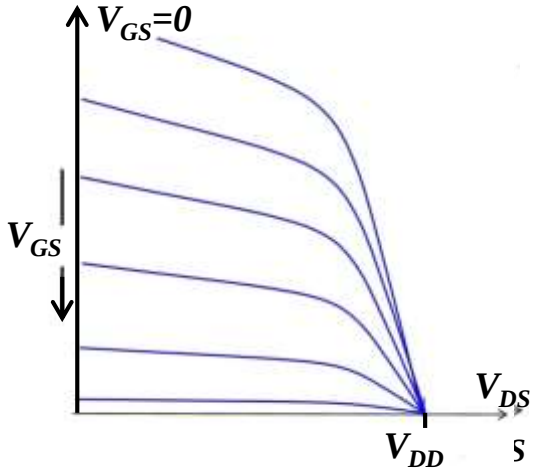

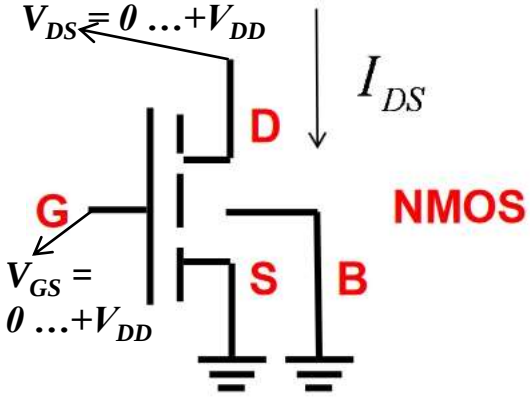

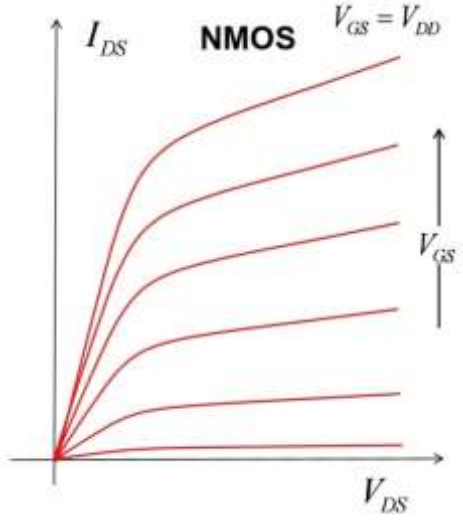

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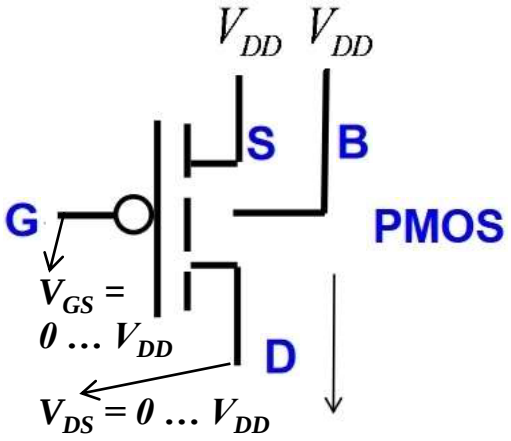
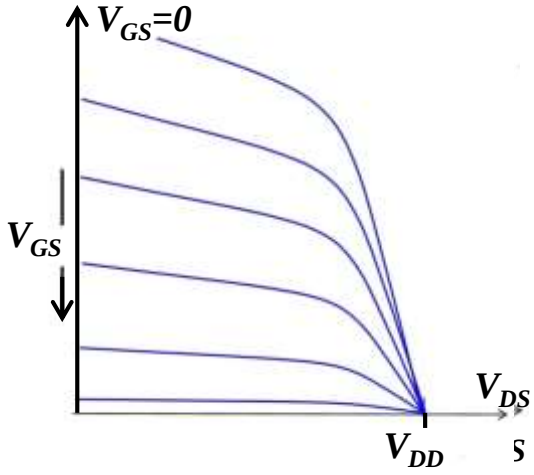
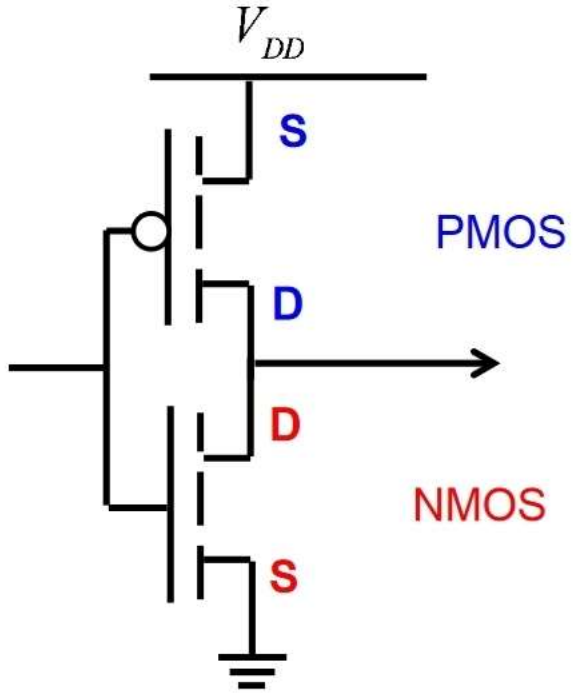
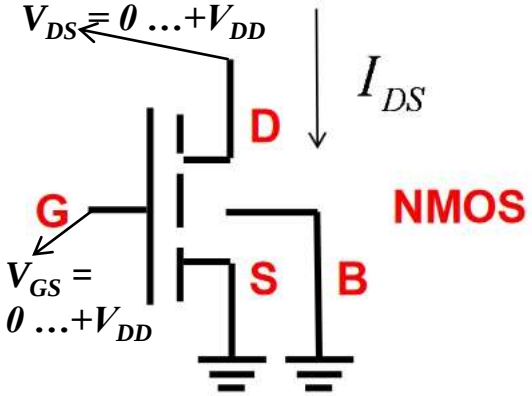
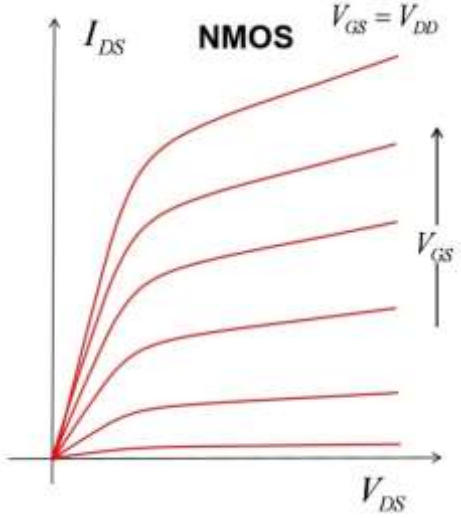






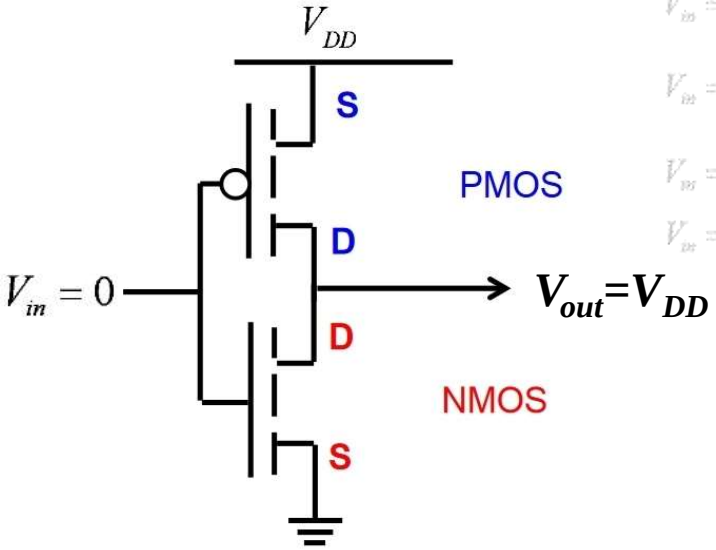




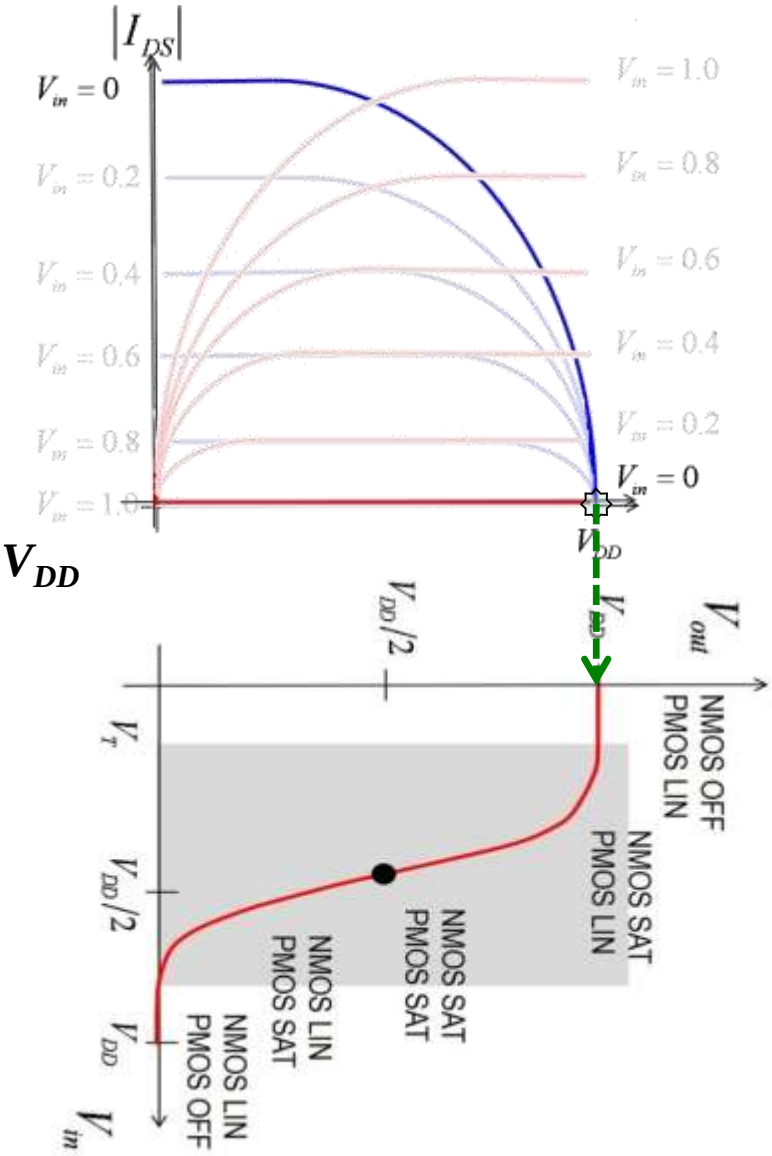
Concept of the CMOS Inverter

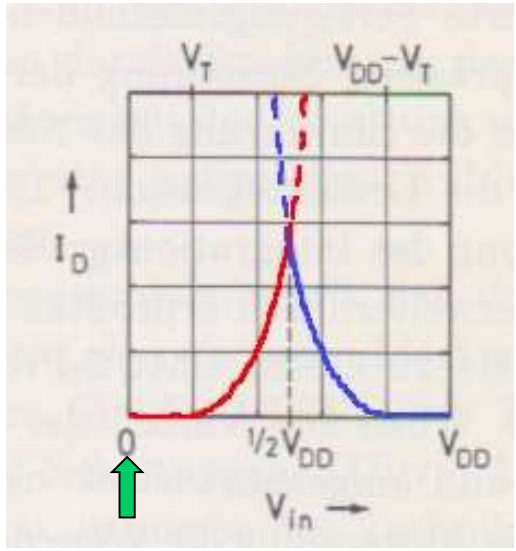
Input = low

$$V_{DD} = 1.0\ \text{V}$$



$$V_{TN} = -V_{TP} = 0.15\ \text{V}$$

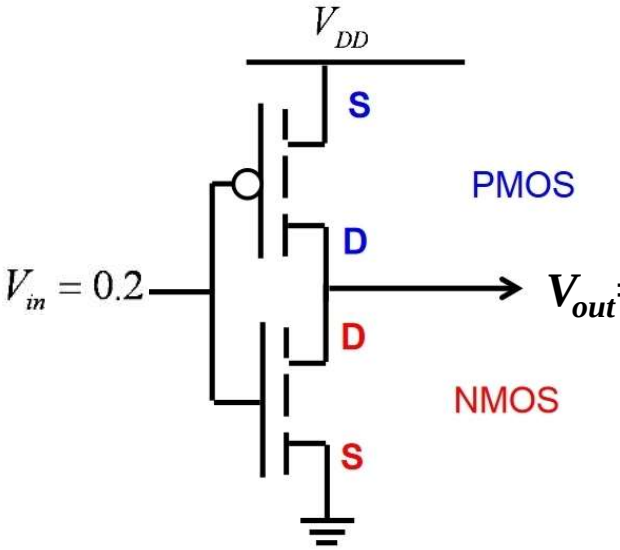




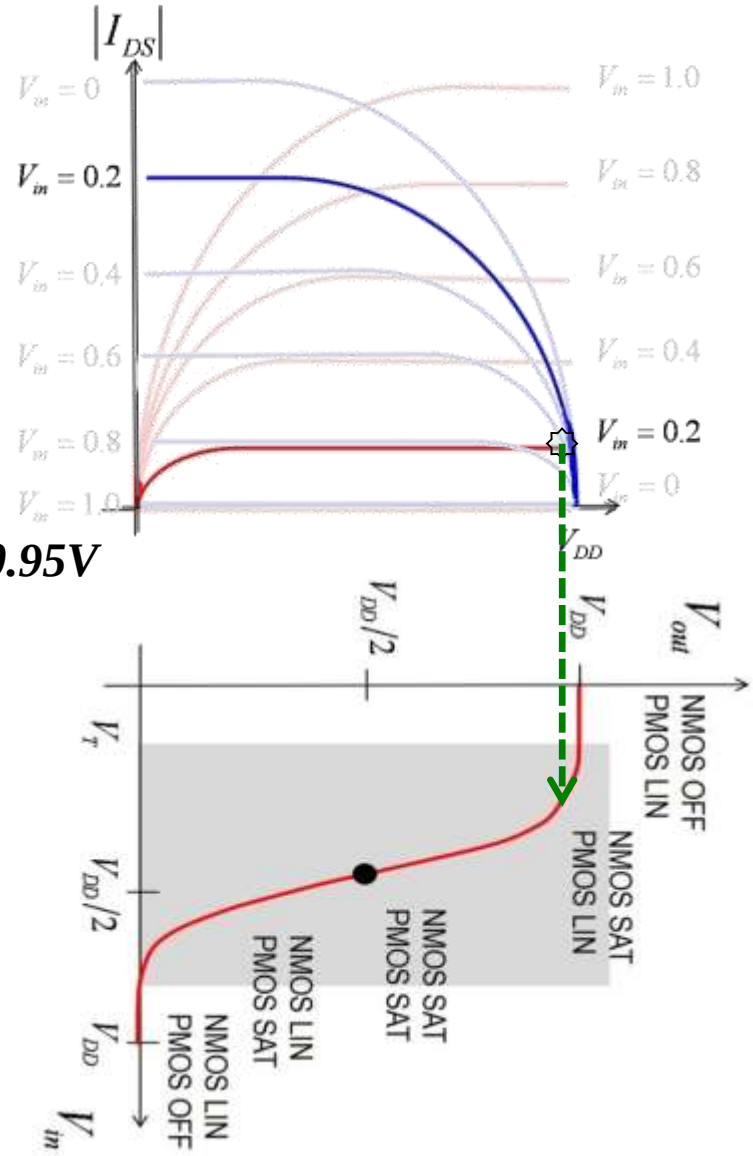
No Current!

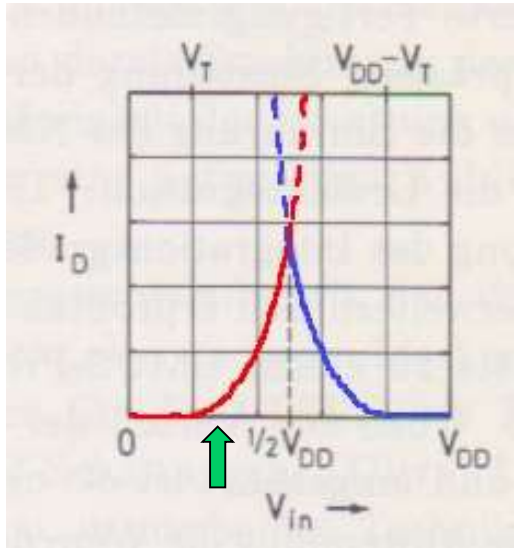
Concept of the CMOS Inverter

$V_{DD} = 1.0\ \text{V}$



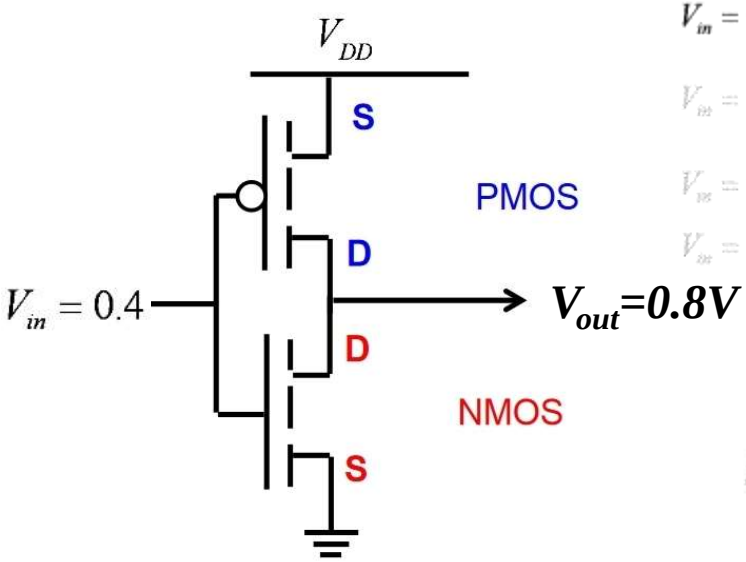
$V_{TN} = -V_{TP} = 0.15\ \text{V}$



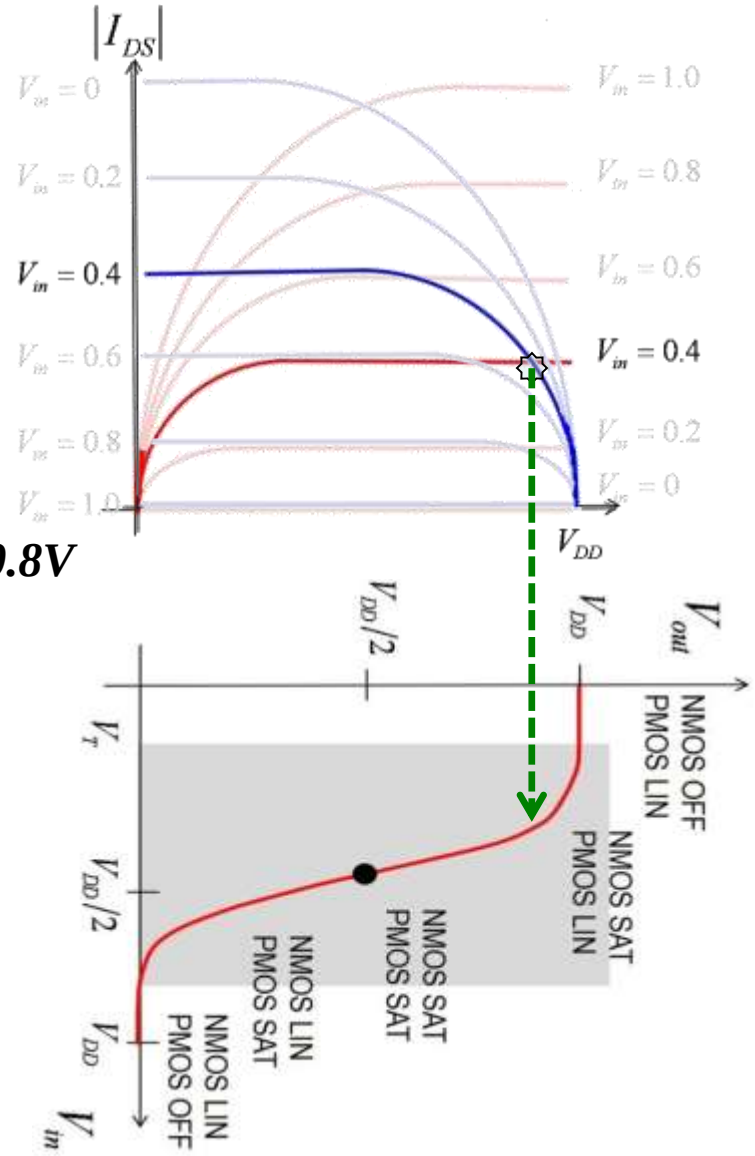


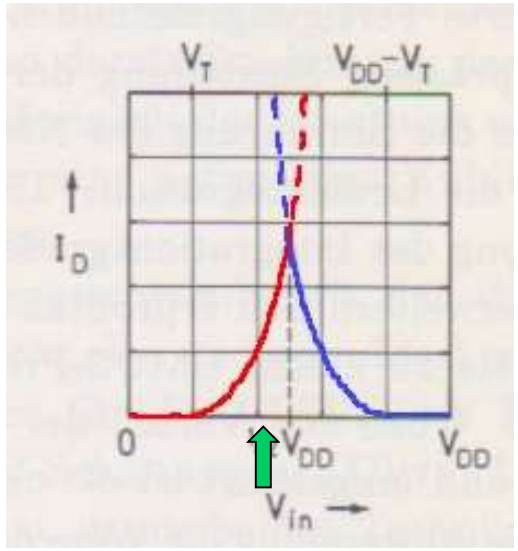
Concept of the CMOS Inverter

$V_{DD} = 1.0\ \text{V}$



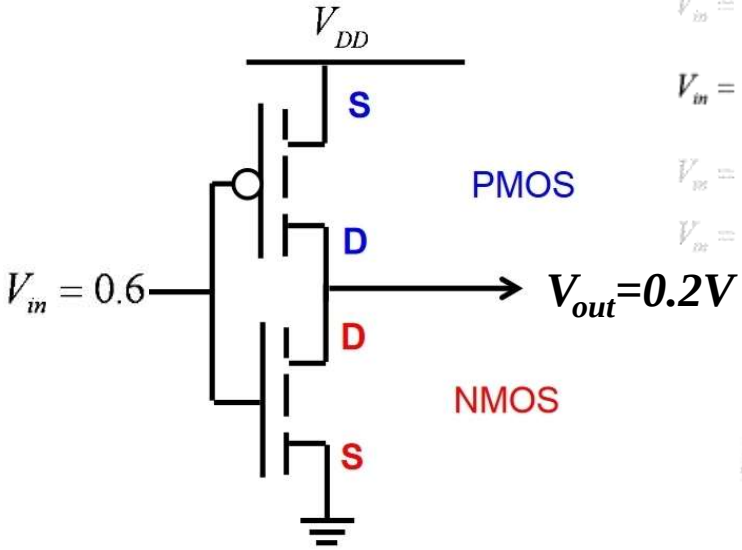
$V_{TN} = -V_{TP} = 0.15\ \text{V}$



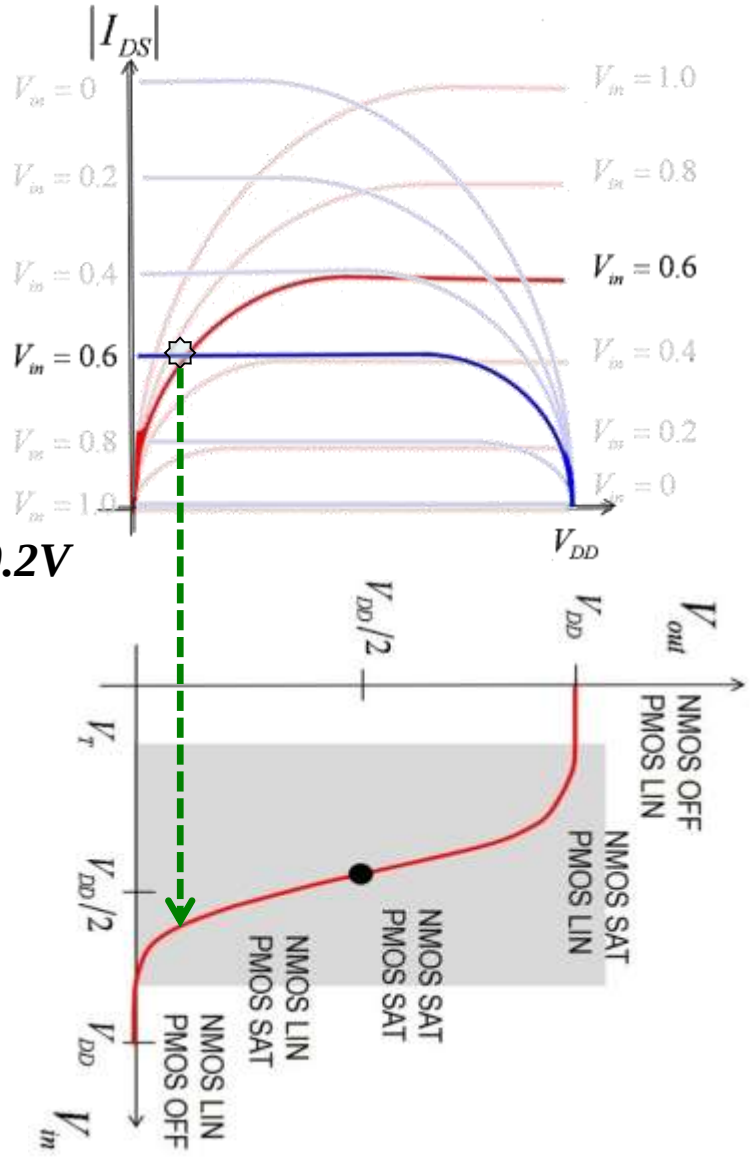


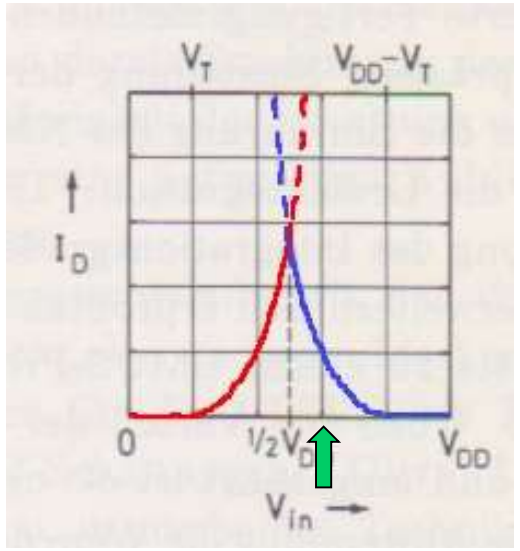
Concept of the CMOS Inverter

$$V_{DD} = 1.0\ \text{V}$$



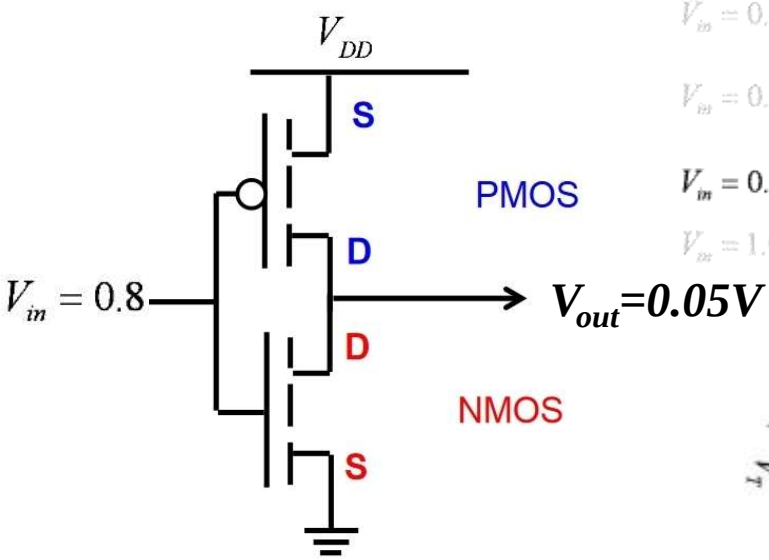
$$V_{TN} = -V_{TP} = 0.15\ \text{V}$$



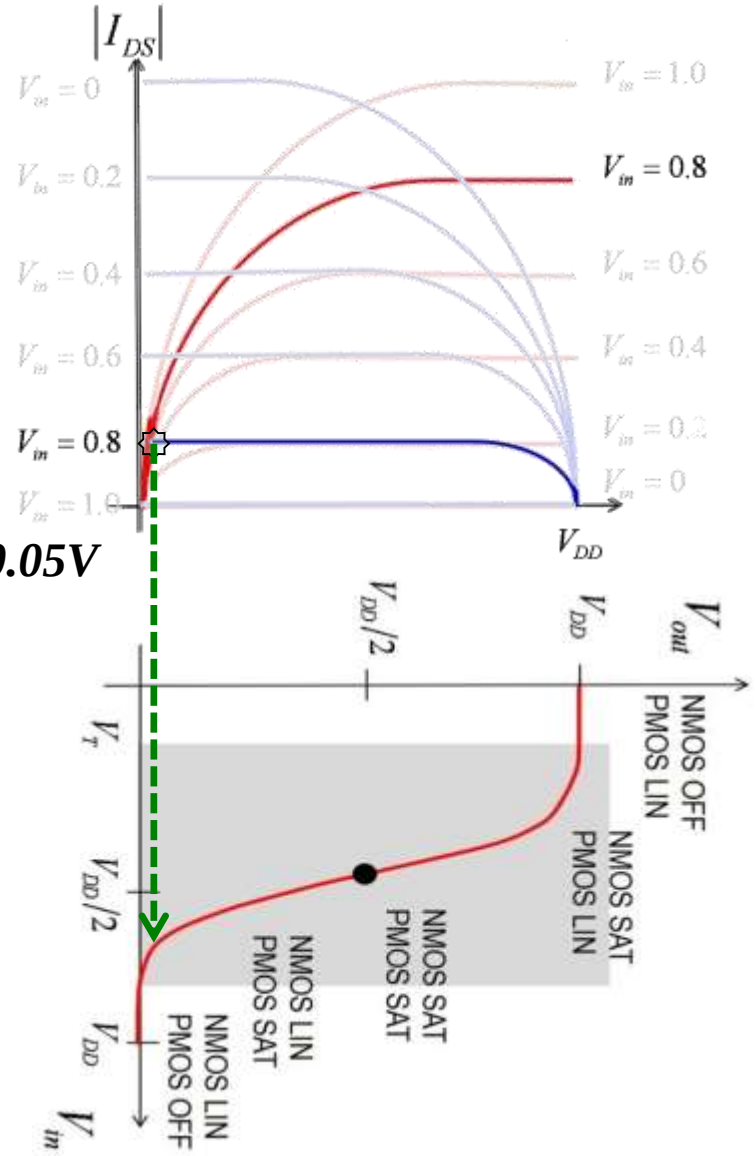


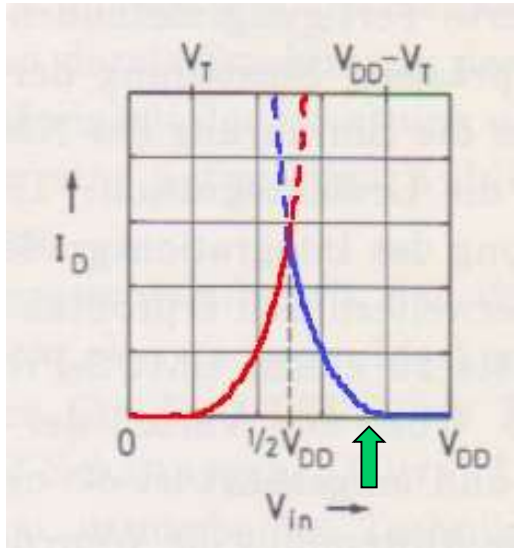
Concept of the CMOS Inverter

$V_{DD} = 1.0\ \text{V}$



$V_{TN} = -V_{TP} = 0.15\ \text{V}$

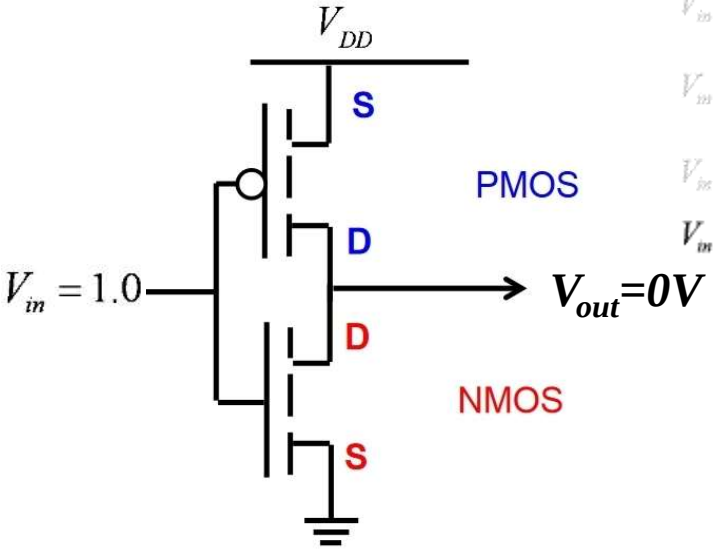




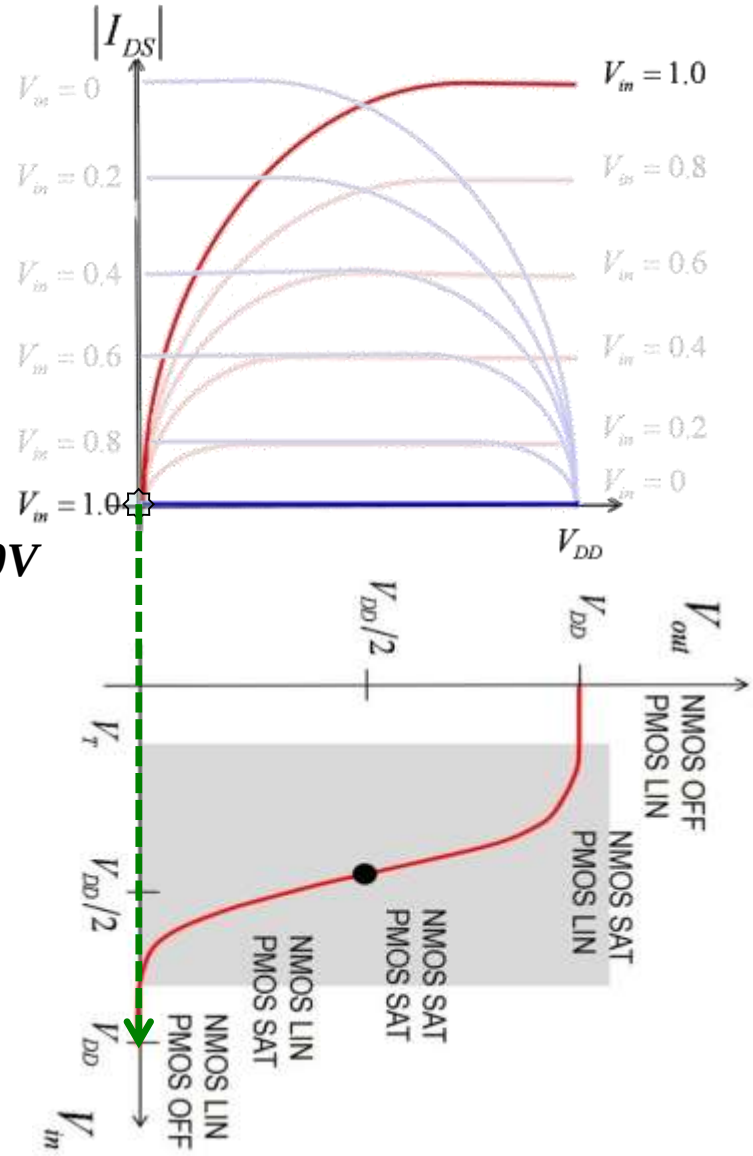
Concept of the CMOS Inverter

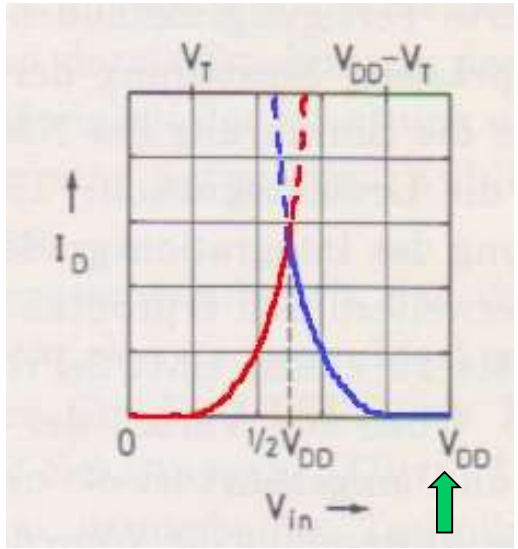
Input = high

$$V_{DD} = 1.0\ \text{V}$$



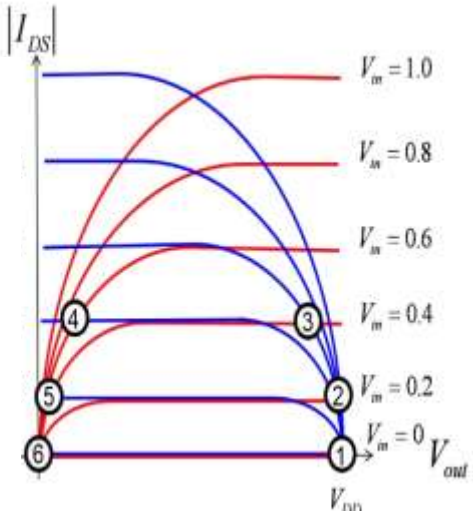
$$V_{TN} = -V_{TP} = 0.15\ \text{V}$$



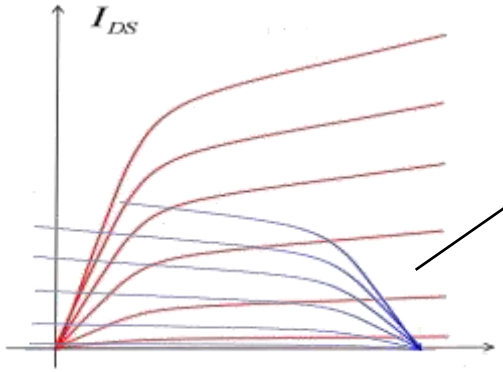


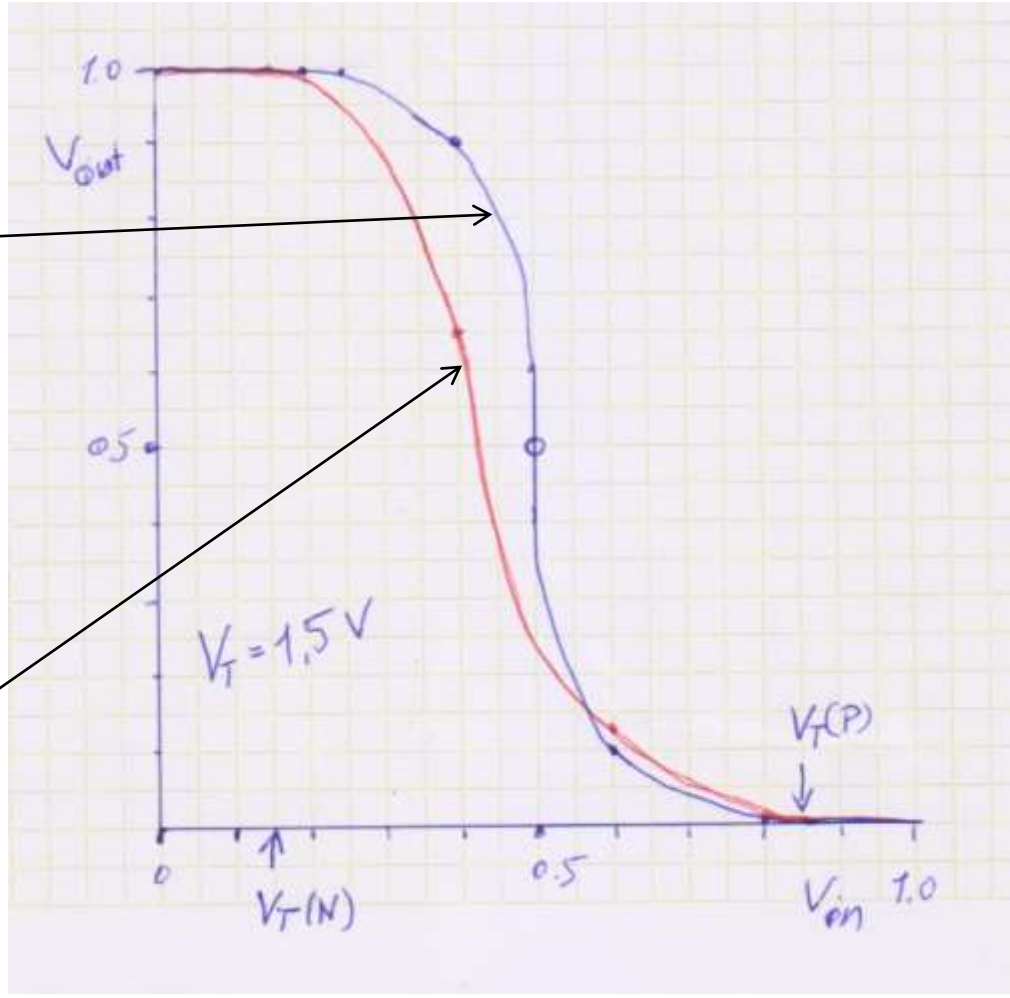
No Current!

Ideal: long channel & $I_{Dsat}(N)=I_{Dsat}(P)$



Real: short channel & $I_{Dsat}(N)>I_{Dsat}(P)$

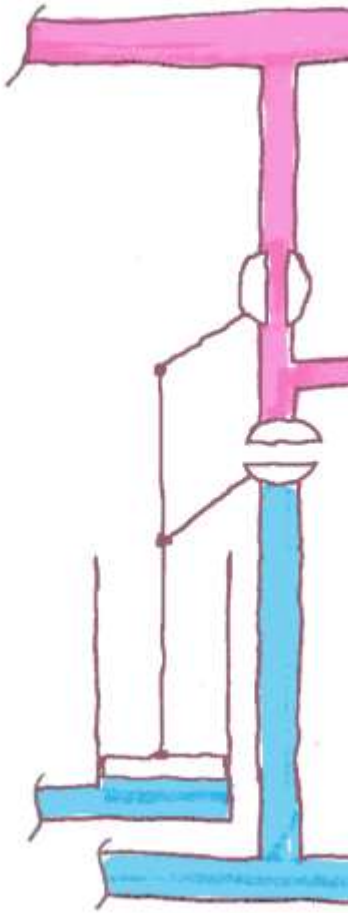


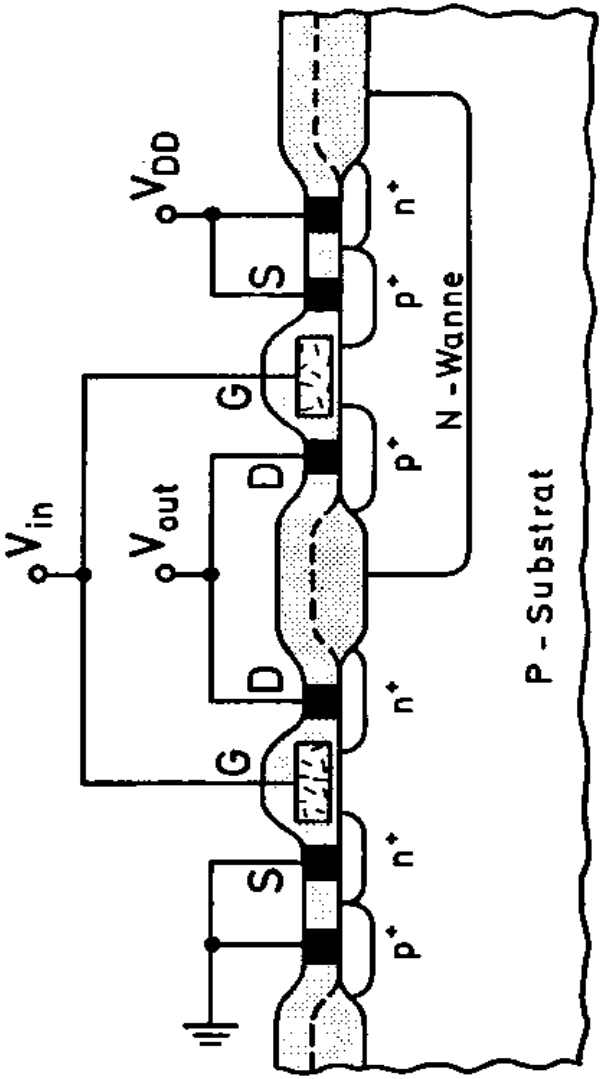


To get closer to ideal, design of FET width W(P) > W(N) !

CMOS Complementary MOS (Utilizing NMOS & PMOS)

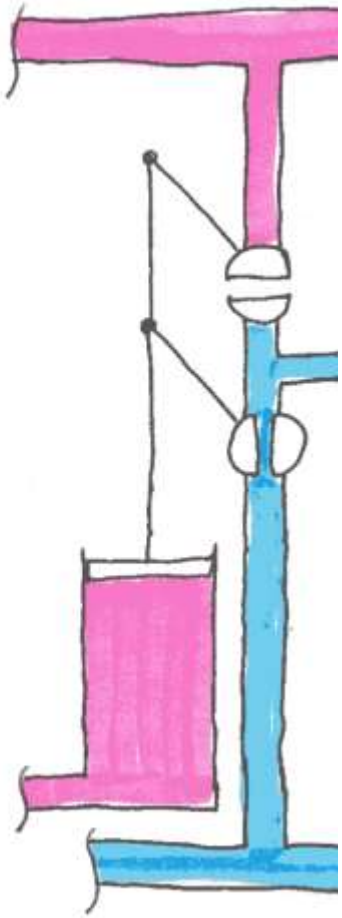
Inverter

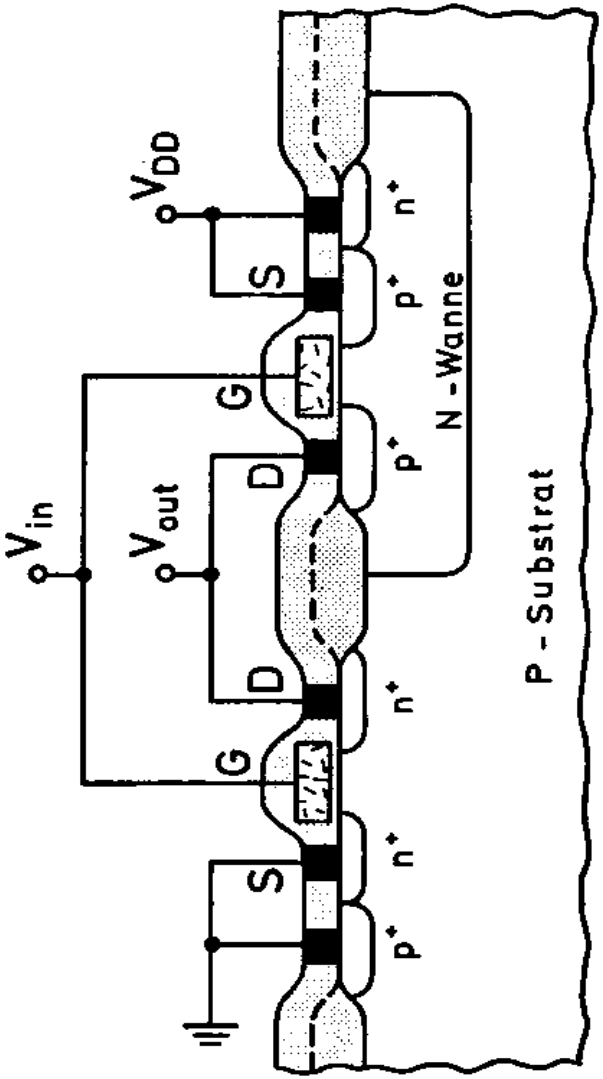




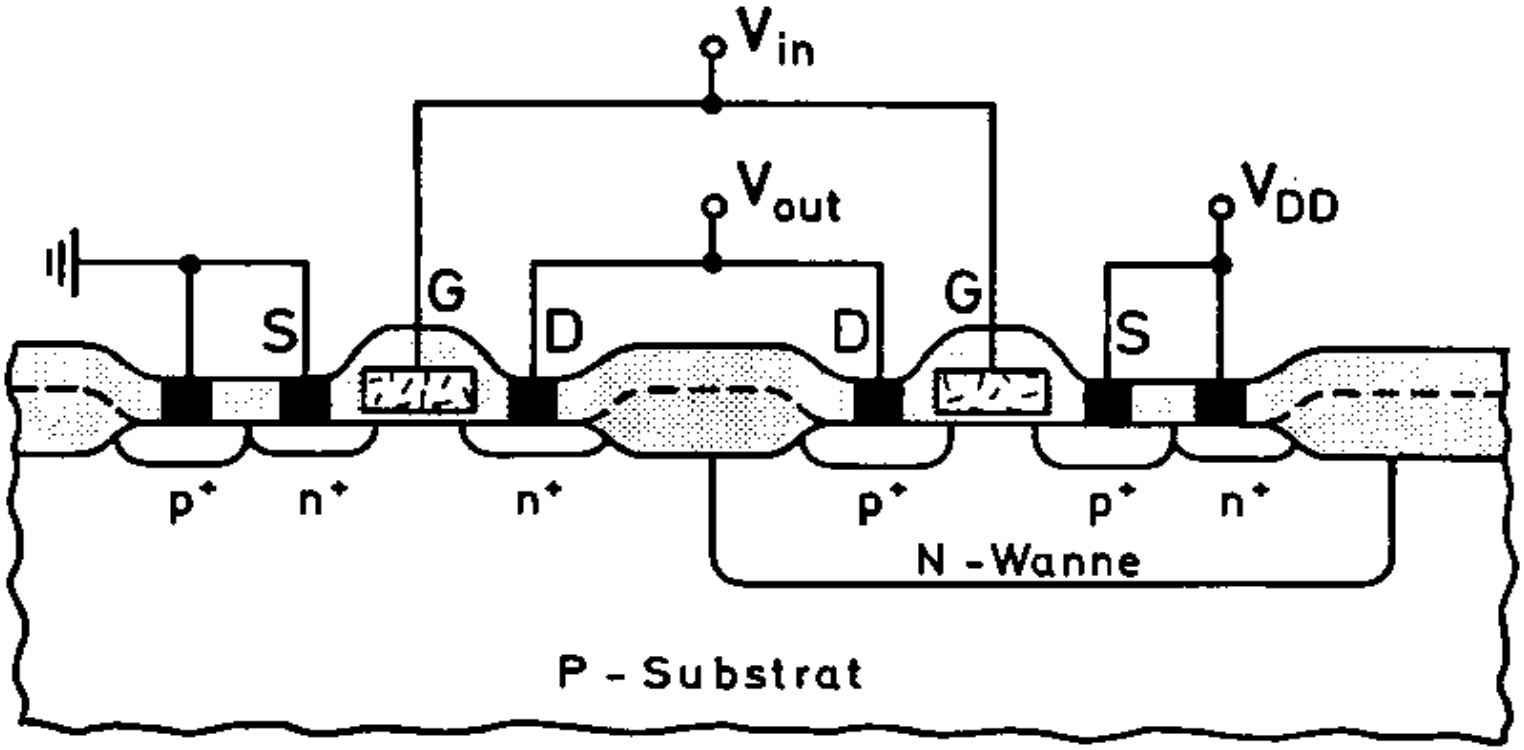
CMOS Complementary MOS (Utilizing NMOS & PMOS)

Inverter



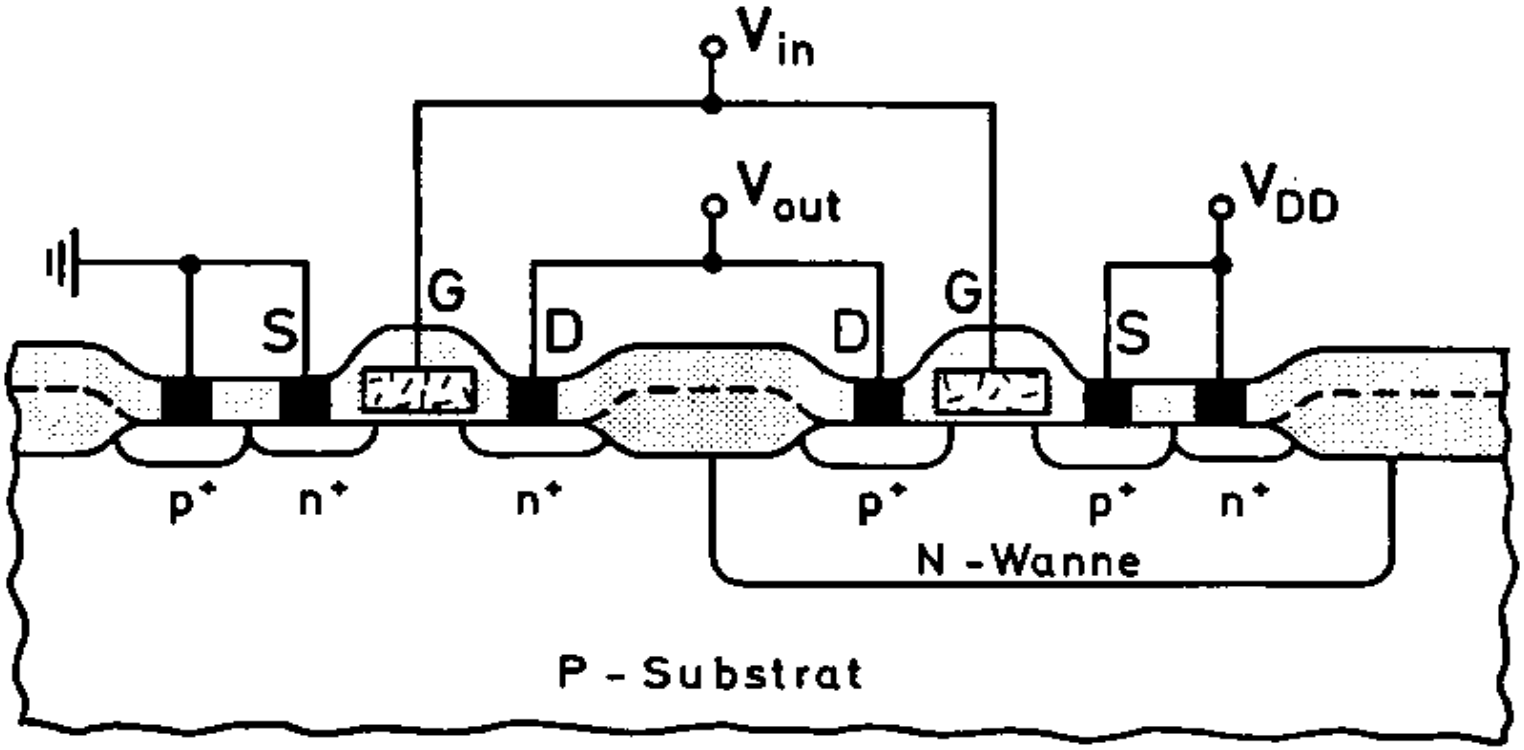


CMOS Inverter



Aus: Schumiki, Seegebrecht „Prozeßtechnologie“ Springer 1991

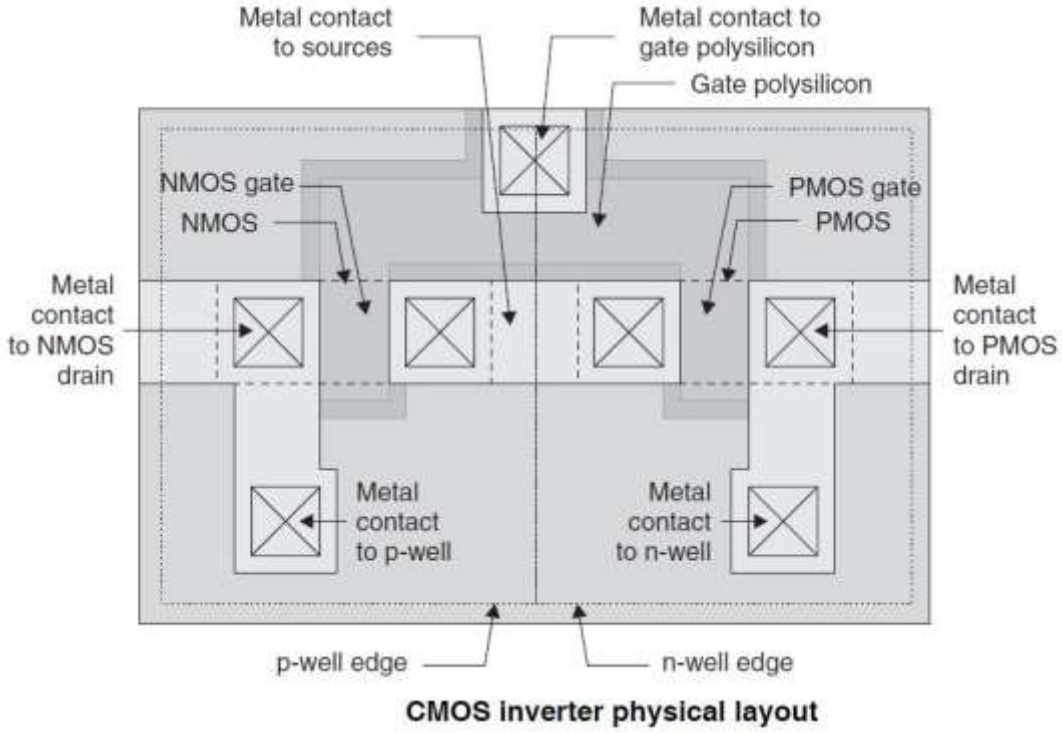
CMOS Inverter



Aus: Schumiki, Seegebrecht „Prozeßtechnologie“ Springer 1991

Continue
"HLT_SS20_12.04" 36:28

4.3. CMOS Prozessablauf



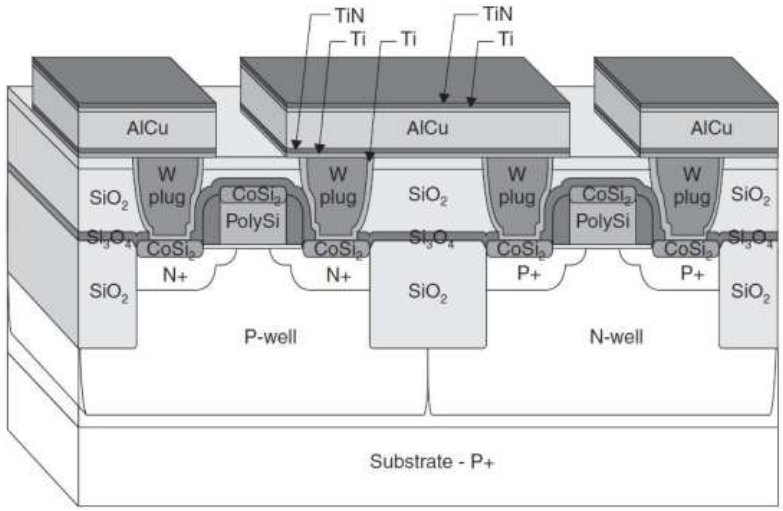
CMOS inverter physical layout

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

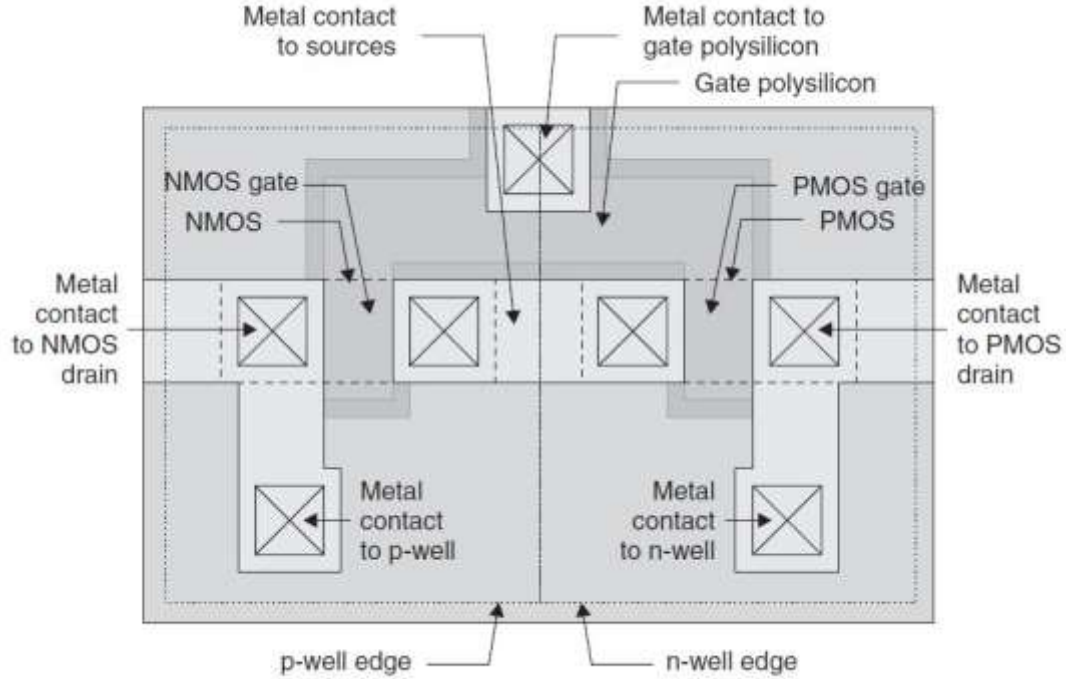
4.3. CMOS Prozessablauf

CMOS Inverter:

Epi Wafer-
Dual well-
STI-
SiGate-
LDD (S/D extensions)-
SALICIDE-
SAC-
Dielecric CMP



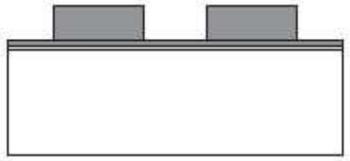
CMOS wafer after metal 1



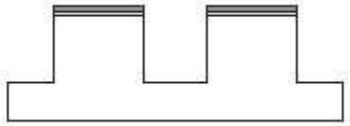
CMOS inverter physical layout

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

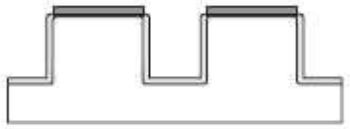
CMOS Inverter-STI



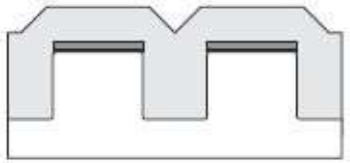
- Grow thin stress relief SiO_2 layer.
- Deposit Si_3N_4 polish stop layer.
- Apply photoresist and pattern with shallow trench isolation mask.



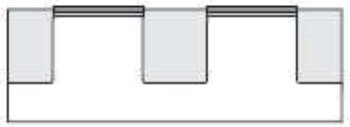
- Etch Si_3N_4 polish stop layer.
- Etch thin stress relief SiO_2 layer.
- Etch shallow trenches into silicon.
- Strip the photoresist.



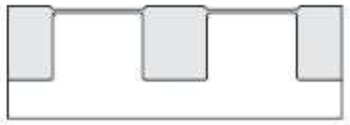
- Grow thin SiO_2 layer to round off the trench corners.



- Deposit thick SiO_2 layer to fill the trenches.



- Chemical mechanical planarise the SiO_2 trench fill layer down to the top of the Si_3N_4 polish stop layer.

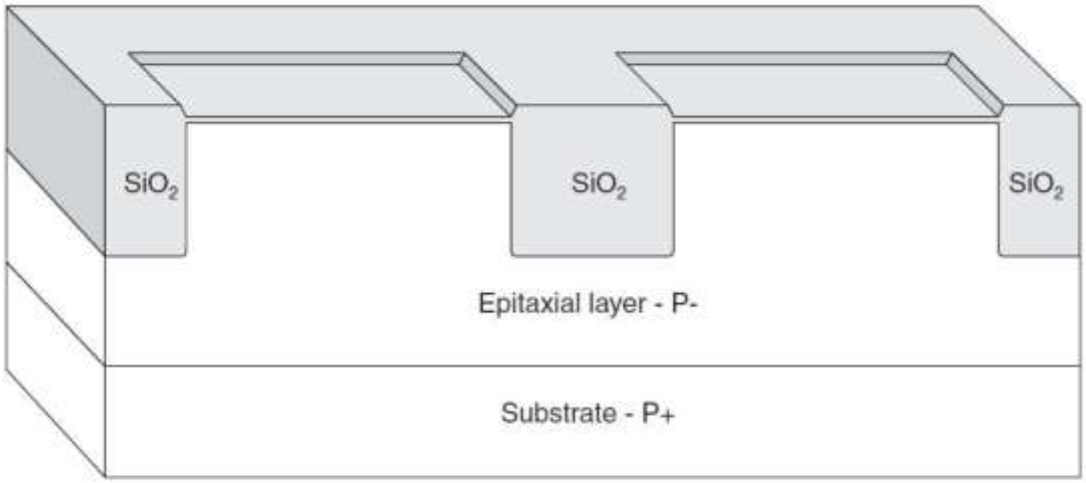


- Strip off the Si_3N_4 polish stop layer and etch back the trench fill SiO_2 layer.

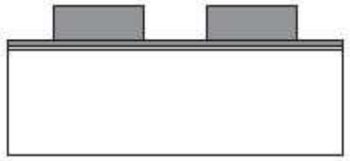
Shallow trench isolation formation

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

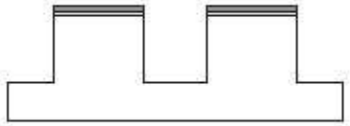
CMOS Inverter-STI



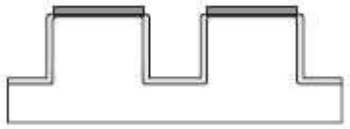
CMOS wafer after shallow trench isolation



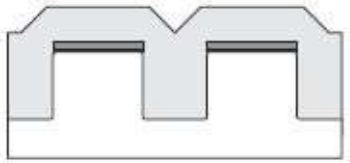
- Grow thin stress relief SiO_2 layer.
- Deposit Si_3N_4 polish stop layer.
- Apply photoresist and pattern with shallow trench isolation mask.



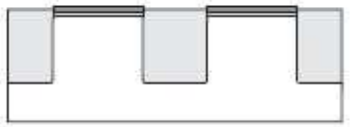
- Etch Si_3N_4 polish stop layer.
- Etch thin stress relief SiO_2 layer.
- Etch shallow trenches into silicon.
- Strip the photoresist.



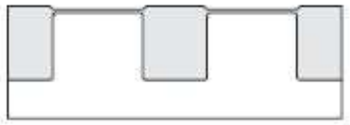
- Grow thin SiO_2 layer to round off the trench corners.



- Deposit thick SiO_2 layer to fill the trenches.



- Chemical mechanical planarise the SiO_2 trench fill layer down to the top of the Si_3N_4 polish stop layer.

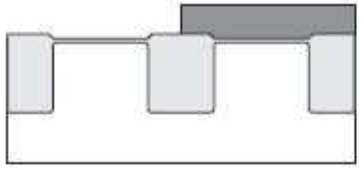


- Strip off the Si_3N_4 polish stop layer and etch back the trench fill SiO_2 layer.

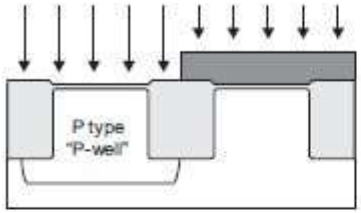
Shallow trench isolation formation

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

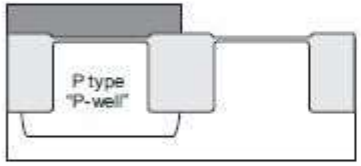
CMOS Inverter-wells



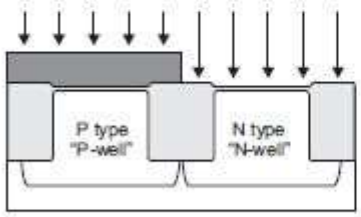
- Apply photoresist and pattern with P-well mask.



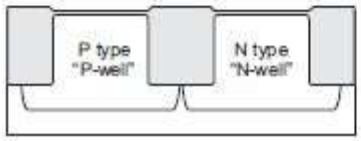
- Ion implant P type dopants to create the P-well. Note that the P-well may be created by using multiple sequential implants with different characteristics to create different dopant levels at different depths into the silicon optimizing threshold and punch through voltages.



- Strip the P-well photoresist.
- Apply photoresist and pattern with N-well mask.



- Ion implant N type dopants to create the N-well. Note that the N-well may be created by using multiple sequential implants with different characteristics to create different dopant levels at different depths into the silicon optimizing threshold and punch through voltages.

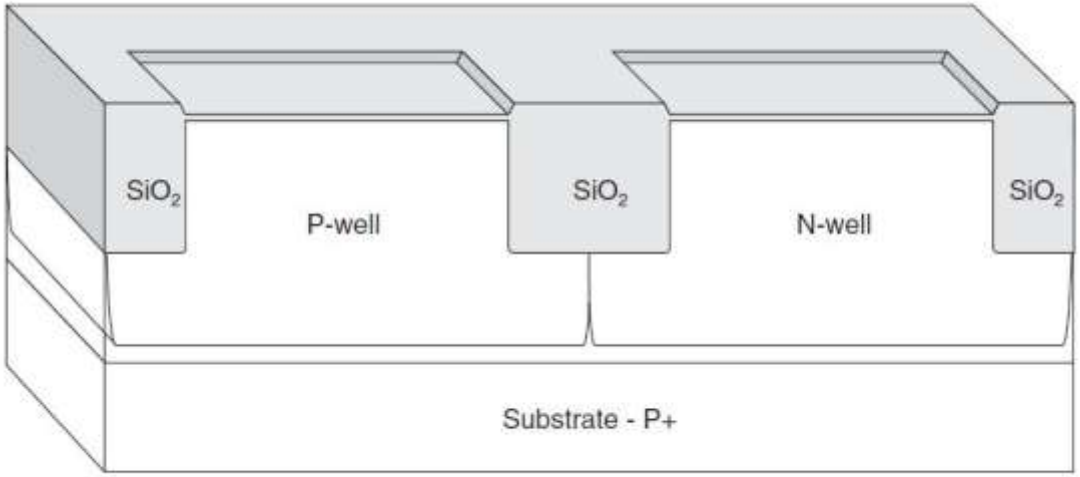


- Strip the N-well photoresist.
- Rapid thermal anneal the wells.

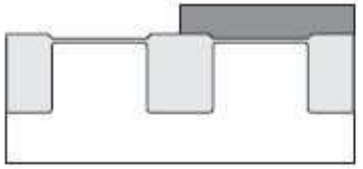
Well formation

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

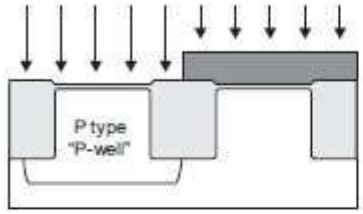
CMOS Inverter-wells



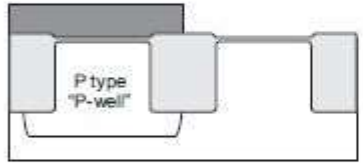
CMOS wafer after well formation



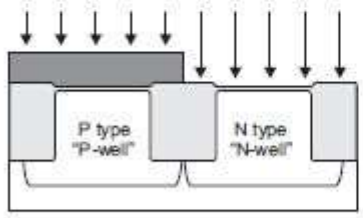
- Apply photoresist and pattern with P-well mask.



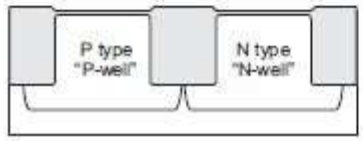
- Ion implant P type dopants to create the P-well. Note that the P-well may be created by using multiple sequential implants with different characteristics to create different dopant levels at different depths into the silicon optimizing threshold and punch through voltages.



- Strip the P-well photoresist.
- Apply photoresist and pattern with N-well mask.



- Ion implant N type dopants to create the N-well. Note that the N-well may be created by using multiple sequential implants with different characteristics to create different dopant levels at different depths into the silicon optimizing threshold and punch through voltages.

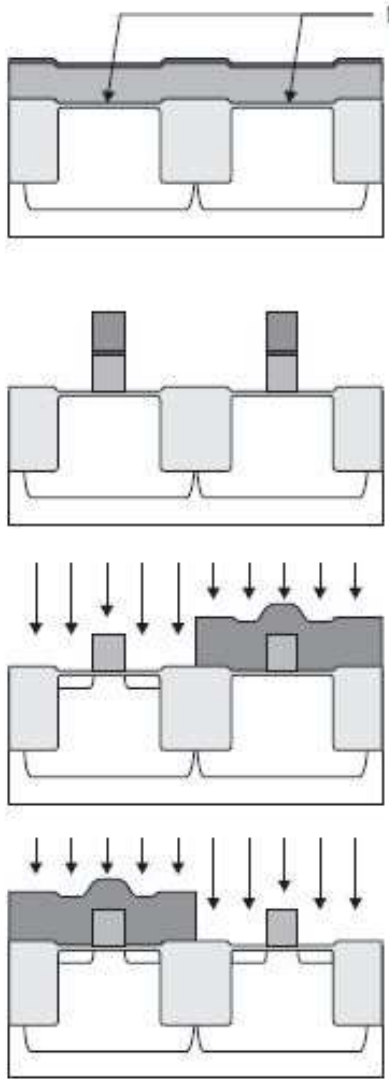


- Strip the N-well photoresist.
- Rapid thermal anneal the wells.

Well formation

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

CMOS Inverter-Si Gate & S/D extensions



- Strip off thin SiO_2.
- Grow sacrificial gate SiO_2 layer and strip back off.
- Grow gate SiO_2 layer.
- Anneal gate SiO_2 in NO to create nitrogen layer.
- Deposit polysilicon.
- Deposit thin Si_3N_4 layer anti reflective layer.

- Apply photoresist and pattern with the gate mask.
- Etch the thin Si_3N_4 anti reflective layer
- Etch the polysilicon and stop on the underlying gate SiO_2.

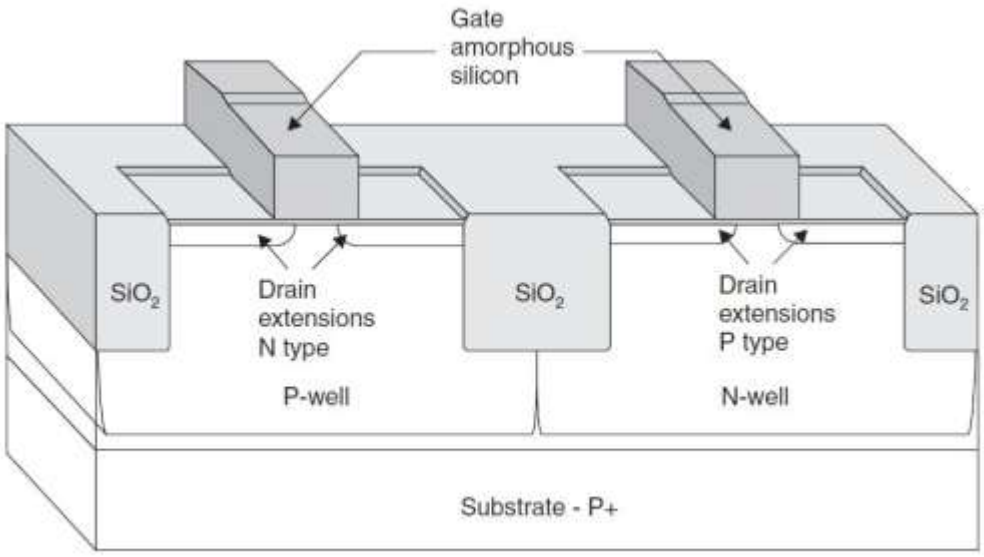
- Strip the gate photoresist.
- Strip the thin anti reflective Si_3N_4 layer.
- Oxidize the polysilicon.
- Apply photoresist and pattern with the N-extension mask.
- Ion implant the N-extension regions with N

- Strip the gate photoresist.
- Apply photoresist and pattern with the P-extension mask.
- Ion implant the P-extension regions with P type dopant.

CMOS gate and drain extension formation

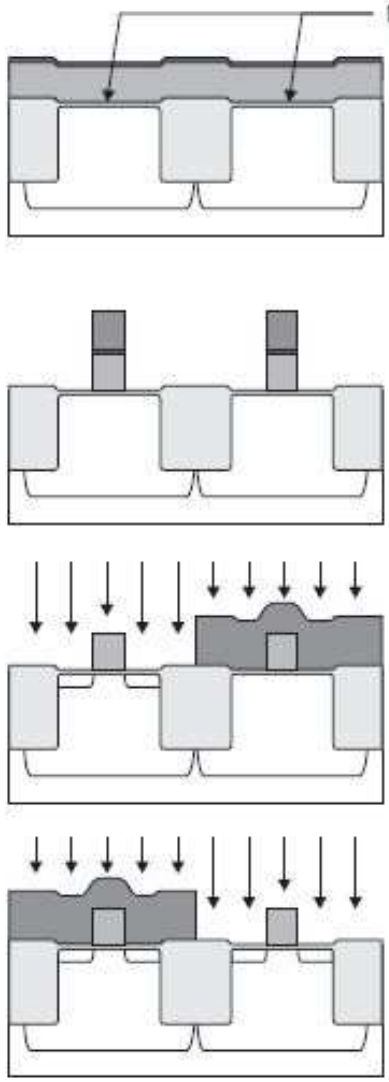
Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

CMOS Inverter-Si Gate & S/D extensions



CMOS wafer after gate and drain extension formation

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf



- Strip off thin SiO_2.
- Grow sacrificial gate SiO_2 layer and strip back off.
- Grow gate SiO_2 layer.
- Anneal gate SiO_2 in NO to create nitrogen layer.
- Deposit polysilicon.
- Deposit thin Si_3N_4 layer anti reflective layer.

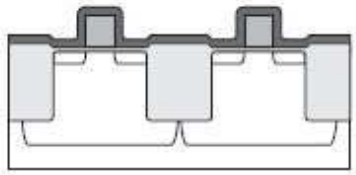
- Apply photoresist and pattern with the gate mask.
- Etch the thin Si_3N_4 anti reflective layer
- Etch the polysilicon and stop on the underlying gate SiO_2.

- Strip the gate photoresist.
- Strip the thin anti reflective Si_3N_4 layer.
- Oxidize the polysilicon.
- Apply photoresist and pattern with the N-extension mask.
- Ion implant the N-extension regions with N

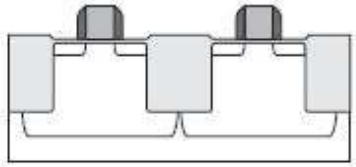
- Strip the gate photoresist.
- Apply photoresist and pattern with the P-extension mask.
- Ion implant the P-extension regions with P type dopant.

CMOS gate and drain extension formation

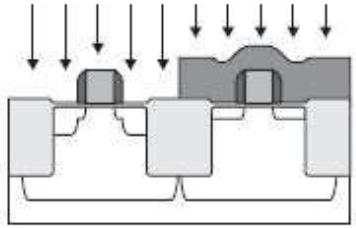
CMOS Inverter-S/D formation



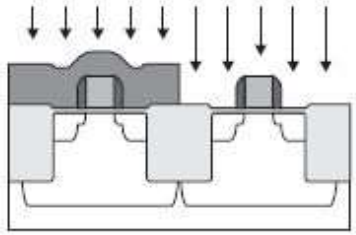
- Strip the P-extension photoresist.
- Deposit Si_3N_4 layer.



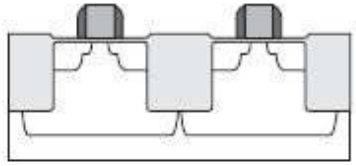
- Etch back the Si_3N_4 layer using an anisotropic etch process (directional etch). Stop on the underlying SiO_2 layer.



- Apply photoresist and pattern with the N source-drain mask.
- Ion implant the N source-drain regions with N type dopant.



- Strip N source-drain photoresist.
- Apply photoresist and pattern with the P source-drain mask.
- Ion implant the P source-drain regions with N type dopant.

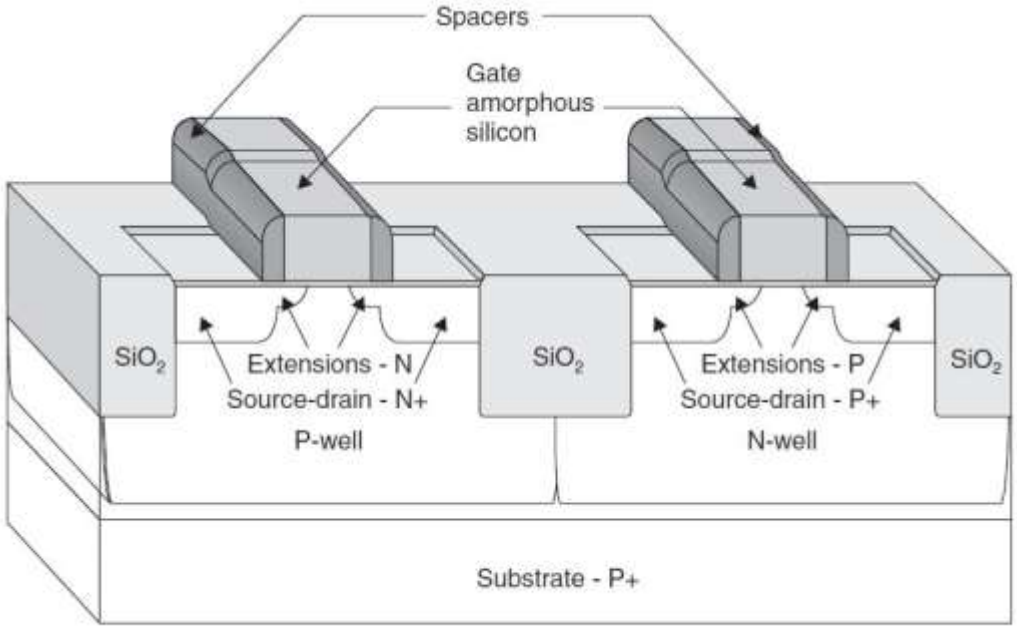


- Strip P source-drain photoresist.
- Rapid thermal anneal the drain extension and drain-source ion implants.

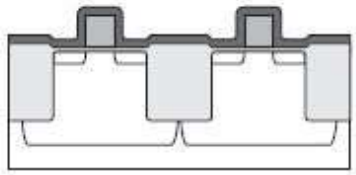
CMOS source-drain formation process

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

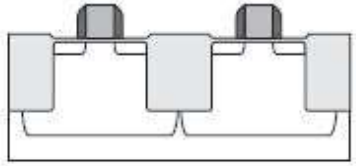
CMOS Inverter-S/D formation



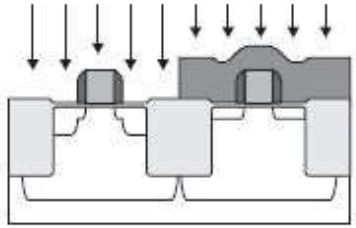
CMOS wafer following source-drain formation



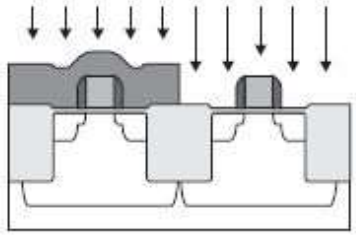
- Strip the P-extension photoresist.
- Deposit Si_3N_4 layer.



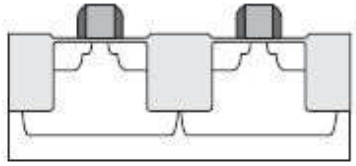
- Etch back the Si_3N_4 layer using an anisotropic etch process (directional etch). Stop on the underlying SiO_2 layer.



- Apply photoresist and pattern with the N source-drain mask.
- Ion implant the N source-drain regions with N type dopant.



- Strip N source-drain photoresist.
- Apply photoresist and pattern with the P source-drain mask.
- Ion implant the P source-drain regions with N type dopant.

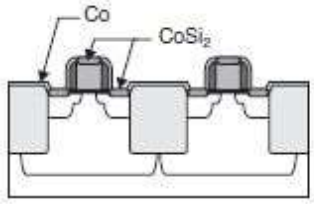


- Strip P source-drain photoresist.
- Rapid thermal anneal the drain extension and drain-source ion implants.

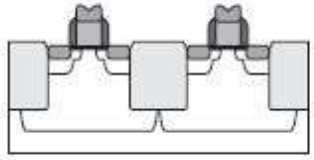
CMOS source-drain formation process

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

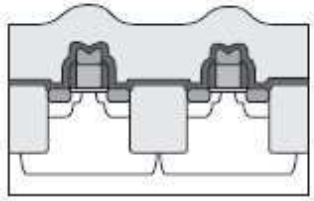
CMOS Inverter-SALICIDE & SAC contact etch



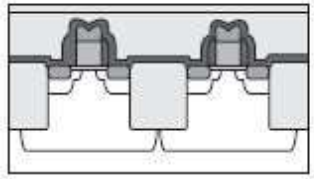
- Etch off thin oxide over the source-drains.
- Deposit thin Co metal layer.
- Rapid thermal anneal the metal layer to form $CoSi_2$ where the metal layer touches Si. No $CoSi_2$ is formed where the Co contacts SiO_2 or Si_3N_4.



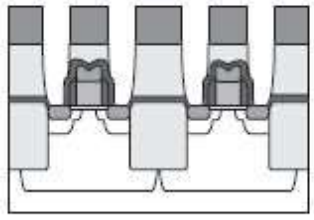
- Etch off un-reacted Co. The etch is selective removing un-reacted Co and leaving $CoSi_2$.
- Rapid thermal anneal $CoSi_2$ to create low resistance phase. This rapid thermal anneal is performed at a higher temperature than the original anneal.



- Deposit thin Si_3N_4 etch-stop layer.
- Deposit thick SiO_2 layer.



- Chemical mechanical planarization.
- Deposit a thin SiO_2 capping layer.

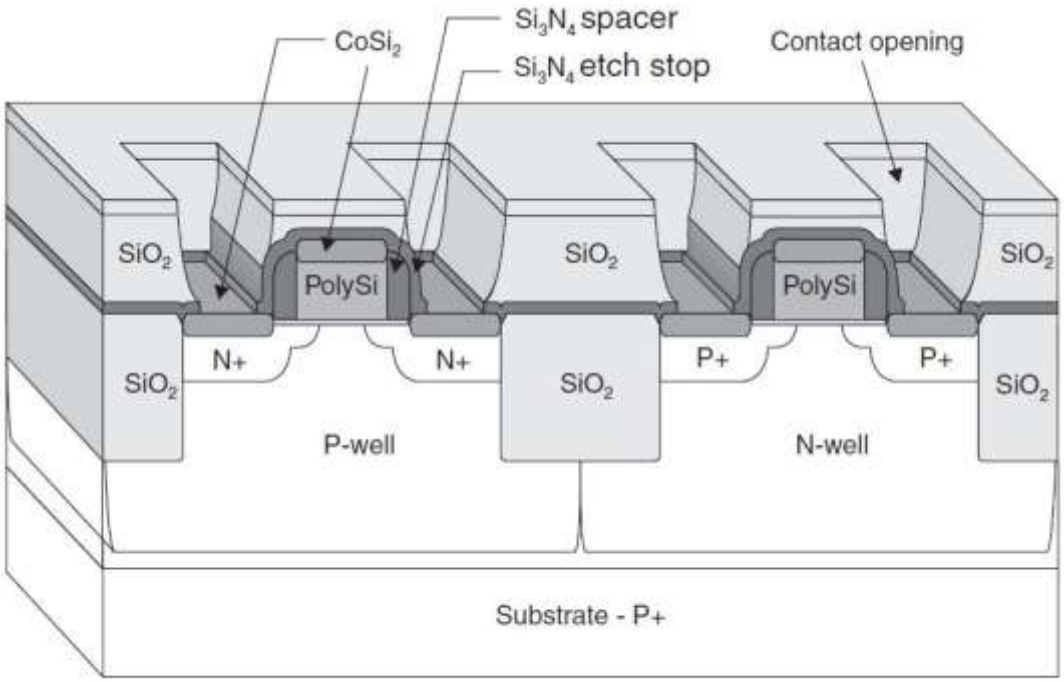


- Apply photoresist and pattern with the contact mask.
- Etch thick SiO_2 and stop on the Si_3N_4 layer.
- Etch the Si_3N_4 layer.

CMOS contact formation process

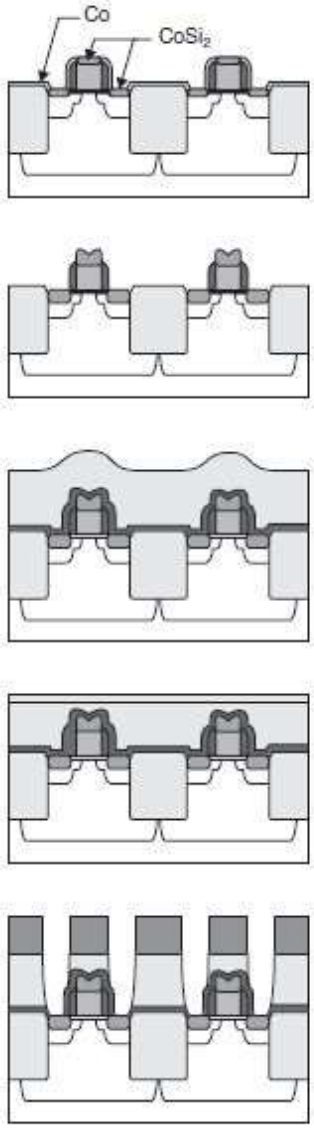
Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

CMOS Inverter-SALICIDE & SAC contact etch



CMOS wafer following contact etch

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf



- Etch off thin oxide over the source-drains.
- Deposit thin Co metal layer.
- Rapid thermal anneal the metal layer to form $CoSi_2$ where the metal layer touches Si. No $CoSi_2$ is formed where the Co contacts SiO_2 or Si_3N_4.

- Etch off un-reacted Co. The etch is selective removing un-reacted Co and leaving $CoSi_2$.
- Rapid thermal anneal $CoSi_2$ to create low resistance phase. This rapid thermal anneal is performed at a higher temperature than the original anneal.

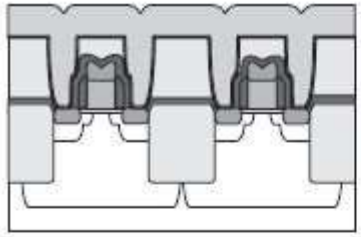
- Deposit thin Si_3N_4 etch-stop layer.
- Deposit thick SiO_2 layer.

- Chemical mechanical planarization.
- Deposit a thin SiO_2 capping layer.

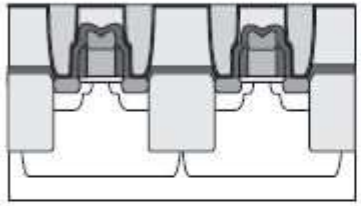
- Apply photoresist and pattern with the contact mask.
- Etch thick SiO_2 and stop on the Si_3N_4 layer.
- Etch the Si_3N_4 layer.

CMOS contact formation process

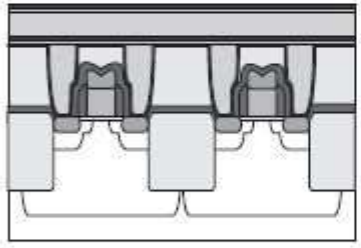
CMOS Inverter- Metal 1



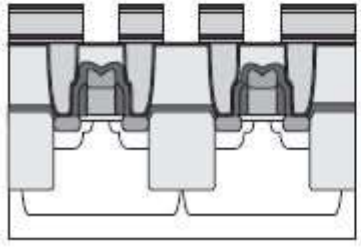
- Strip contact photoresist.
- Deposit thin Ti "glue" layer.
- Deposit thick W "plug" layer.



- Chemical mechanical planarize the W layer.



- Deposit thin Ti "glue" layer.
- Deposit thin TiN "barrier" layer.
- Deposit AlCu interconnect layer 1.
- Deposit thin Ti layer to prevent AlN formation.
- Deposit TiN antireflective layer.

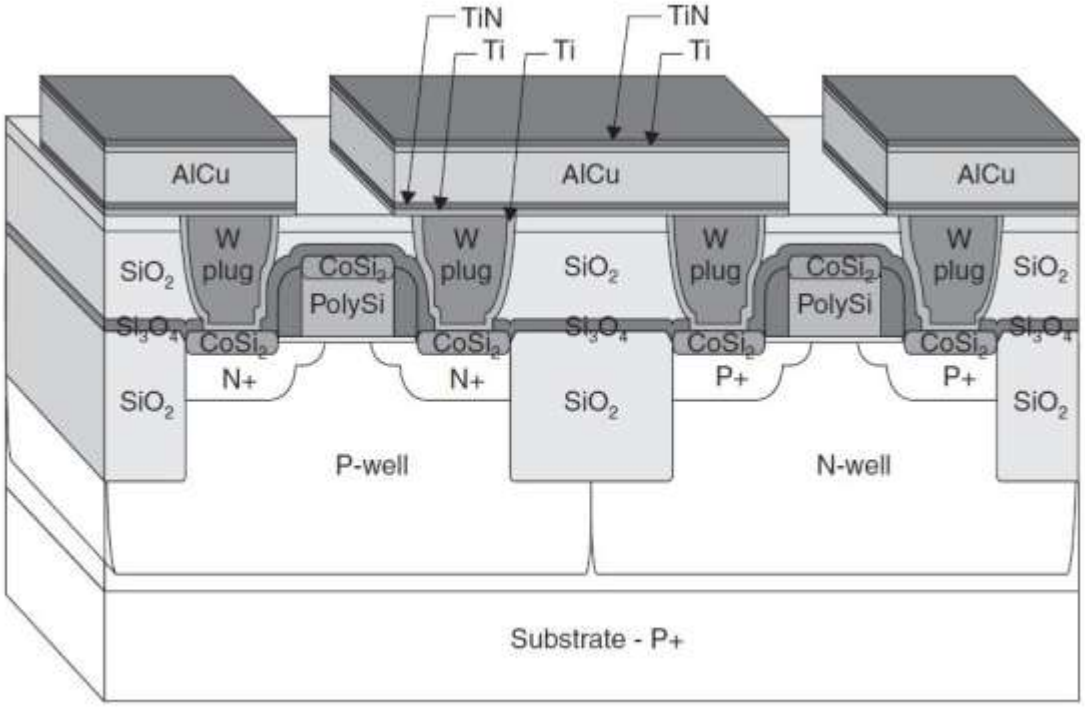


- Apply photoresist and pattern with Metal 1 mask.
- Etch metal stack.
- Strip metal 1 photoresist.

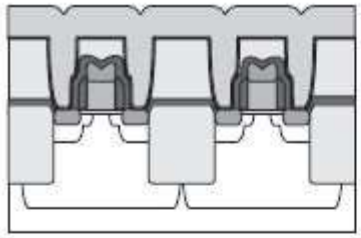
CMOS metal 1 process

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

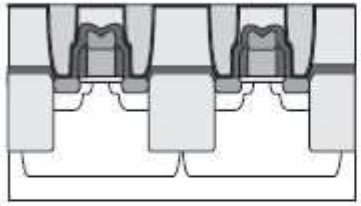
CMOS Inverter- Metal 1



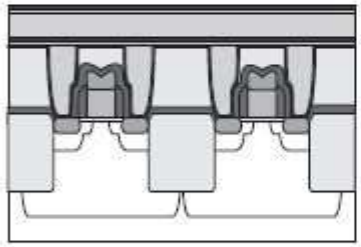
CMOS wafer after metal 1



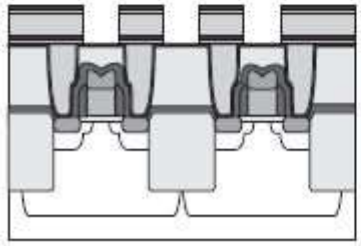
- Strip contact photoresist.
- Deposit thin Ti "glue" layer.
- Deposit thick W "plug" layer.



- Chemical mechanical planarize the W layer.



- Deposit thin Ti "glue" layer.
- Deposit thin TiN "barrier" layer.
- Deposit AlCu interconnect layer 1.
- Deposit thin Ti layer to prevent AlN formation.
- Deposit TiN antireflective layer.

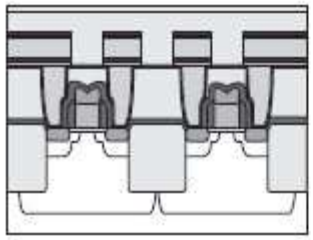


- Apply photoresist and pattern with Metal 1 mask.
- Etch metal stack.
- Strip metal 1 photoresist.

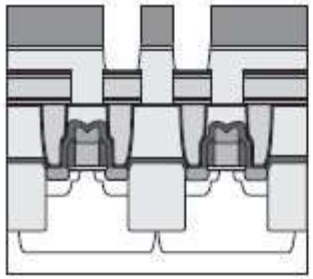
CMOS metal 1 process

Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

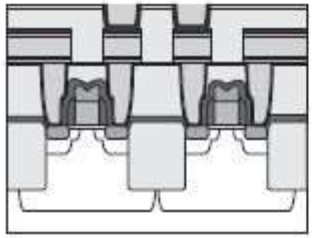
CMOS Inverter-Metal 2 +



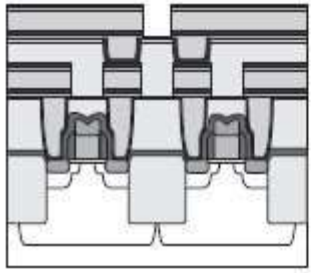
- Deposit thick inter-layer SiO_2.
- Chemical mechanical planarise SiO_2 layer.
- Deposit thin SiO_2 "capping" layer.



- Apply photoresist and pattern with Via 1 mask.
- Etch interlevel SiO_2 layer.



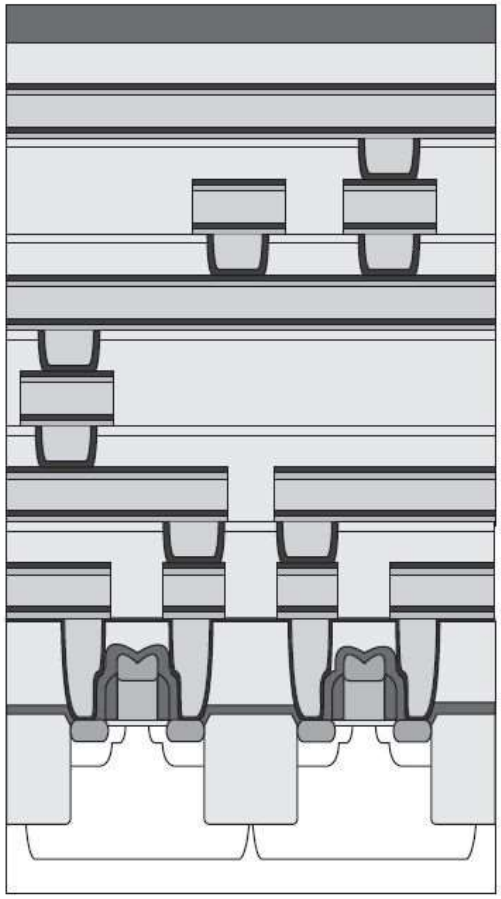
- Strip the Via 1 photoresist.
- Deposit thin Ti "glue" layer.
- Deposit thick W "Via" fill layer.
- Chemical mechanical planarise the W layer.



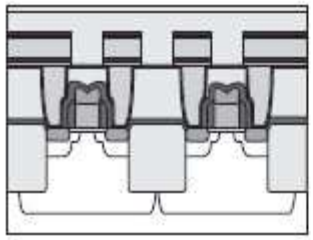
- Deposit thin Ti "glue" layer.
- Deposit thin TiN "barrier" layer.
- Deposit AlCu interconnect layer 1.
- Deposit thin Ti layer to prevent AlN formation.
- Deposit TiN antireflective layer.
- Apply photoresist and pattern with metal 2 mask.
- Etch metal stack.
- Strip metal 2 photoresist.

CMOS metal 2 process

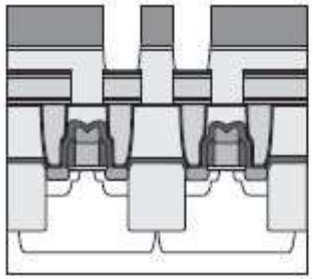
CMOS Inverter-Metal 2 +



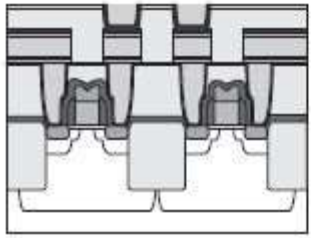
CMOS wafer with six levels of metal



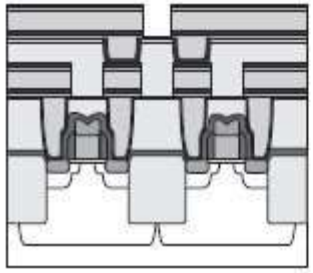
- Deposit thick inter-layer SiO_2.
- Chemical mechanical planarise SiO_2 layer.
- Deposit thin SiO_2 "capping" layer.



- Apply photoresist and pattern with Via 1 mask.
- Etch interlevel SiO_2 layer.



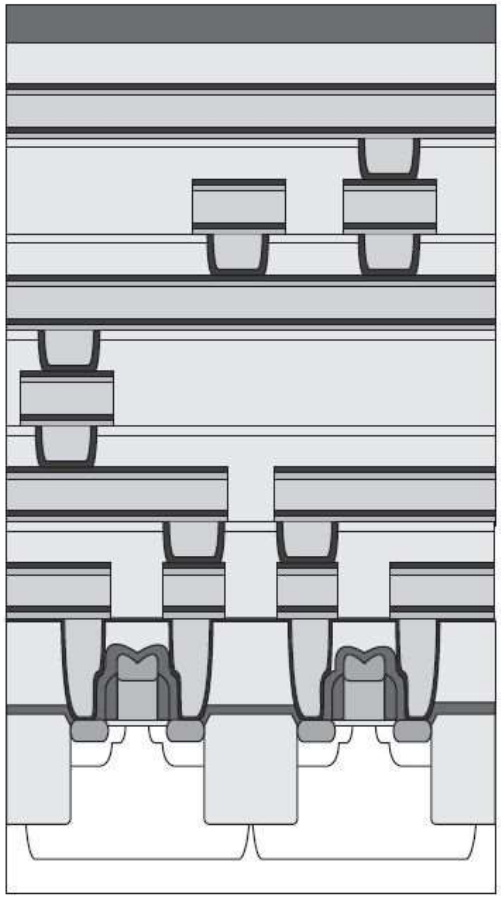
- Strip the Via 1 photoresist.
- Deposit thin Ti "glue" layer.
- Deposit thick W "Via" fill layer.
- Chemical mechanical planarise the W layer.



- Deposit thin Ti "glue" layer.
- Deposit thin TiN "barrier" layer.
- Deposit AlCu interconnect layer 1.
- Deposit thin Ti layer to prevent AlN formation.
- Deposit TiN antireflective layer.
- Apply photoresist and pattern with metal 2 mask.
- Etch metal stack.
- Strip metal 2 photoresist.

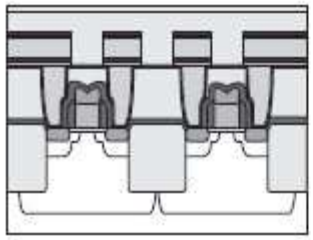
CMOS metal 2 process

CMOS Inverter-Metal 2 +

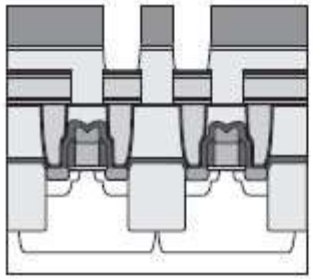


CMOS wafer with six levels of metal

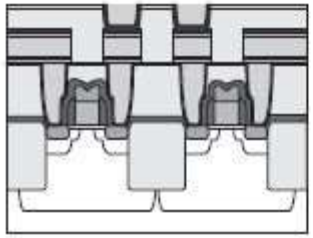
In this scheme:
Metal is etched and Oxide is polished!



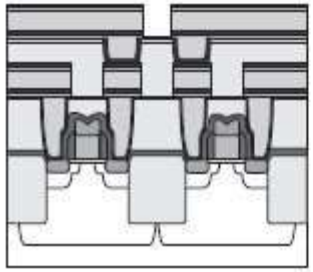
- Deposit thick inter-layer SiO_2.
- Chemical mechanical planarise SiO_2 layer.
- Deposit thin SiO_2 "capping" layer.



- Apply photoresist and pattern with Via 1 mask.
- Etch interlevel SiO_2 layer.



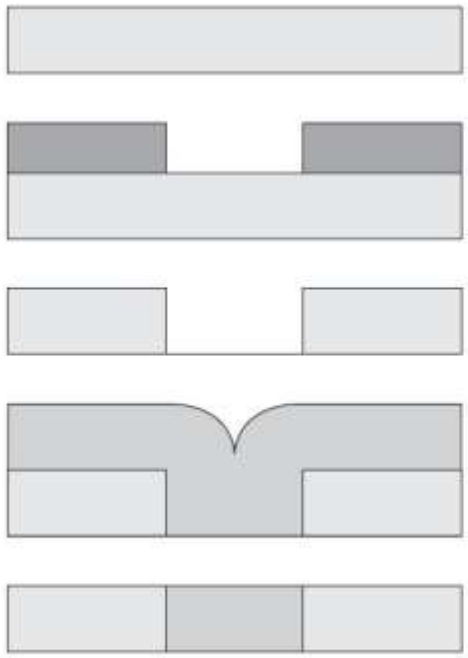
- Strip the Via 1 photoresist.
- Deposit thin Ti "glue" layer.
- Deposit thick W "Via" fill layer.
- Chemical mechanical planarise the W layer.



- Deposit thin Ti "glue" layer.
- Deposit thin TiN "barrier" layer.
- Deposit AlCu interconnect layer 1.
- Deposit thin Ti layer to prevent AlN formation.
- Deposit TiN antireflective layer.
- Apply photoresist and pattern with metal 2 mask.
- Etch metal stack.
- Strip metal 2 photoresist.

CMOS metal 2 process

Alternative Metallization Scheme

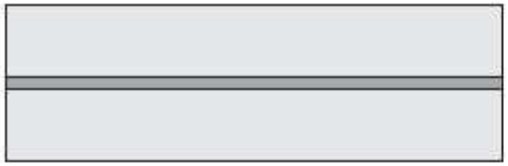


- Deposit SiO_2 layer
- Apply photoresist and pattern
- Etch photoresist pattern into the SiO_2 layer.
- Deposit metal layer
- Planarize the metal flat with the SiO_2

Damascene process

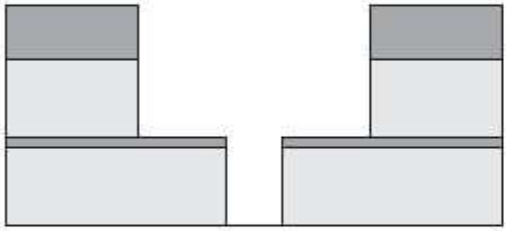
Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

Alternative Metallization Scheme

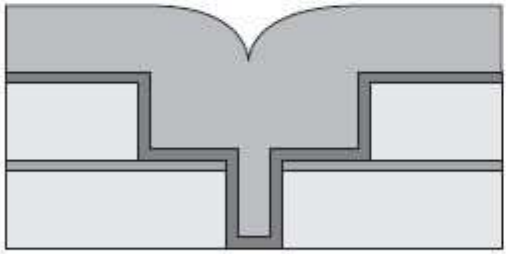


- Deposit SiO_2 interlayer
- Deposit Si_3N_4 etch stop layer
- Deposit SiO_2 interconnect layer

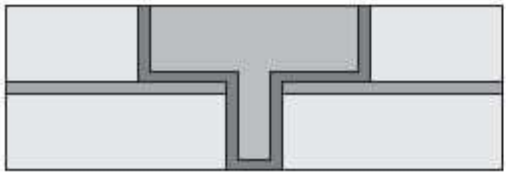
- Apply photoresist and pattern with the via mask
- Etch SiO_2, stop on the Si_3N_4
- Etch Si_3N_4



- Apply photoresist and pattern with the metal mask
- Etch SiO_2, stop on the Si_3N_4, this etch etches the metal area and completes the via etch simultaneously.



- Sputter deposit TaN barrier layer
- Sputter deposit Cu "seed" layer
- Electroplate Cu to fill via and metal opening.

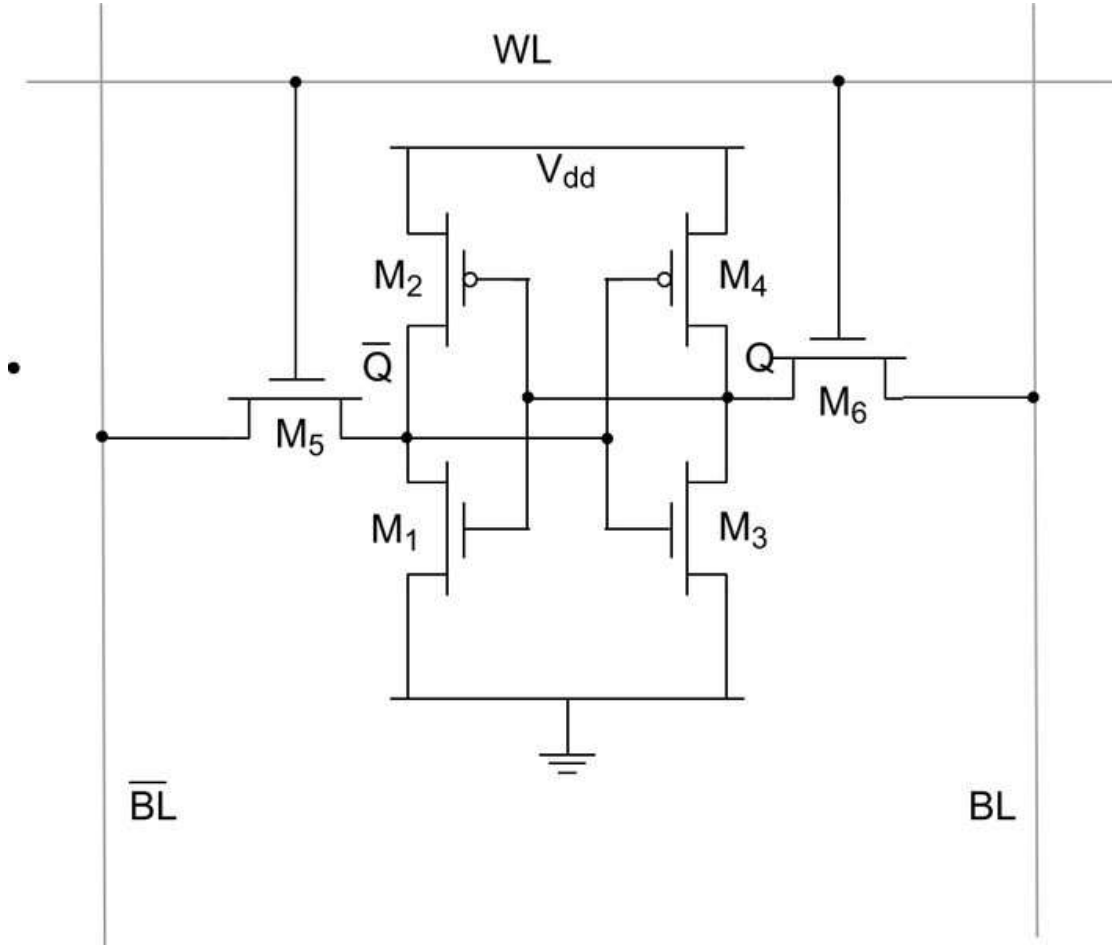


- CMP planarize the metal layer

Copper dual damascene process

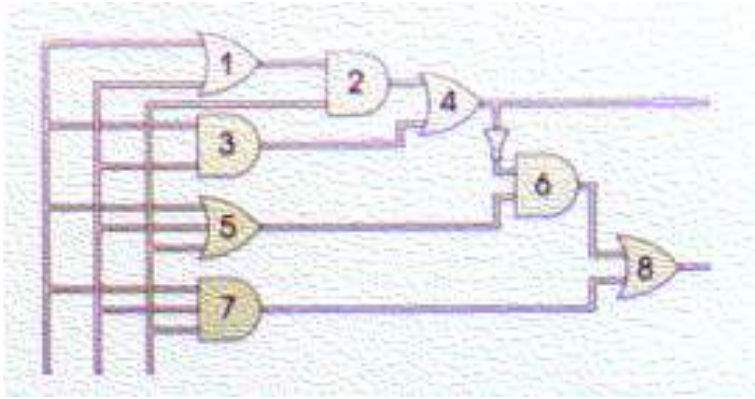
Taken from IC Knowledge 2008
http://www.icknowledge.com/misc_technology/Overview%20Post.pdf

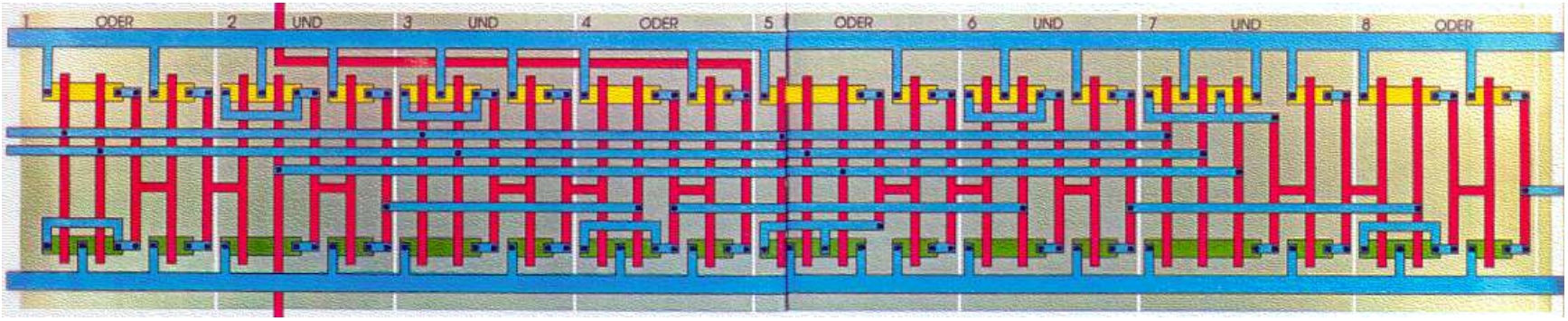
CMOS SRAM



Example for a logic circuit: CMOS Adder

Integrated Circuit of a Logic Adder





Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

»Wissen schafft Brücken.«