TECHNISCHE UNIVERSITÄT DRESDEN

The hyperlinks to the video streams in this virtual lecture are marked by the Video Campus Sachsen Logo.
To watch them you need to be logged on at the host: VCS. Please click on: https://videocampus.sachsen.de/login
select TU-Dresden in the selection mask and than logon with the same ID and password as you use for OPAL or ZIH. Stay logged on as long as you work with the lecture slides.

Lecture SCT2 – Process Integration

13. Web-based virtual Lecture: July 15 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here 

"SCT_SS21_13.1" 09:11

This document including the contained video streams is only available to students of the lecture „Semiconductor Technology 2" at TU-Dresden.
It must not be copied and published outside of TUD!
It is intended for
TUD internal use only!

Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

Review:

- SCT Basics
- MOS-Cap-CV
- MOS-FET (N-FET enh.)
- Al-Gate FET
- SRAM product (E/E)
- V_T adjust => Depl.
- E/D Logic
- Self aligned process
- ~180 nm CMOS Process

Today: Further Scaling

Continue

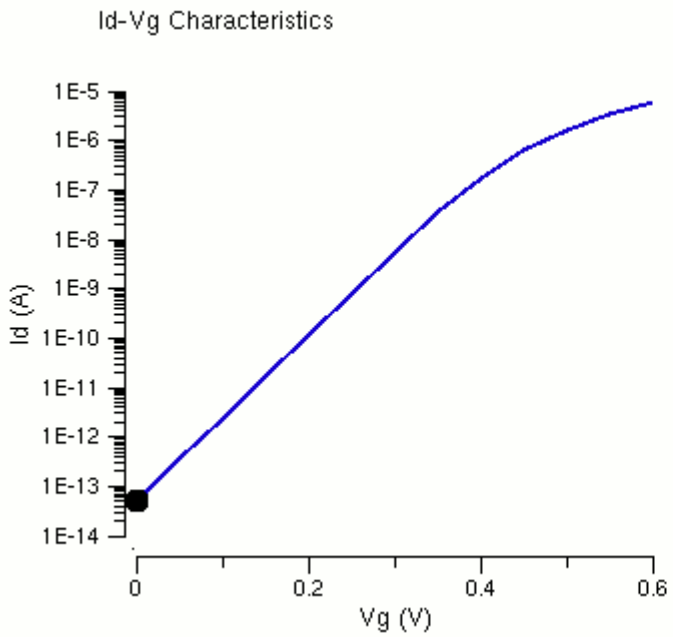
"SCT_SS20_13.2" 48:07

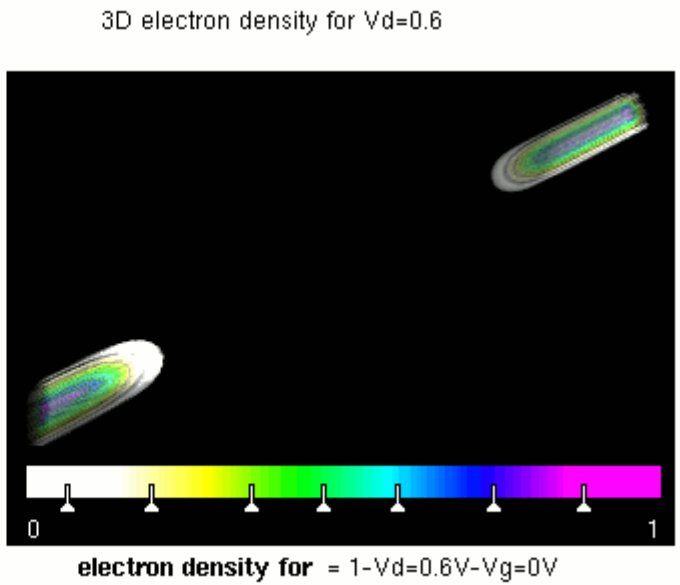
http://www.computerhistory.org/siliconengine/timeline/

5. Further considerations

Semiconductor device fabrication

Half-nodes
Density
CMOS
Device (multi-gate)
Moore's law
Semiconductor Nanoelectronics





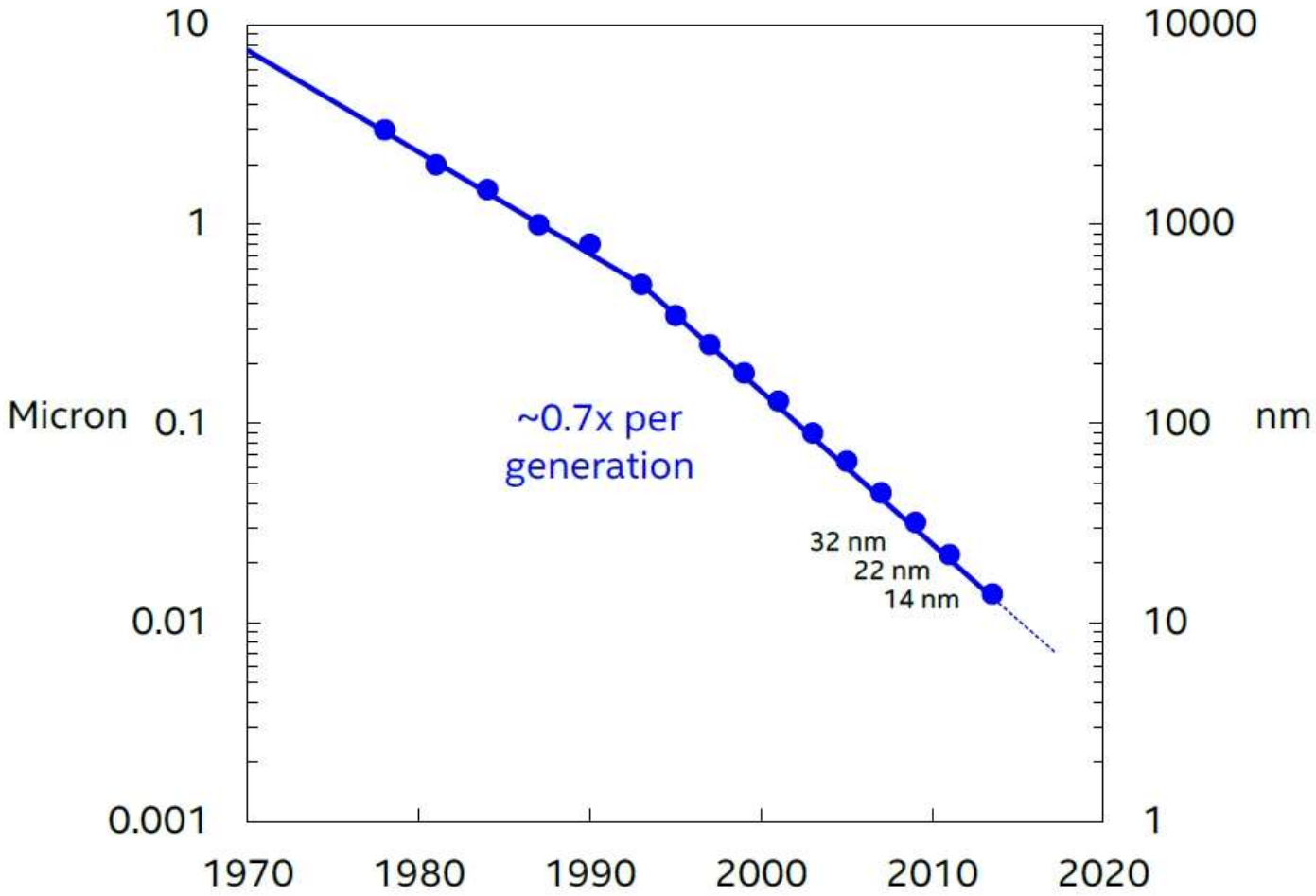
MOSFET scaling (process nodes)

- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018

- Future 5 nm – *~2020*
- 3 nm – *~2022*

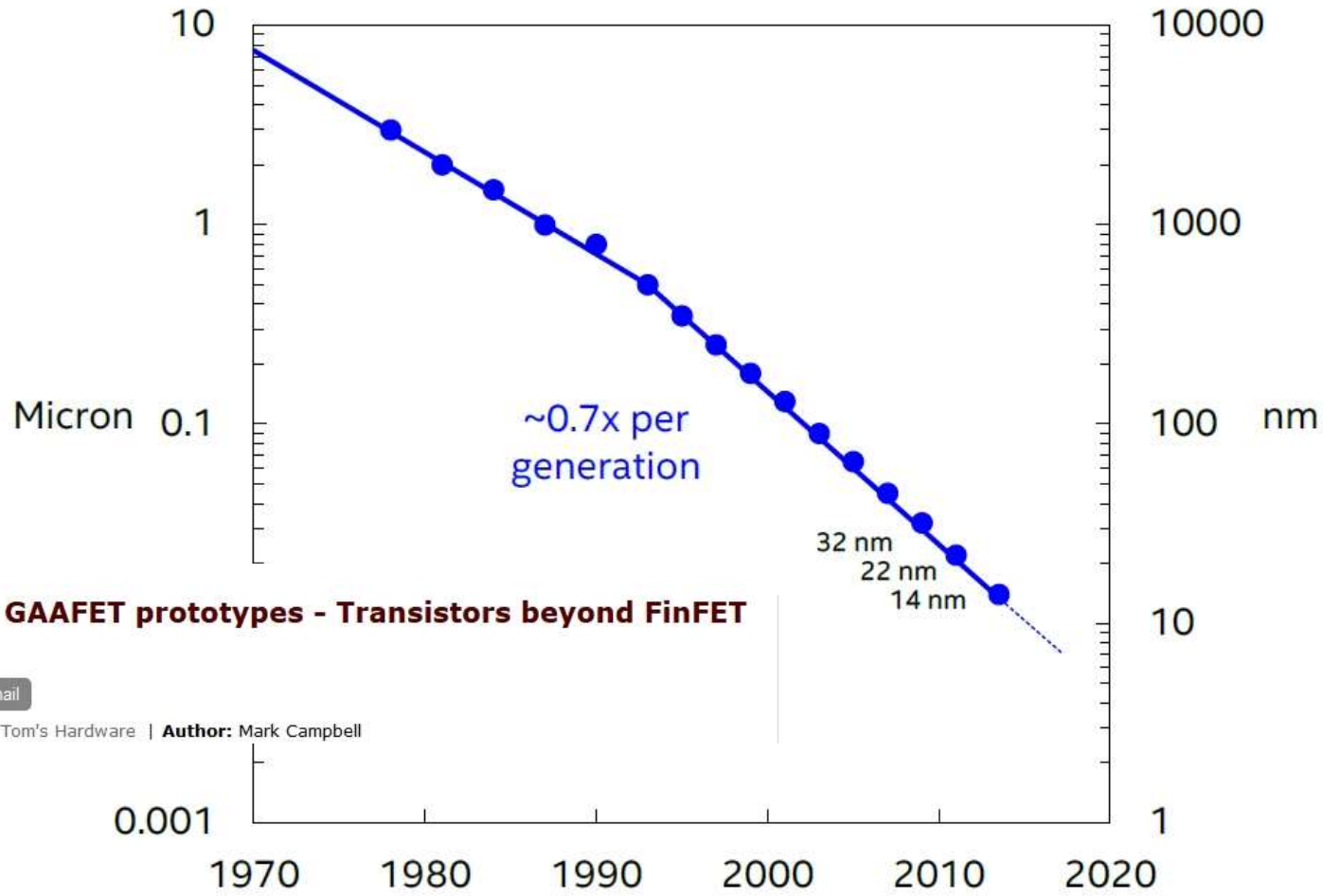
https://www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf

Intel Scaling Trend



https://www.intel.com/content/dam/www/public/us/en/documents/pdf/foundry/mark-bohr-2014-idf-presentation.pdf

Intel Scaling Trend



Samsung has created its first 3nm GAAFET prototypes - Transistors beyond FinFET

Should TSMC be worried?

Facebook Twitter Reddit WhatsApp Email

Published: 4th January 2020 | **Source:** Maeil Economy - Via Tom's Hardware | **Author:** Mark Campbell

5.1 Scaling

Small transistors switch faster!

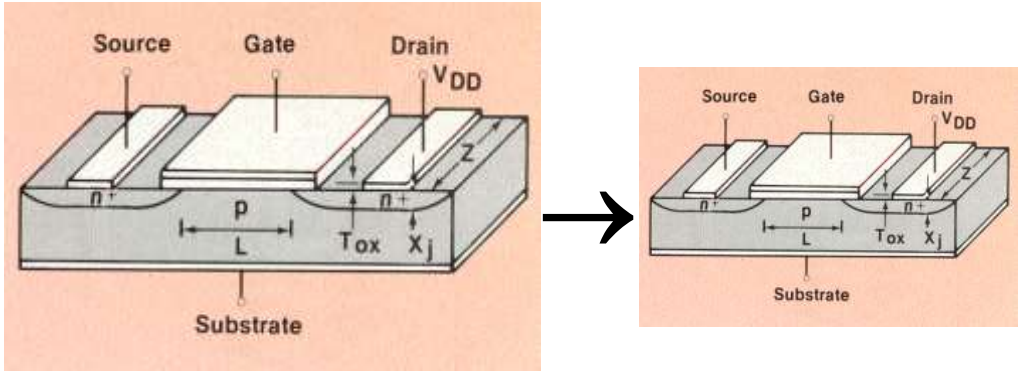


Table II—Scaling Factor

Scaling Factor	$S>1$
Lateral Dimensions	$L \rightarrow L/S$ $Z \rightarrow Z/S$
Vertical Dimensions	$T_{OX} \rightarrow T_{OX}/S$ $X_j \rightarrow X_j/S$
Supply Voltage	$V_{DD} \rightarrow V_{DD}/S$
Substrate Doping Concentration	$N_A \rightarrow SN_A$

Robert H. Dennard, IBM 1974

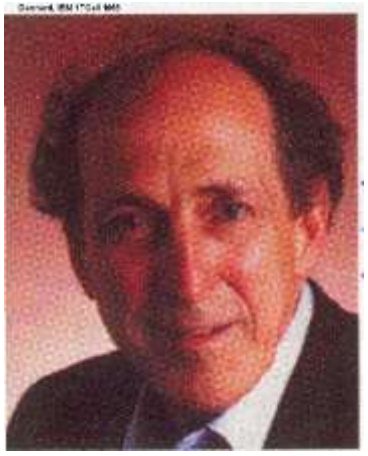
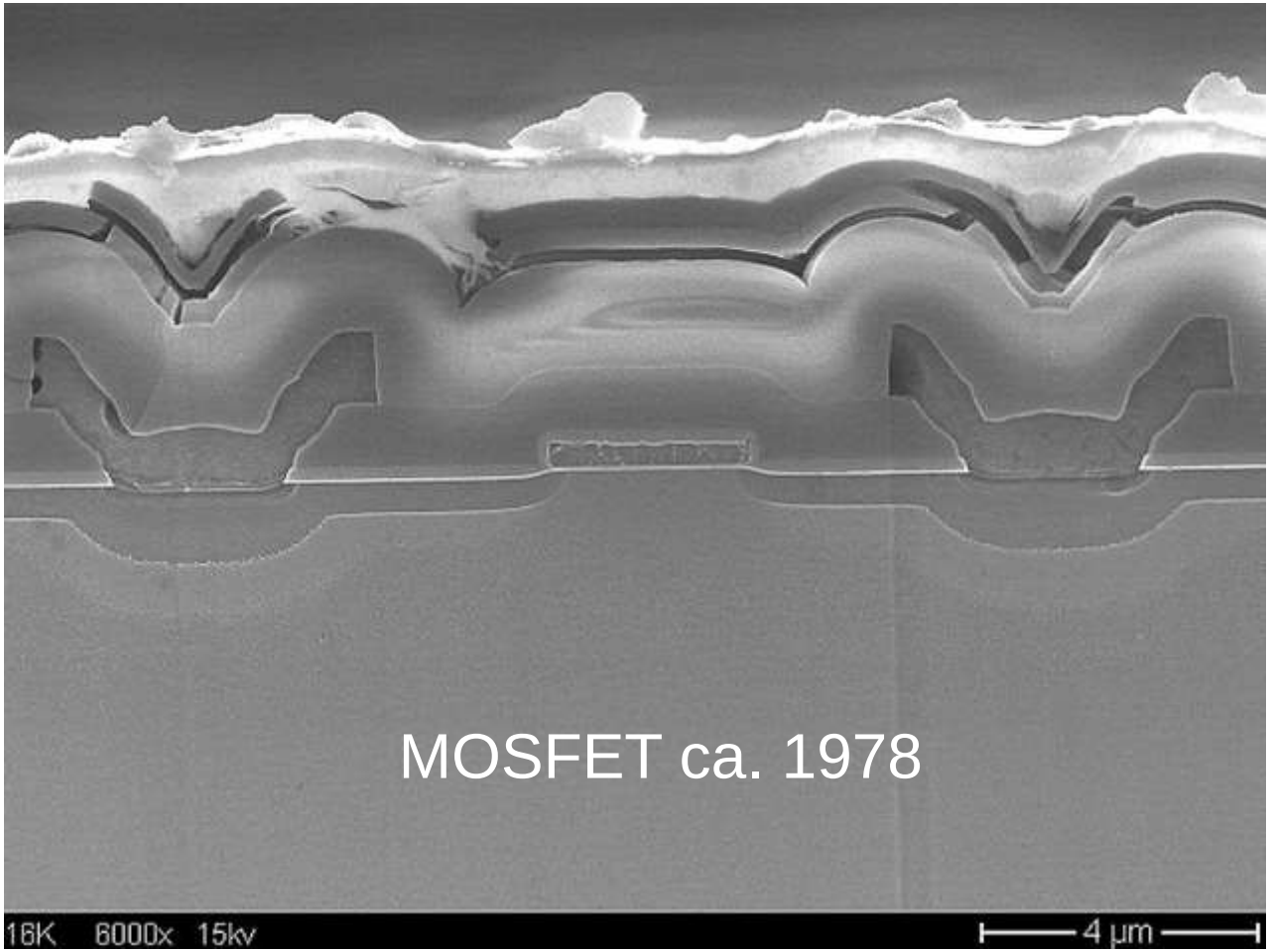


Table III—MOSFET Device Scaling for Constant Field

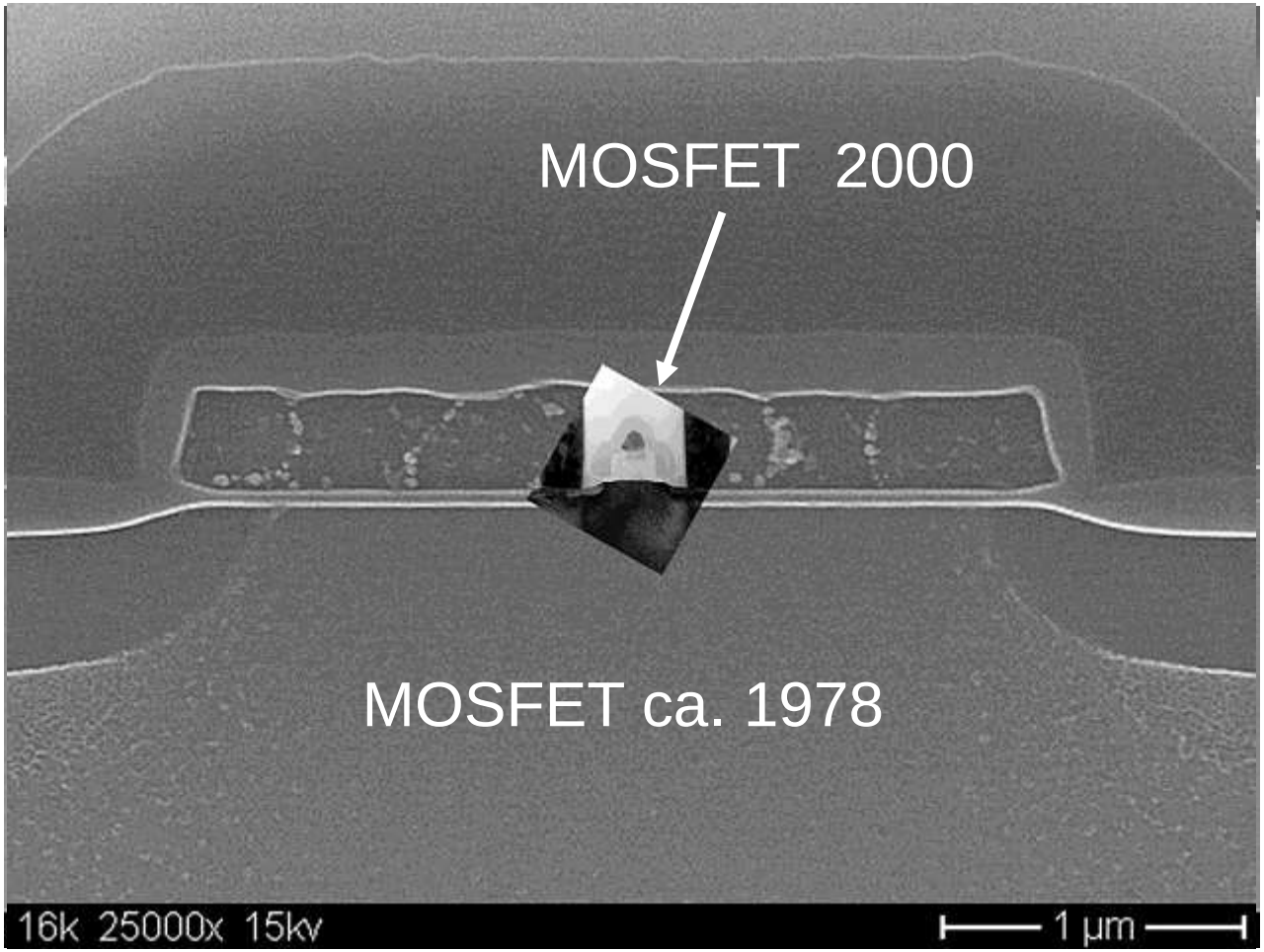
Device Parameter	Scaling Factor
Device Delay	$1/S$
Capacitance	$1/S$
Power Dissipation/Device	$1/S^2$
Power Density	1
Packing Density	S^2
Power Delay Product/Device	$1/S^3$

Evolution of scaling



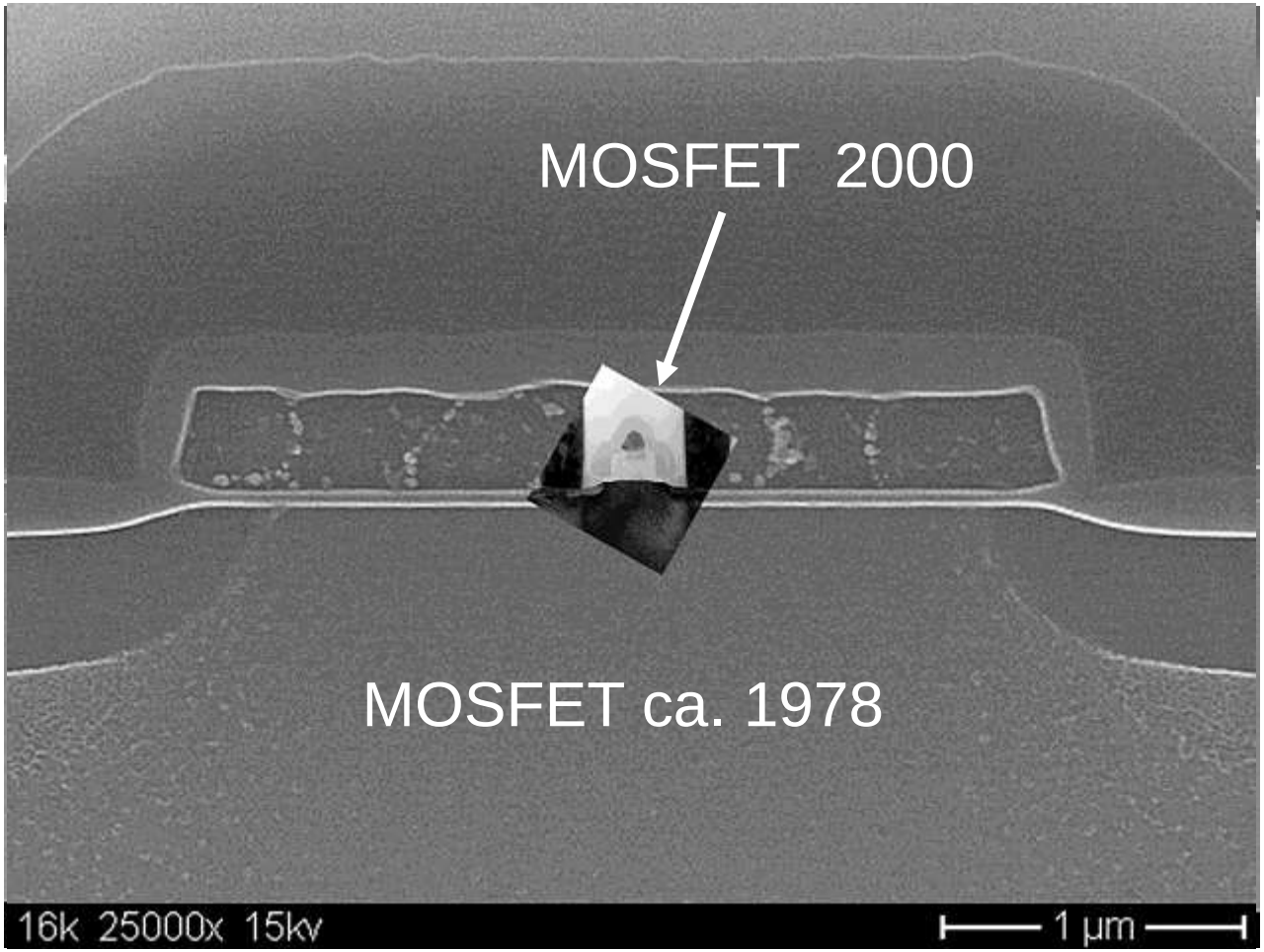
Source: C. Esser, Dresden Mikroelektronik Sommerschule 2007

Evolution of scaling



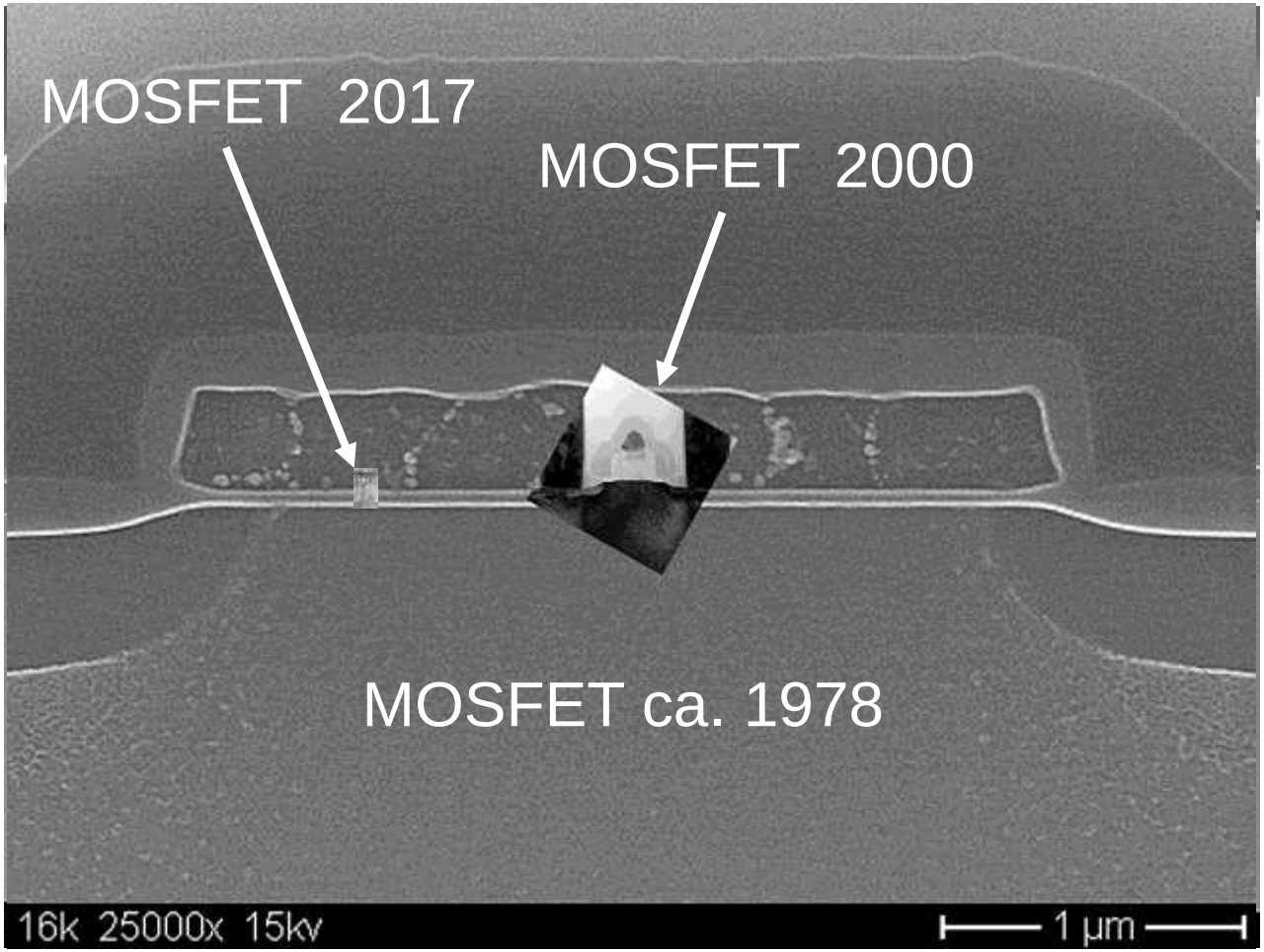
Source: C. Esser, Dresden Mikroelektronik Sommerschule 2007

Evolution of scaling



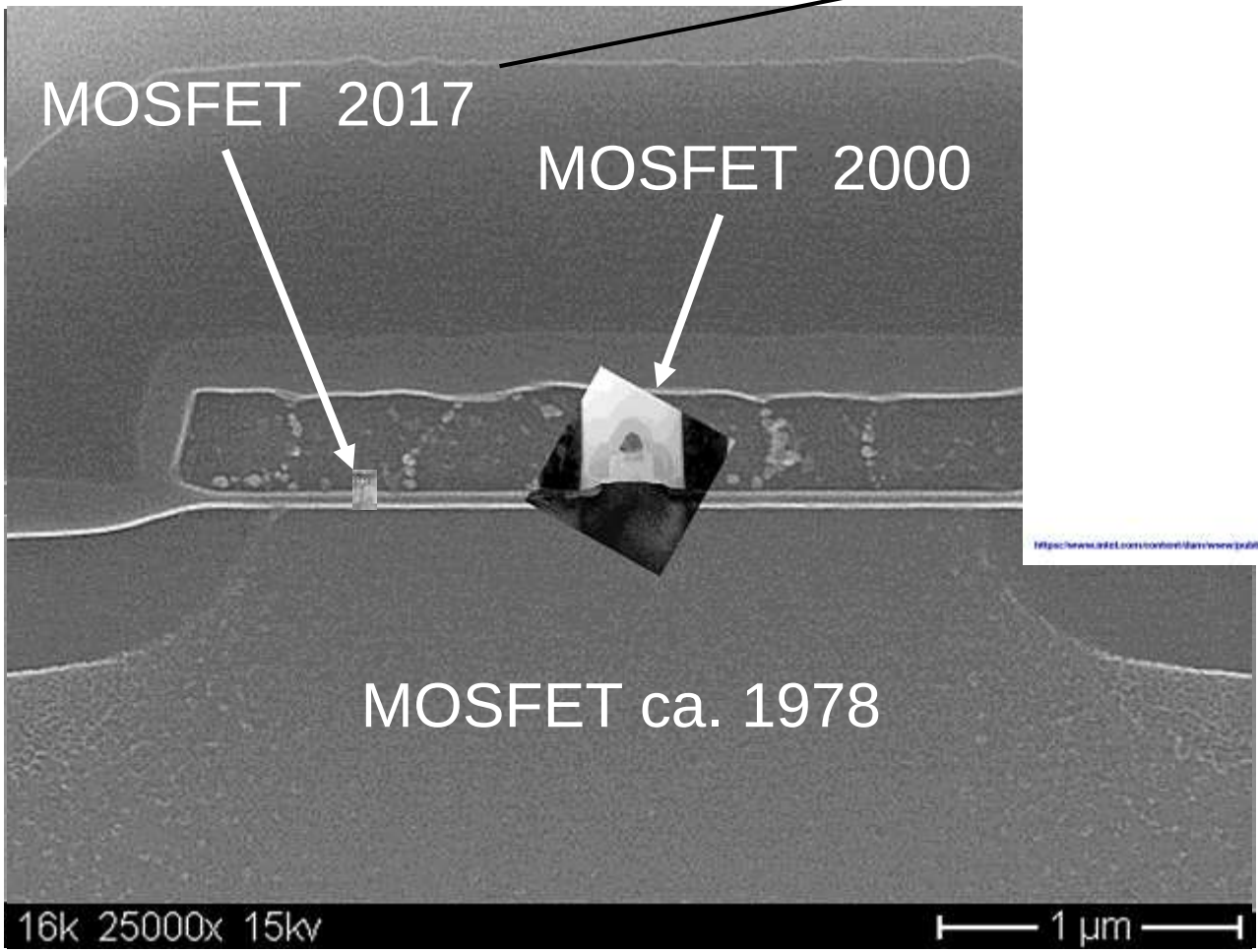
Source: C. Esser, Dresden Mikroelektronik Sommerschule 2007

Evolution of scaling



Source: C. Esser, Dresden Mikroelektronik Sommerschule 2007

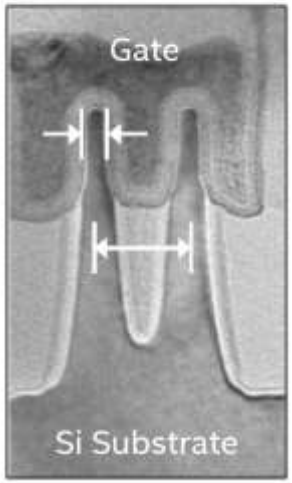
Evolution of scaling



14 nm Tri-gate Transistor Fins

8 nm Fin Width

42 nm Fin Pitch



Source: C. Esser, Dresden Mikroelektronik Sommerschule 2007

Emerging MOSFET with 6nm channel

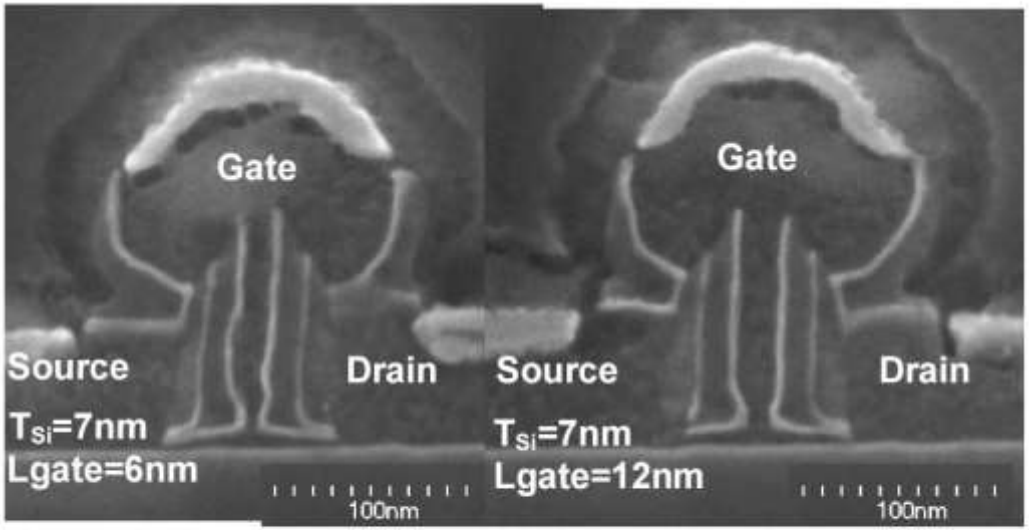


Fig.17: SEM cross-section of ultra-thin silicon channel pFETs with 6nm and 12nm gate lengths

IBM 2002 IEDM 2002

-SOI Substrate
- Gate Dielectric – nitride/oxide
- 248 nm Litho
- Epi raised Source/Drain

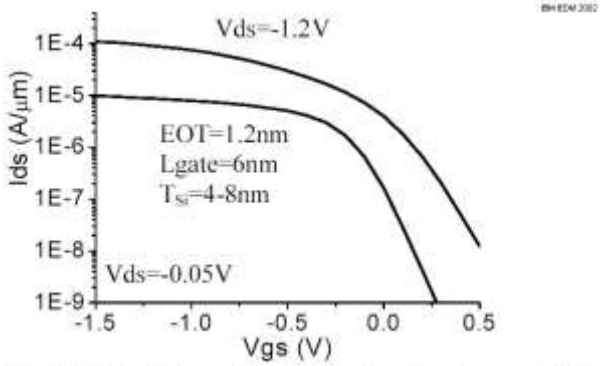


Fig.18: Ids-Vgs characteristic of a 6nm pFET

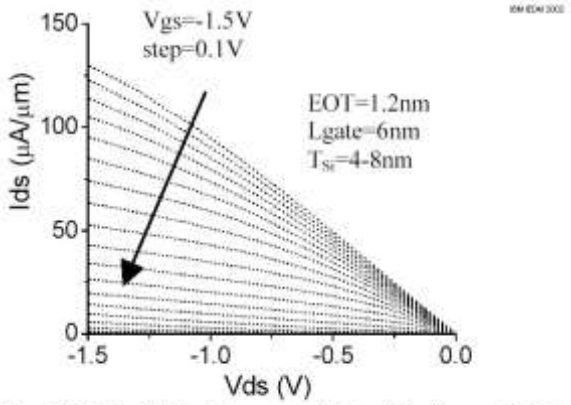


Fig.19: Ids-Vds characteristic of a 6nm pFET

Emerging MOSFET with 6nm channel

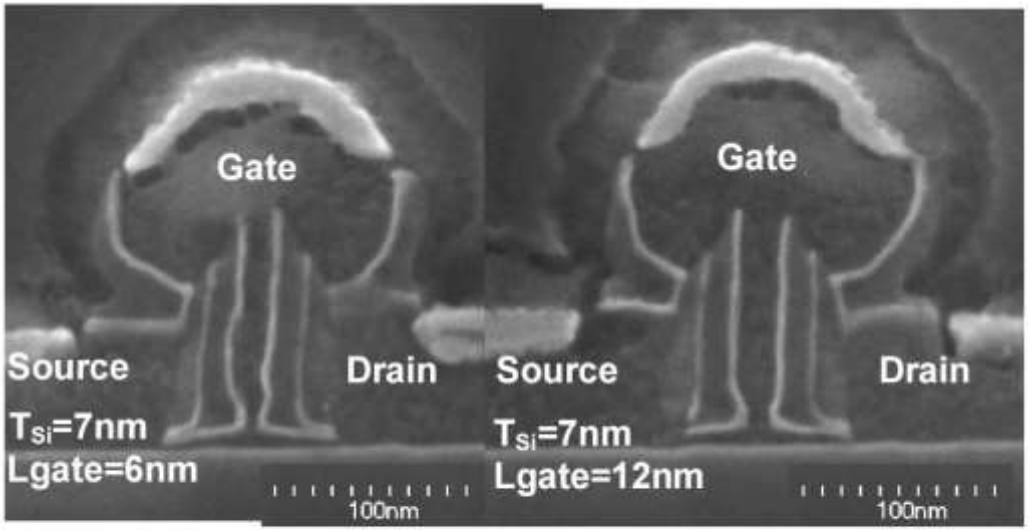


Fig.17: SEM cross-section of ultra-thin silicon channel pFETs with 6nm and 12nm gate lengths

IBM 2002 IEDM 2002

-SOI Substrate
- Gate Dielectric – nitride/oxide
- 248 nm Litho
- Epi raised Source/Drain

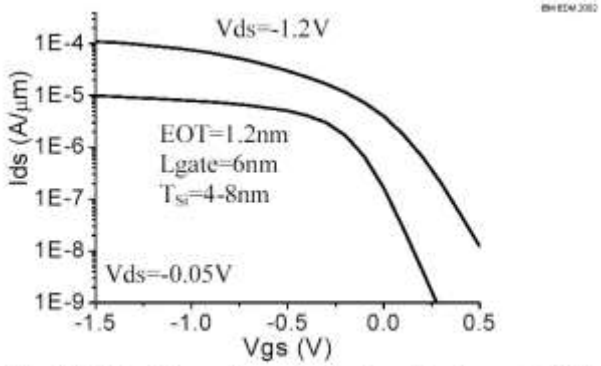


Fig.18: Ids-Vgs characteristic of a 6nm pFET

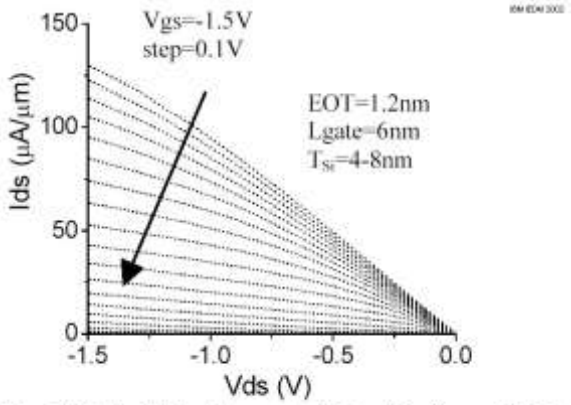


Fig.19: Ids-Vds characteristic of a 6nm pFET

IBM at IEDM 2002

Emerging MOSFET with 6nm channel

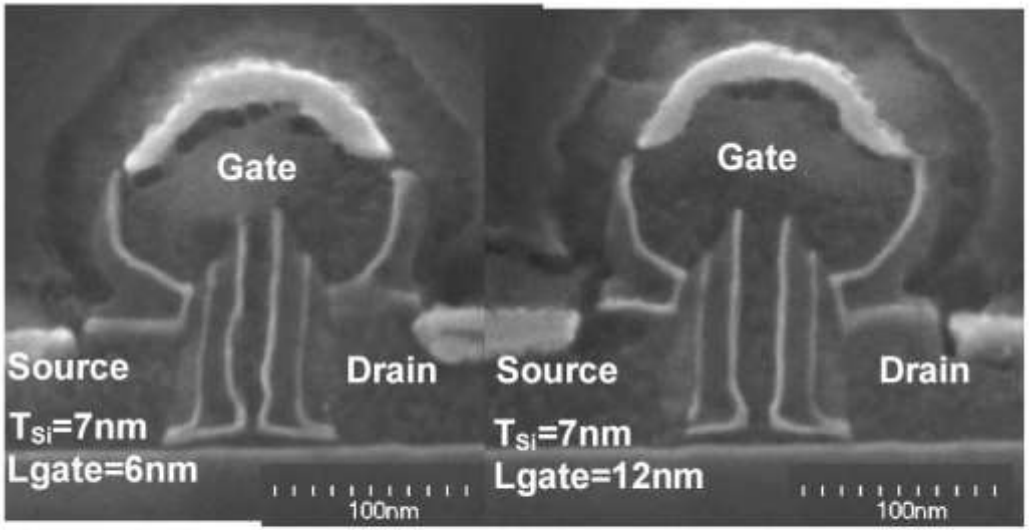


Fig.17: SEM cross-section of ultra-thin silicon channel pFETs with 6nm and 12nm gate lengths

IBM 2002 IEDM 2002

-SOI Substrate
- Gate Dielectric – nitride/oxide
- 248 nm Litho
- Epi raised Source/Drain

Limits to Binary Logic Switch Scaling—A Gedanken Model

VICTOR V. ZHIRNOV, RALPH K. CAVIN, III, FELLOW, IEEE, JAMES A. HUTCHBY, SENIOR MEMBER, IEEE, AND GEORGE I. BOURIANOFF, MEMBER, IEEE

Invited Paper

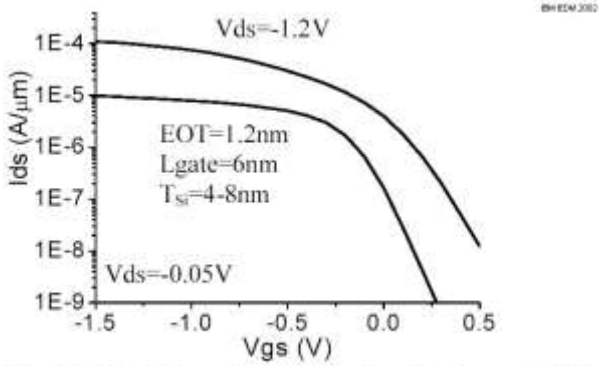


Fig.18: Ids-Vgs characteristic of a 6nm pFET

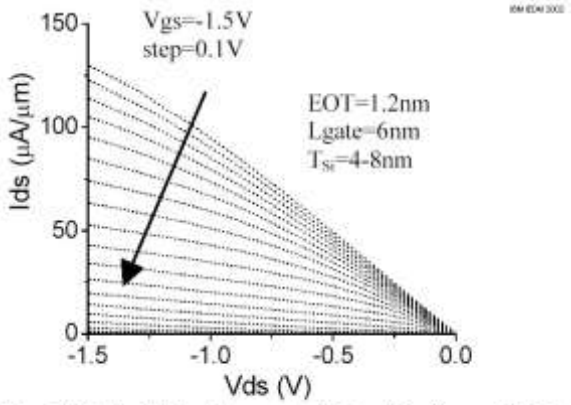


Fig.19: Ids-Vds characteristic of a 6nm pFET

IBM at IEDM 2002

5.1.1. Challenges of Scaling

Classical scaling hits limits:

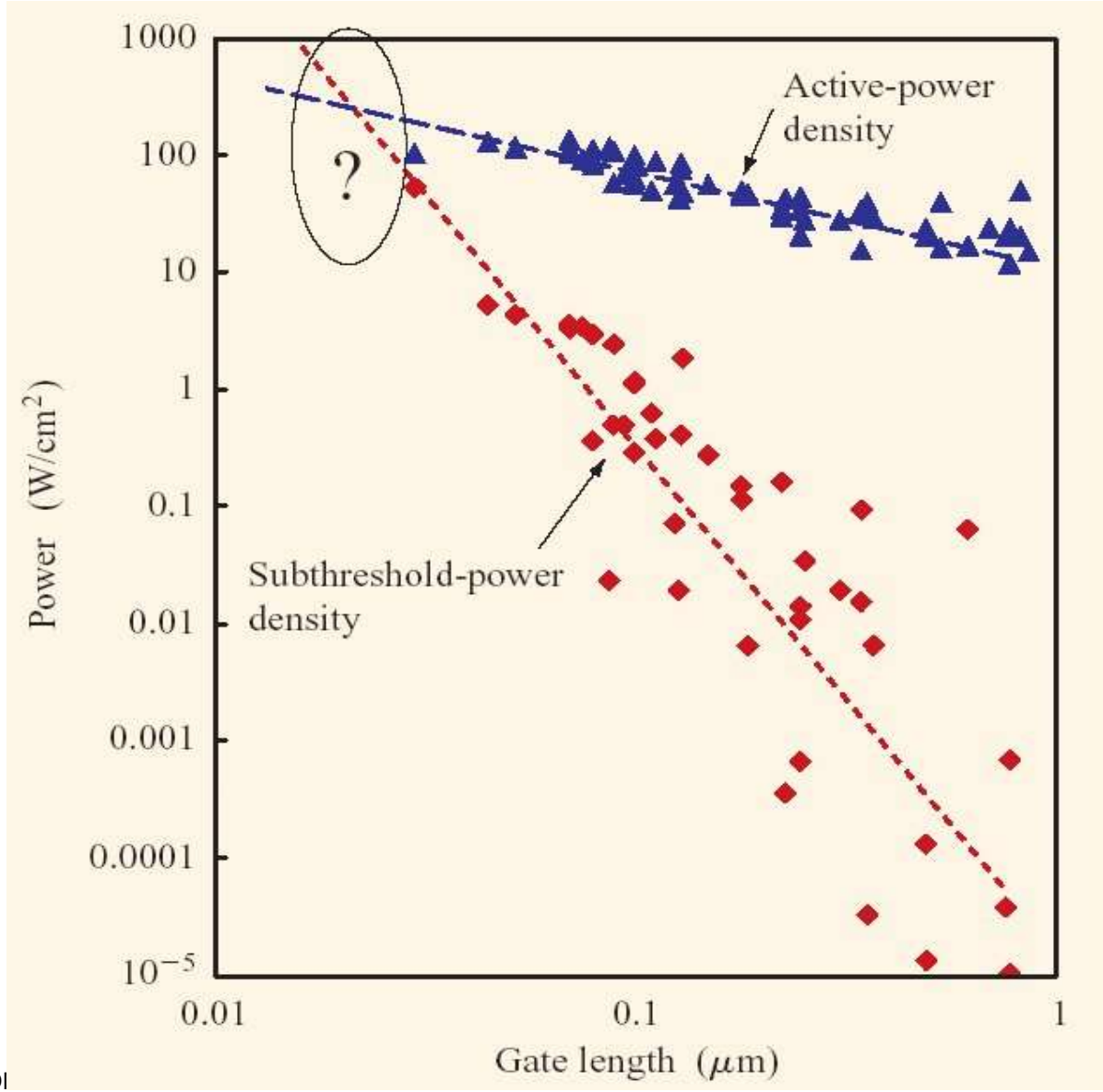
- Leakage current (S/D and Gate/Body)
- Variability of process parameters
- Thermal management
- Interconnects limit switching speed

… and much more

Active Power scales with frequency

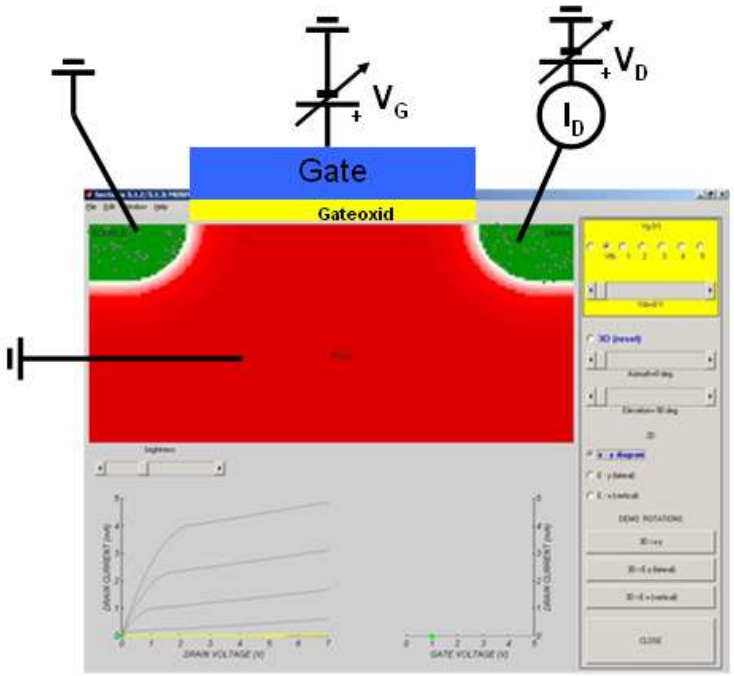
$$P_{active} = \alpha C f V^2$$

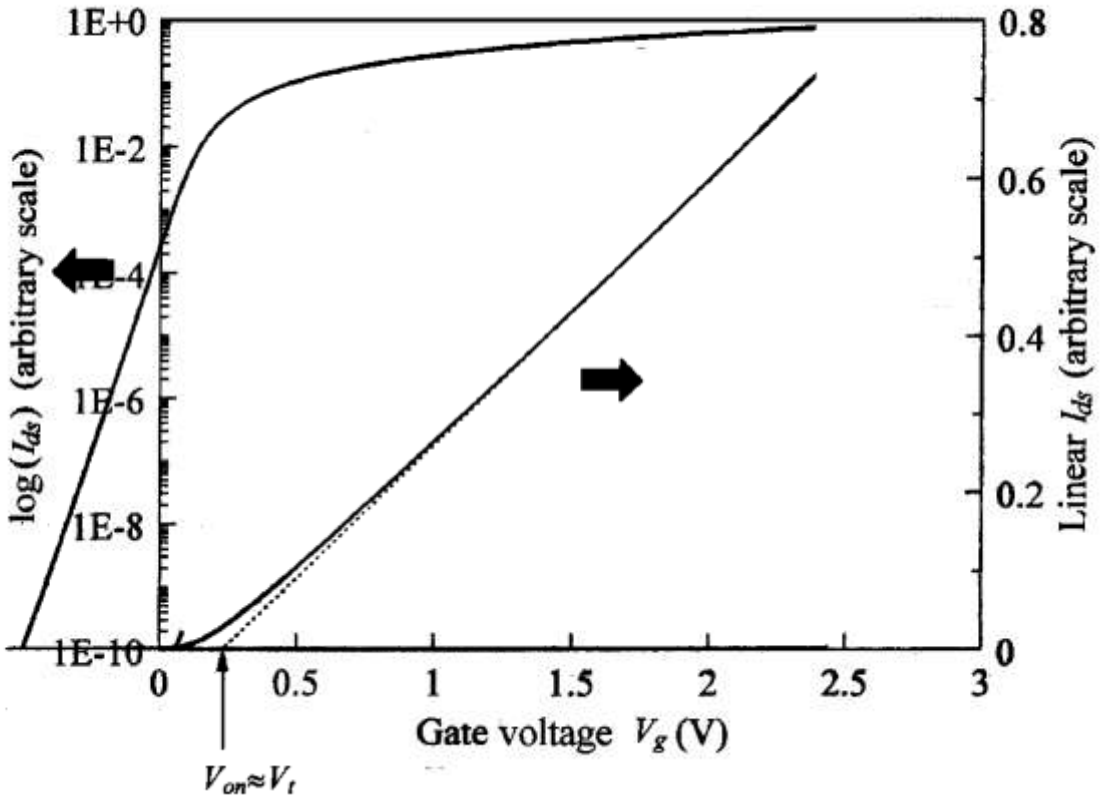
Passive Power scales with the leakage current per transistor times # of transistors



Sub threshold current slope depends only on temperature

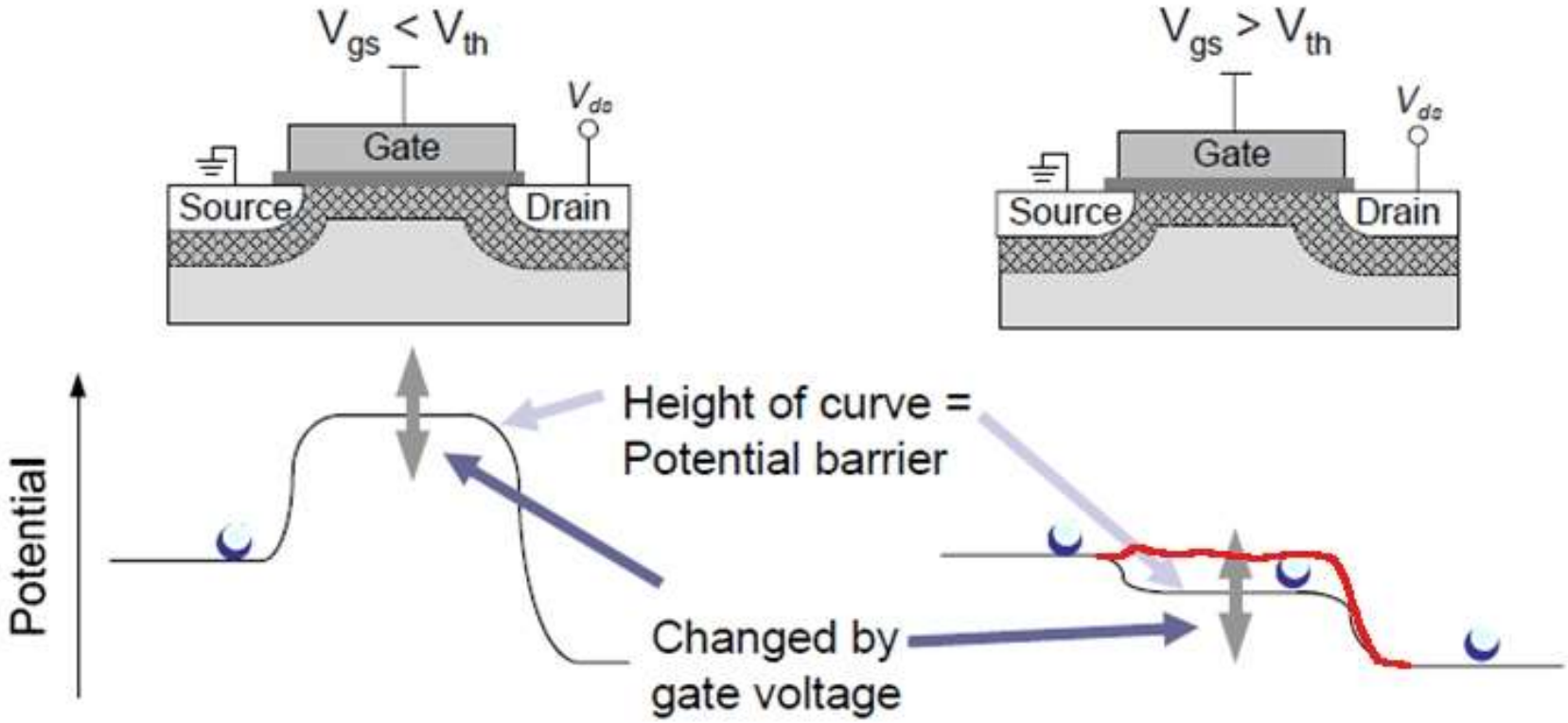
(Nothing you can do, at its best it is fixed to 60 mV/dec)





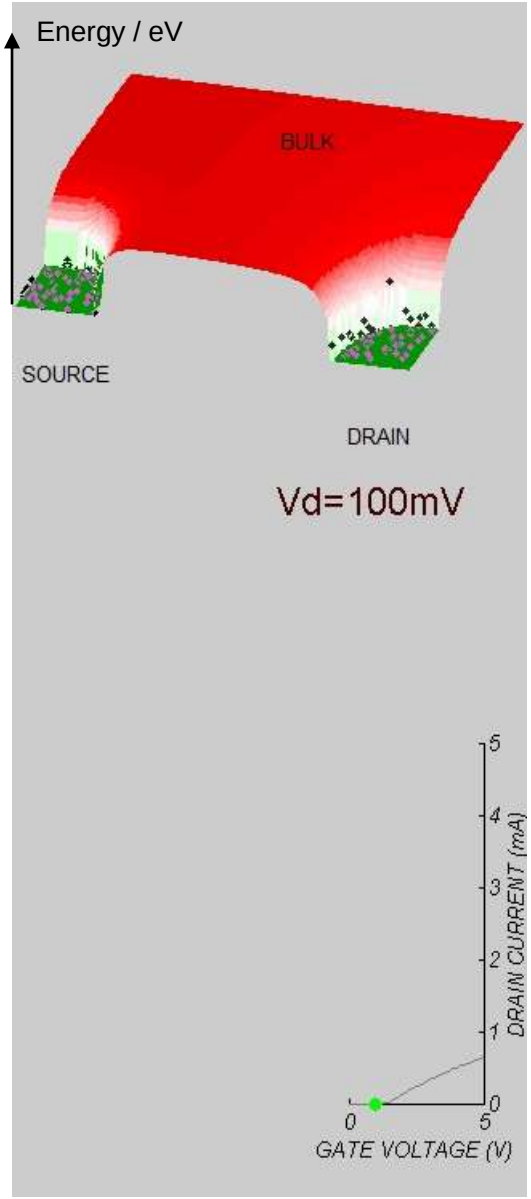
Low V_{dd} means low I_{on}/I_{off} ratio!

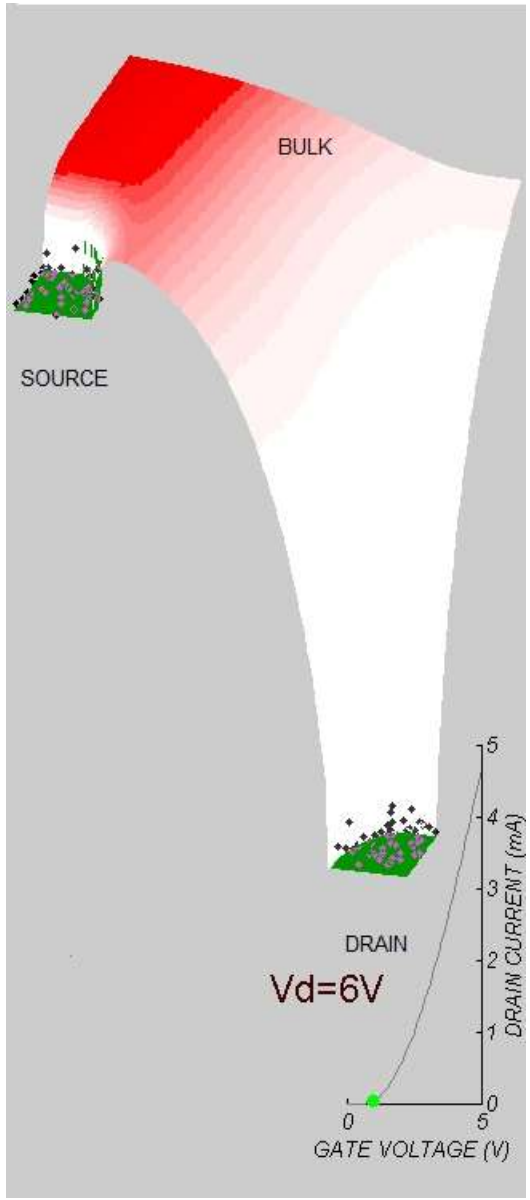
Short channel effects:
Drain induced barrier lowering DIBL

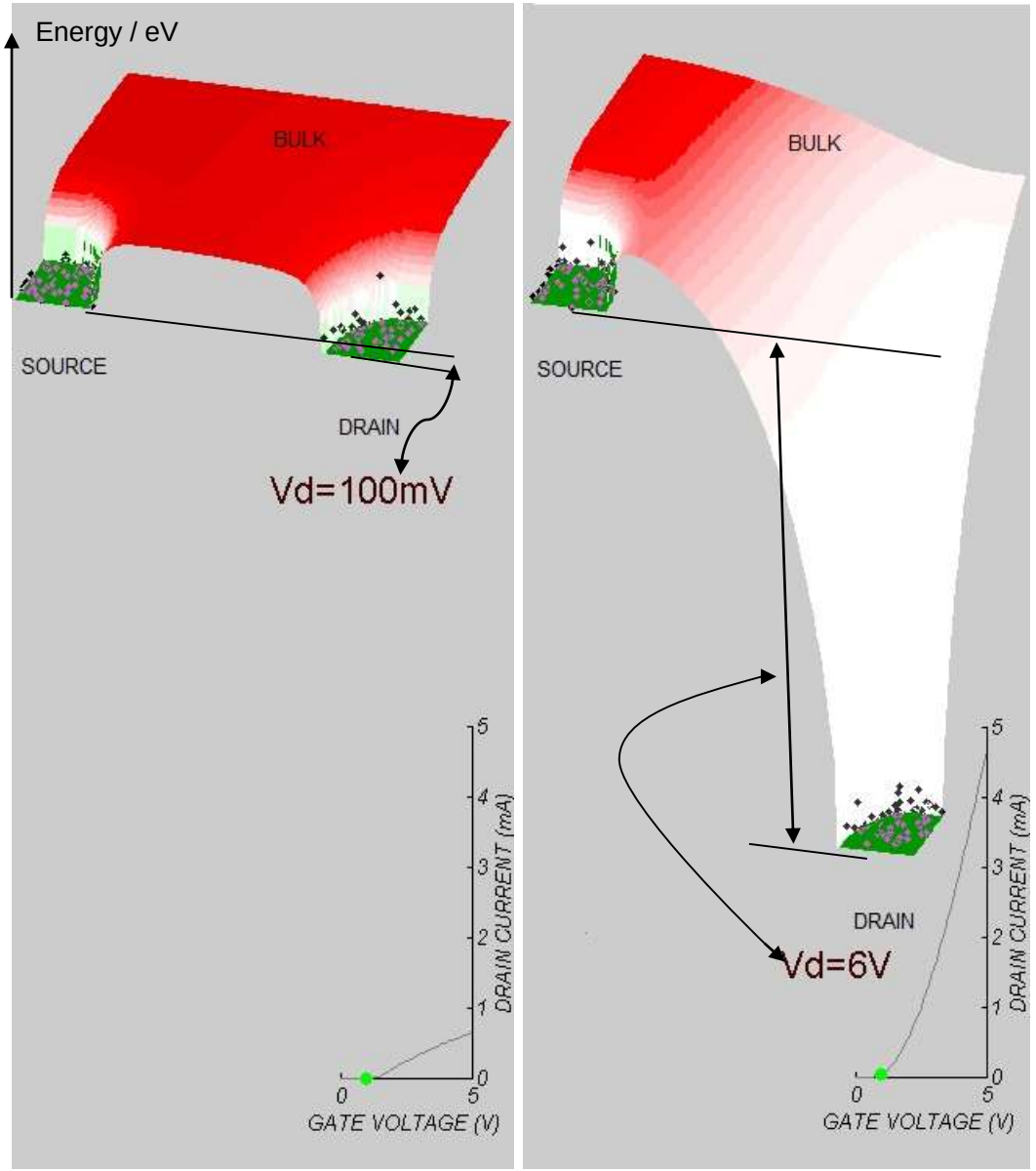


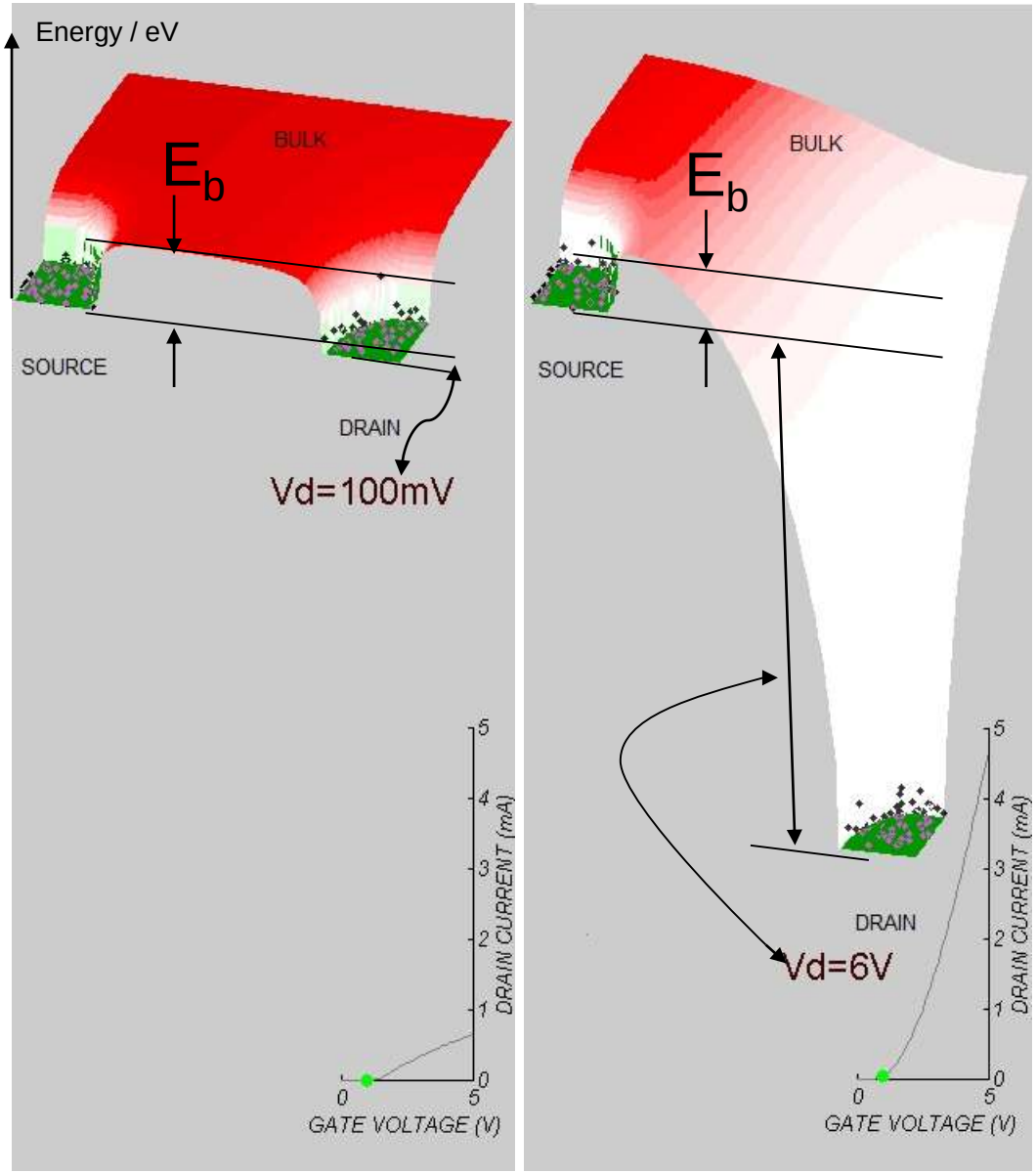
- Electrons have to overcome potential barrier to enter the channel
- Ideal: Potential barrier is only controlled by gate voltage

Taken from F. Sill Micro transductors 08

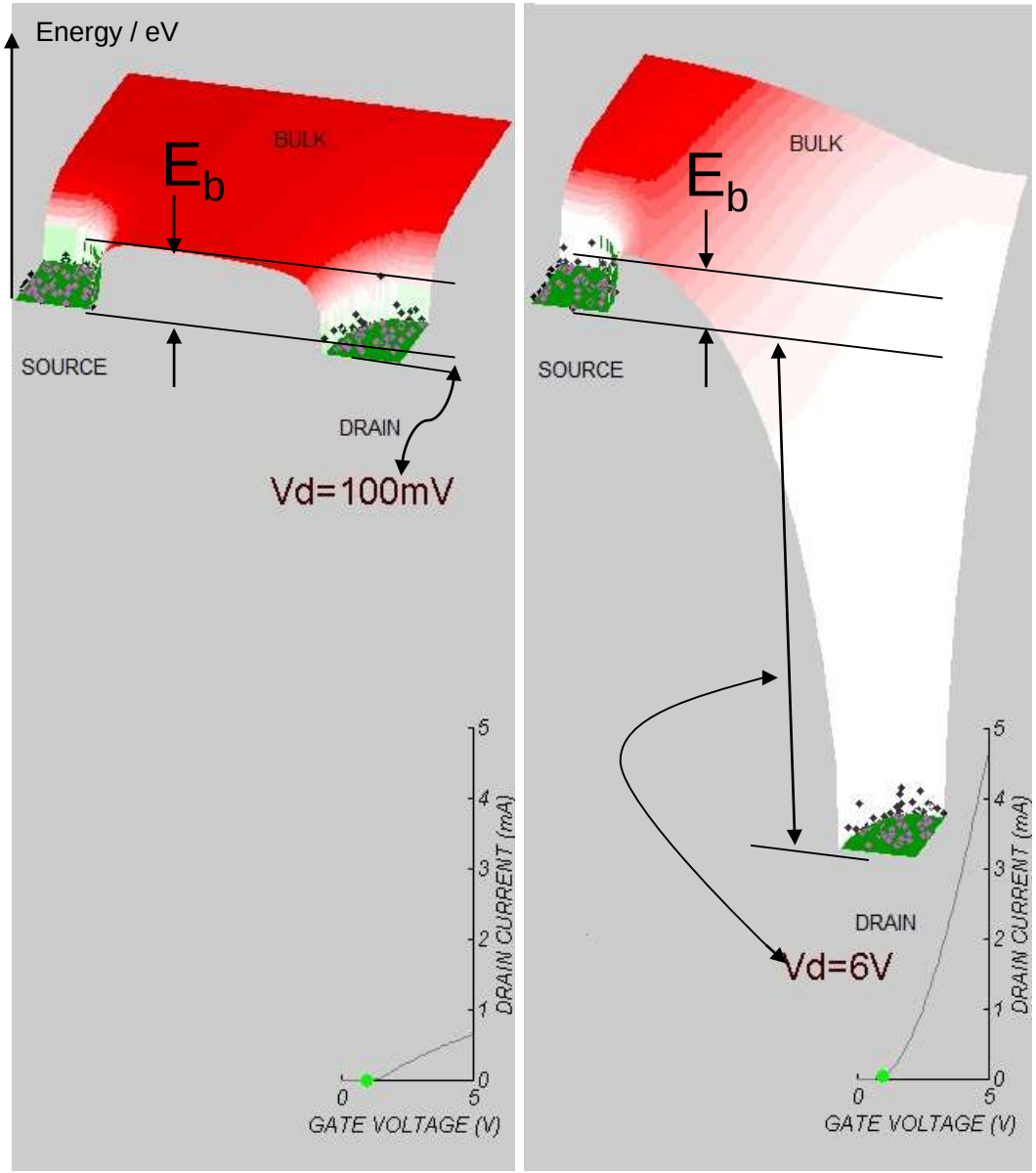

Energy / eV
BULK
SOURCE
DRAIN
Vd=100mV
DRAIN CURRENT (mA)
GATE VOLTAGE (V)
0
1
2
3
4
5


BULK
SOURCE
DRAIN
Vd=6V
DRAIN CURRENT (mA)
GATE VOLTAGE (V)
0
1
2
3
4
5

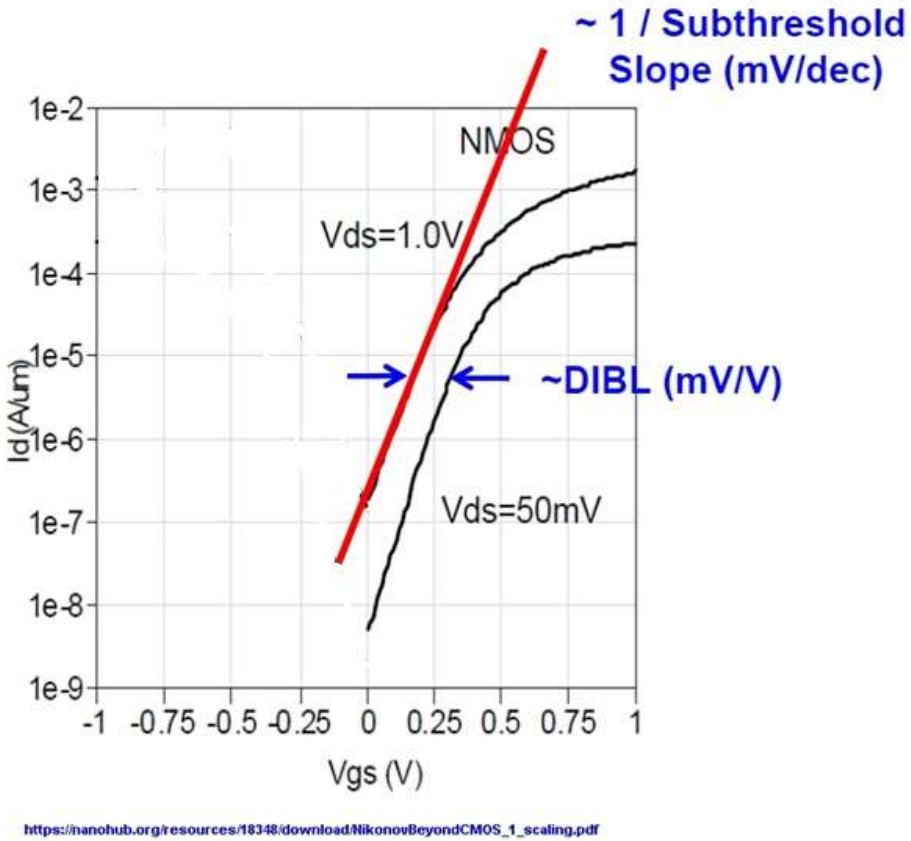

Energy / eV
BULK
SOURCE
DRAIN
Vd=100mV
DRAIN CURRENT (mA)
GATE VOLTAGE (V)
BULK
SOURCE
DRAIN
Vd=6V
DRAIN CURRENT (mA)
GATE VOLTAGE (V)


Energy / eV
BULK
E_b
SOURCE
DRAIN
Vd=100mV
DRAIN CURRENT (mA)
GATE VOLTAGE (V)
BULK
E_b
SOURCE
DRAIN
Vd=6V
DRAIN CURRENT (mA)
GATE VOLTAGE (V)

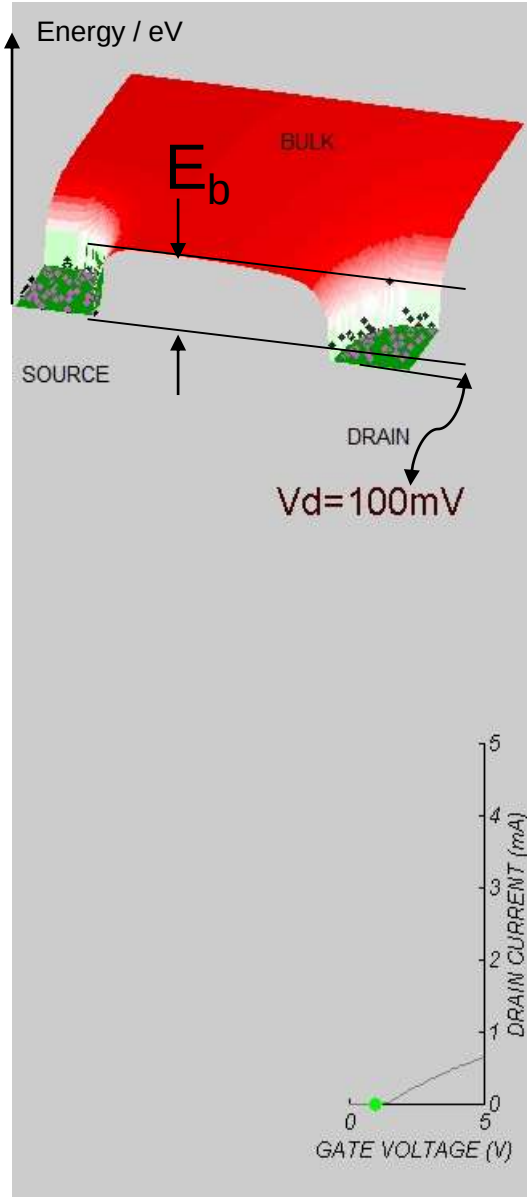
Drain induced barrier lowering: DIBL

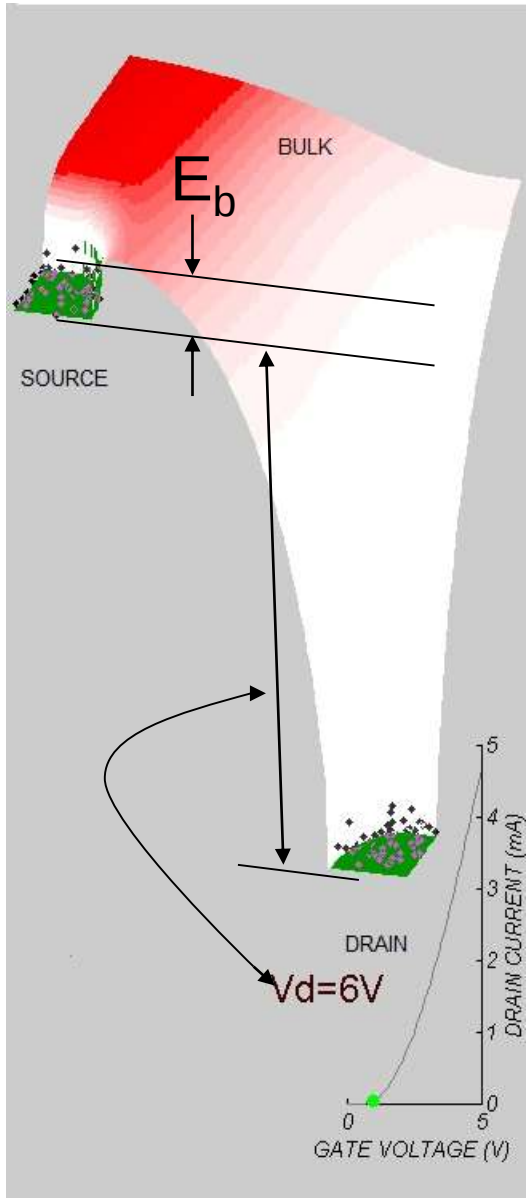


Drain induced barrier lowering: DIBL

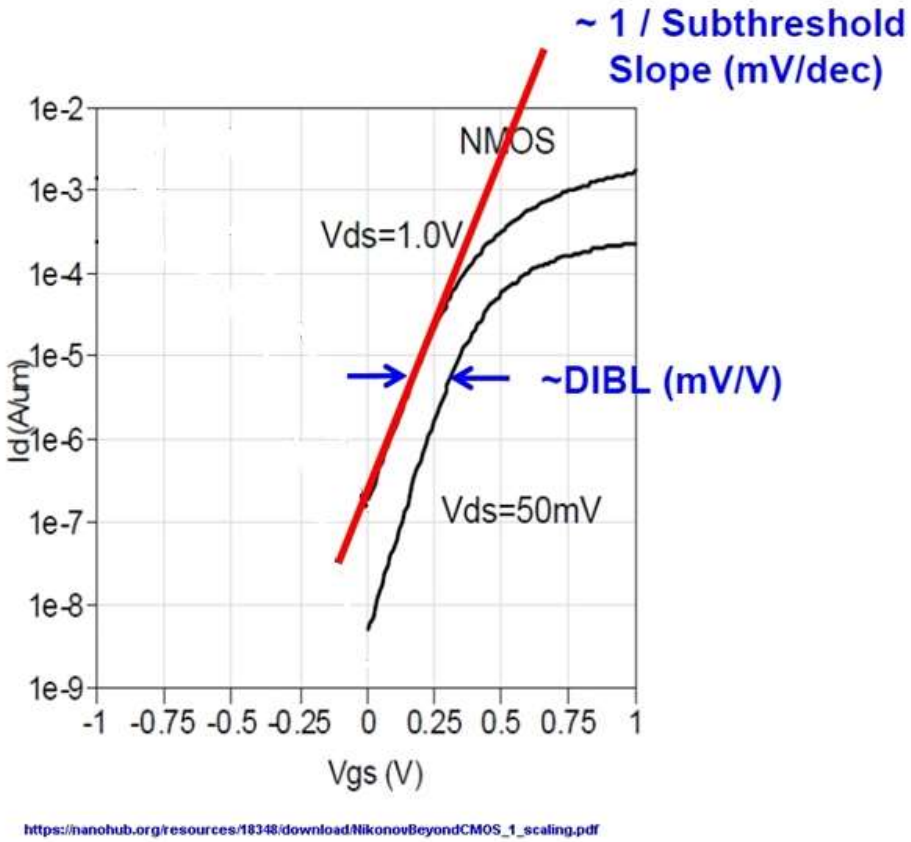


https://nanohub.org/resources/18348/download/NikonovBeyondCMOS_1_scaling.pdf

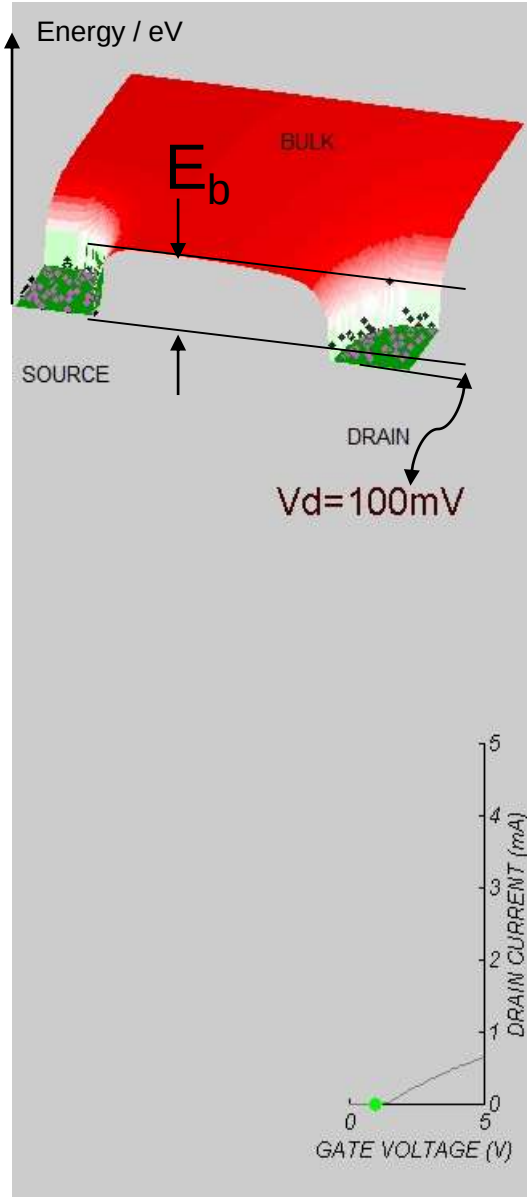


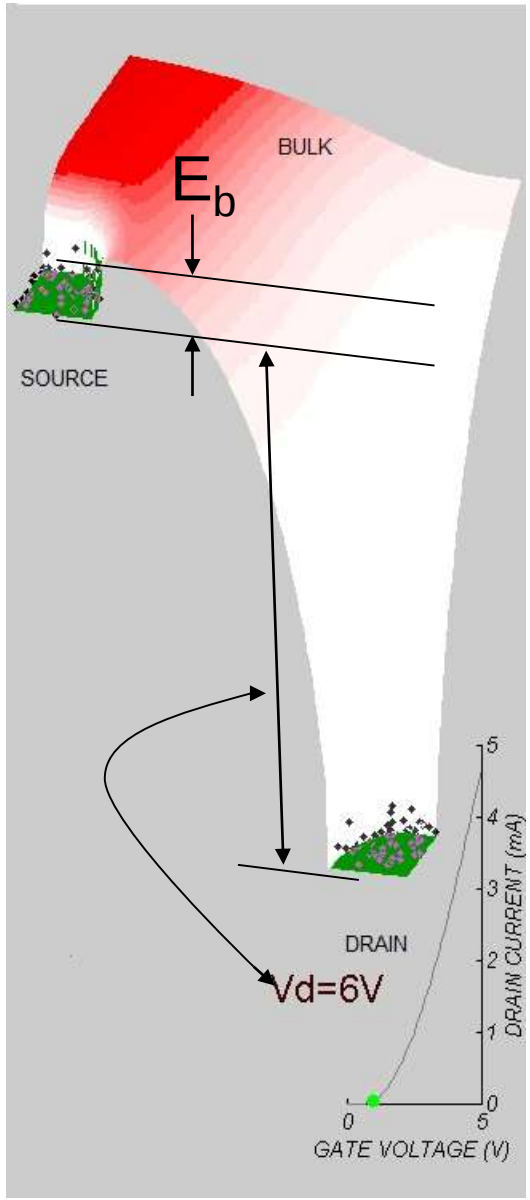


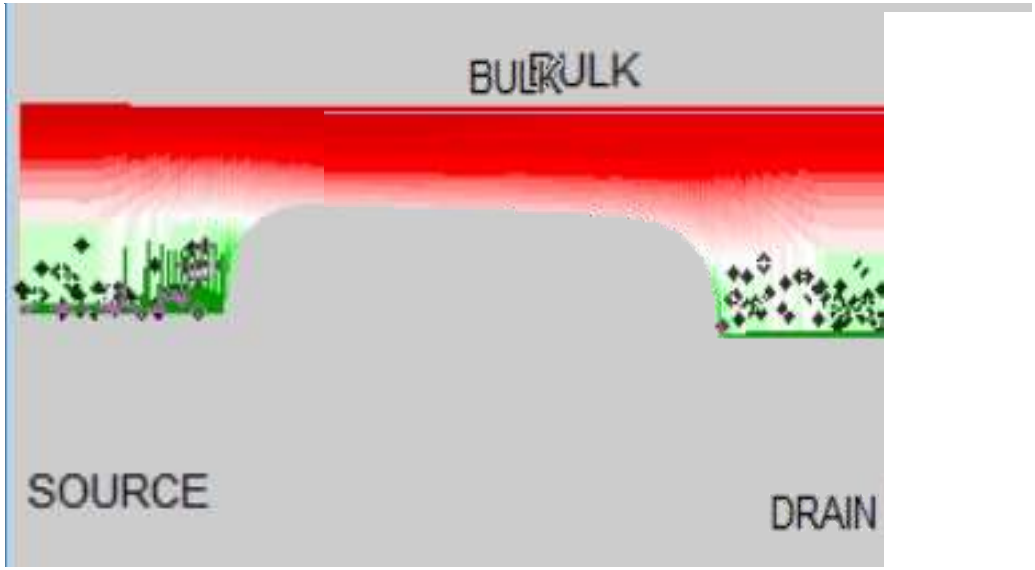
Drain induced barrier lowering: DIBL

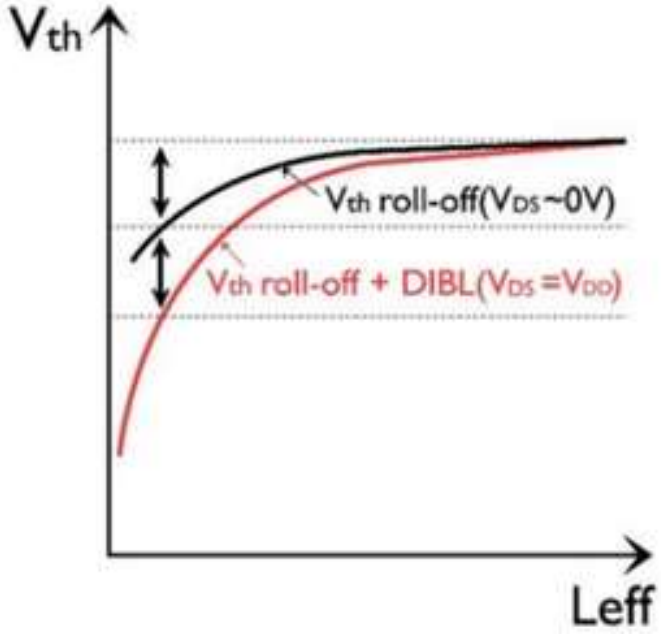


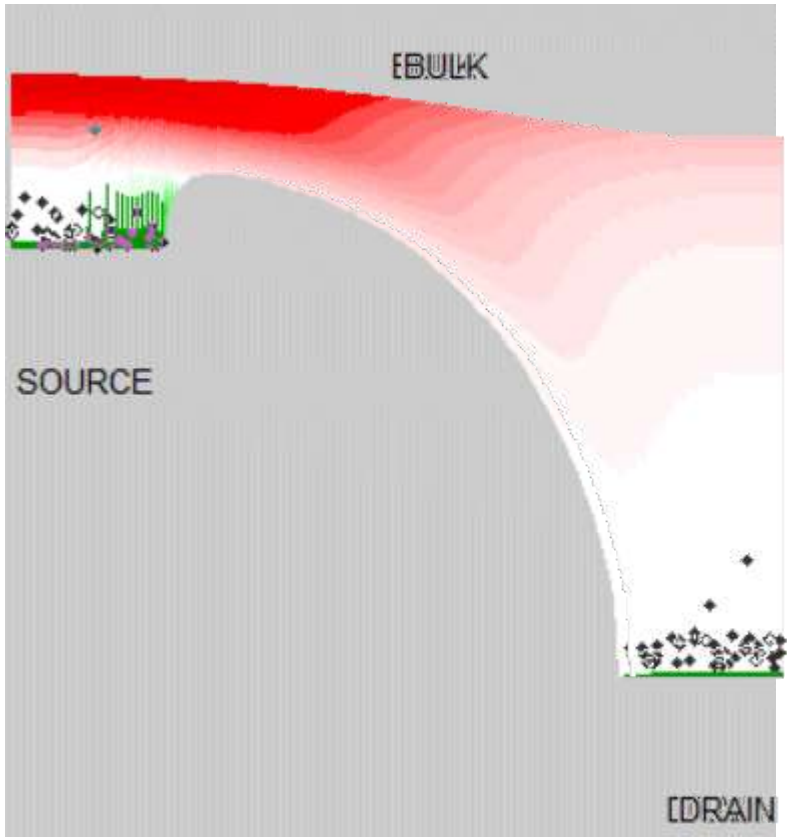
Unit for DIBL: mV/V

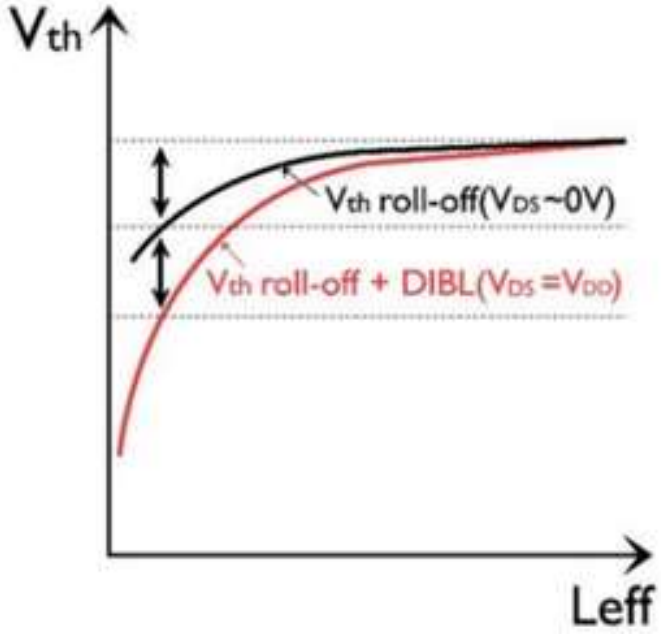


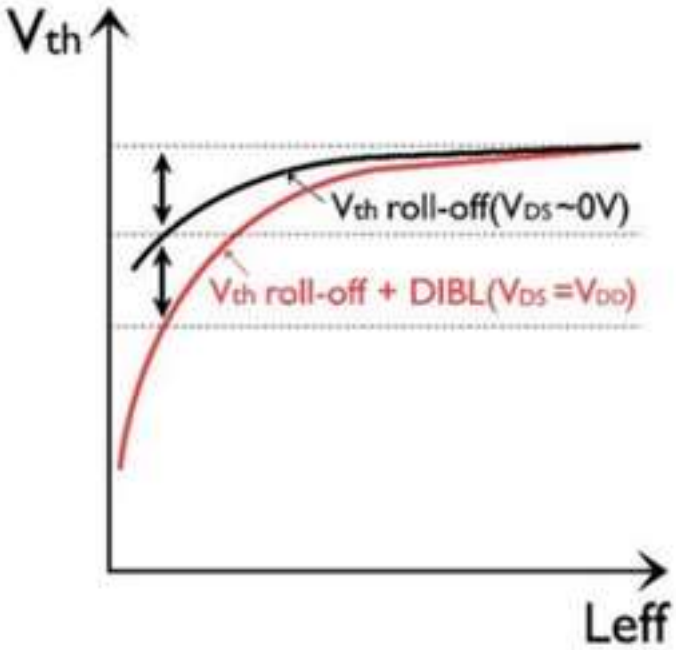


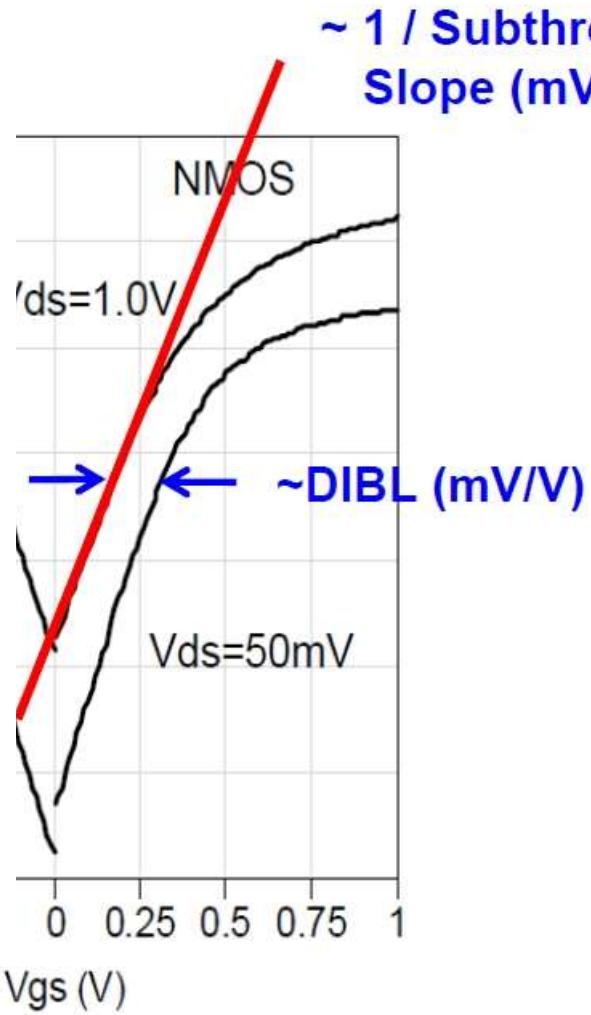

BULK
SOURCE
DRAIN


Vth
Vth roll-off(VDS~0V)
Vth roll-off + DIBL(VDS=VDD)
Leff

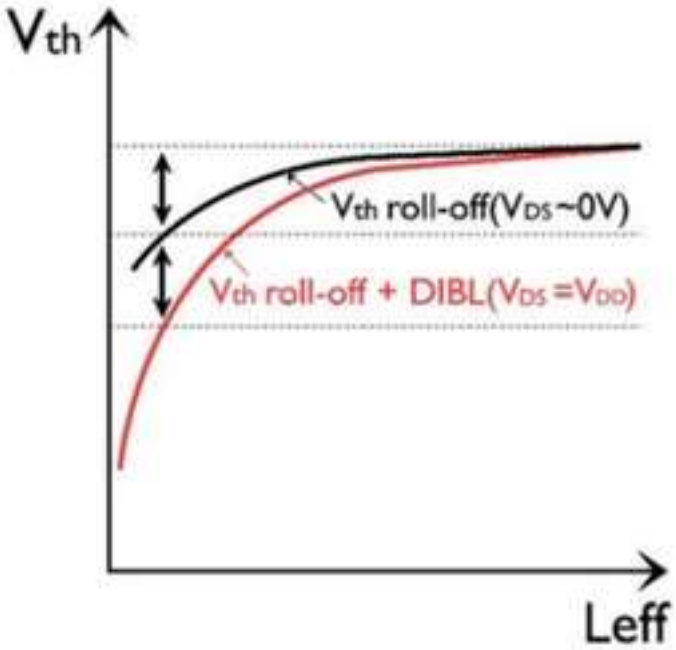

BULK
SOURCE
DRAIN

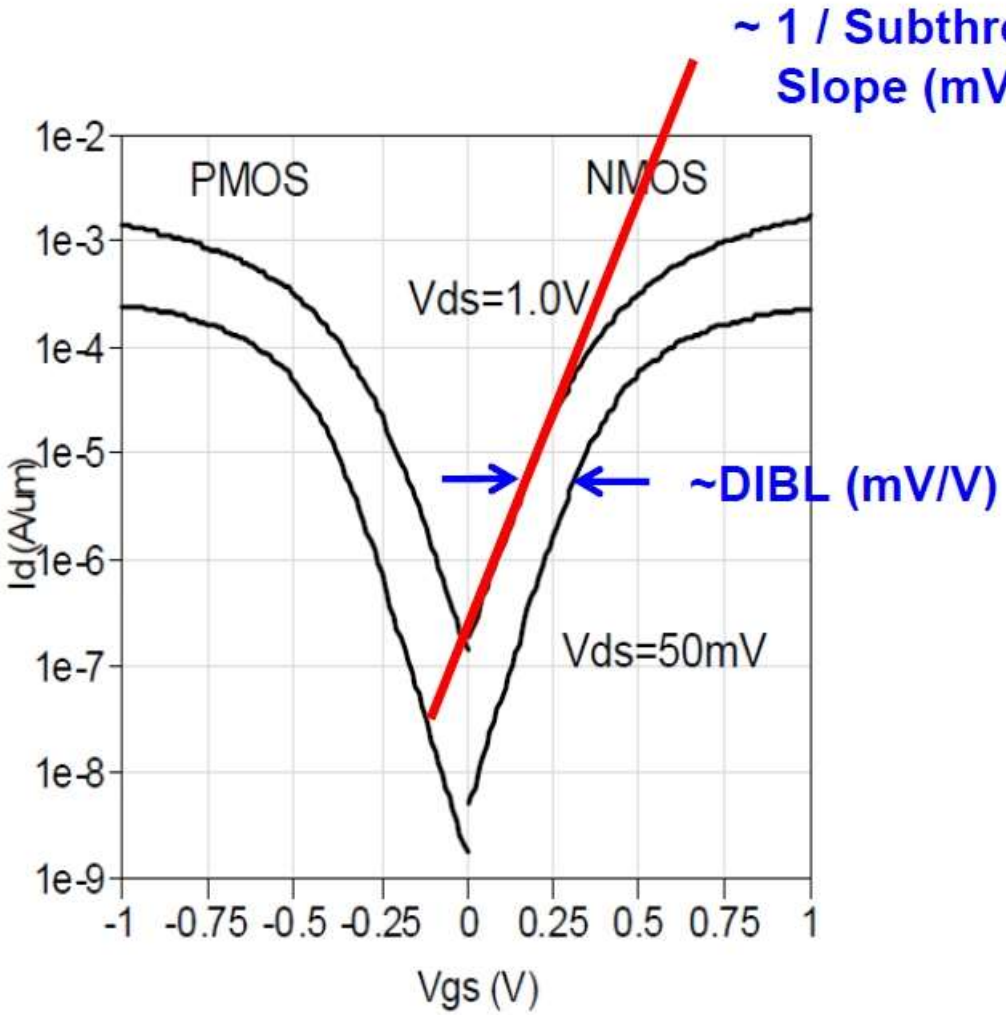

Vth
Vth roll-off(VDS~0V)
Vth roll-off + DIBL(VDS=VDD)
Leff





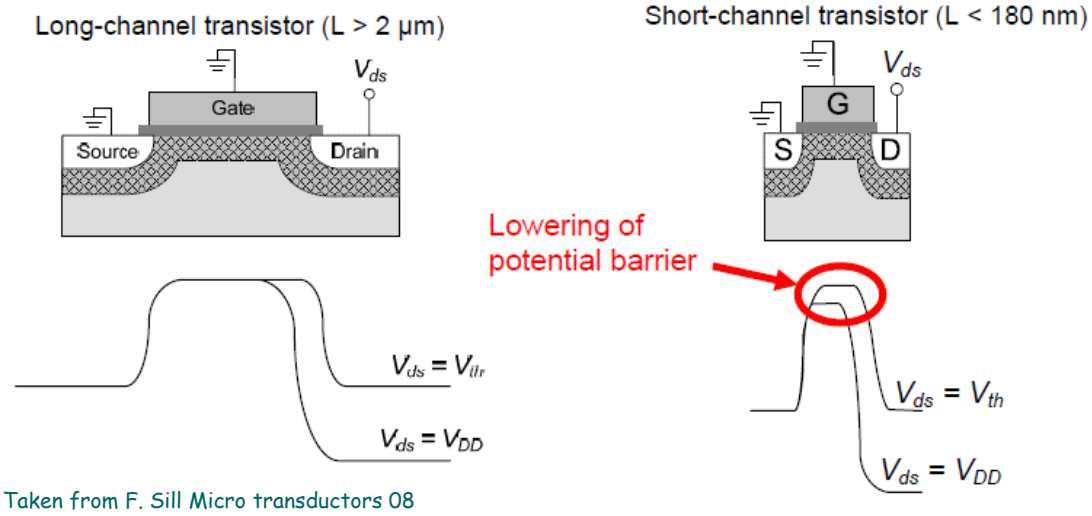
https://nanohub.org/resources/18348/download/NikonovBeyondCMOS_1_scaling.pdf



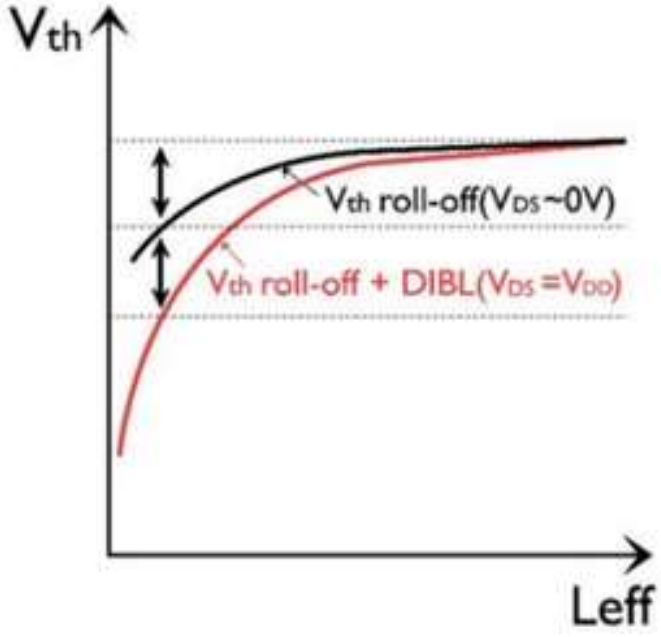


https://nanohub.org/resources/18348/download/NikonovBeyondCMOS_1_scaling.pdf

Short channel effects:
Drain induced barrier lowering DIBL and roll-off

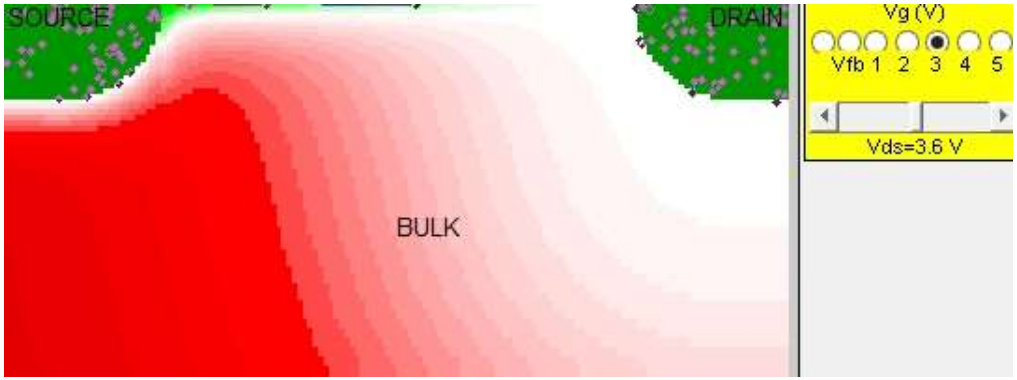


Taken from F. Sill Micro transductors 08

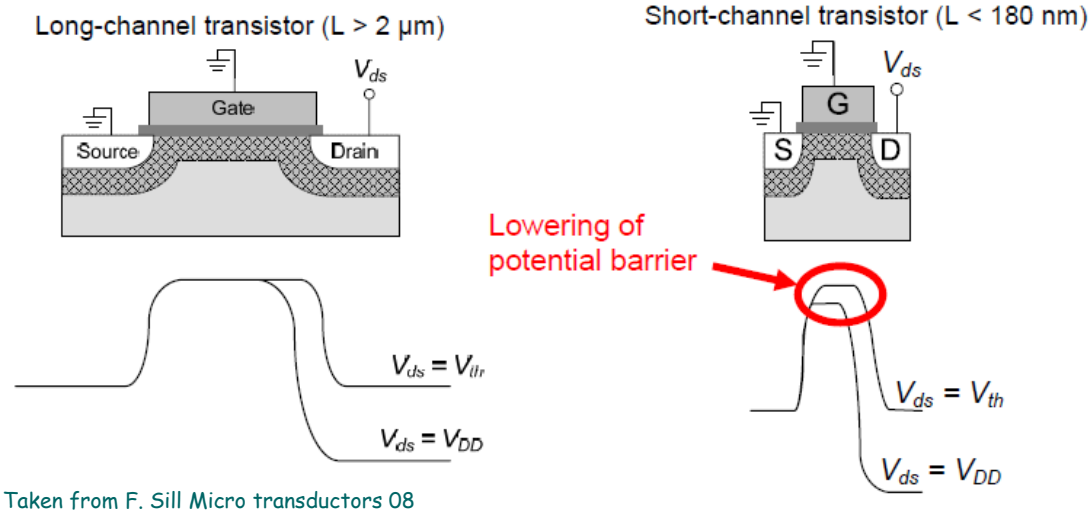


- At short channel transistors potential barrier is also affected by drain voltage

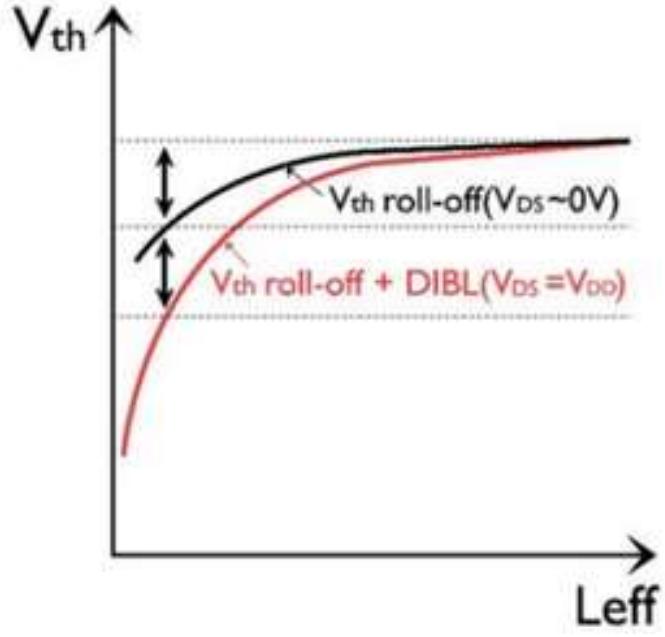
➔ If $V_{ds} = V_{DD}$ Transistors can start to conduct even if $V_{gs} < V_{th}$



Short channel effects:
Drain induced barrier lowering DIBL and roll-off

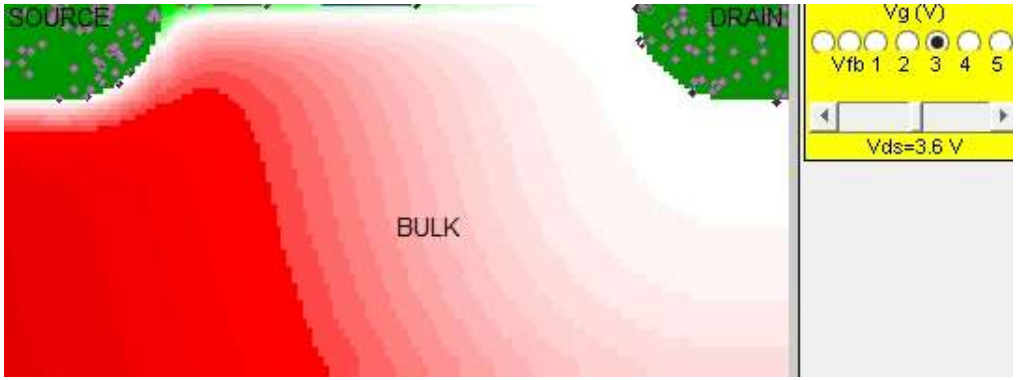


Taken from F. Sill Micro transductors 08



- At short channel transistors potential barrier is also affected by drain voltage

➔ If $V_{ds} = V_{DD}$ Transistors can start to conduct even if $V_{gs} < V_{th}$

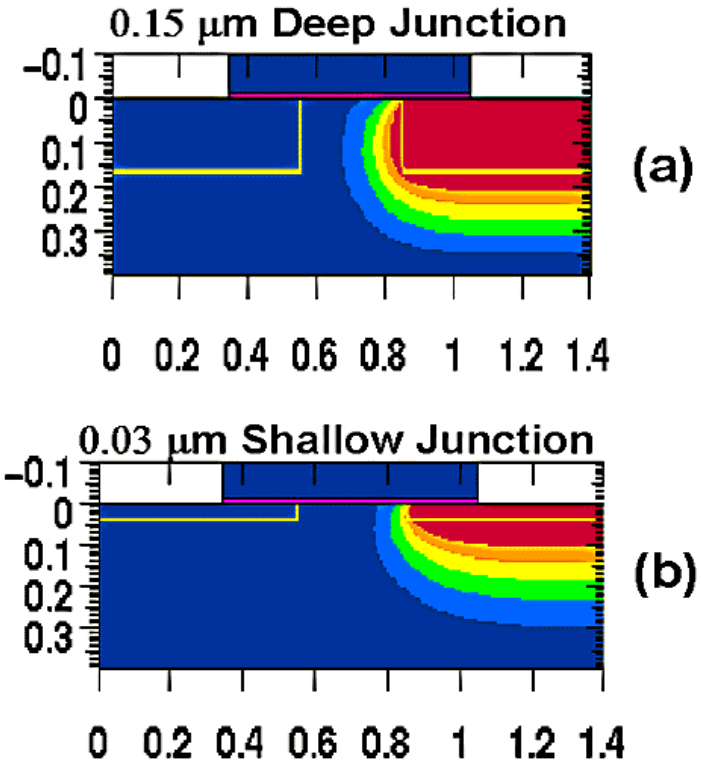


=>

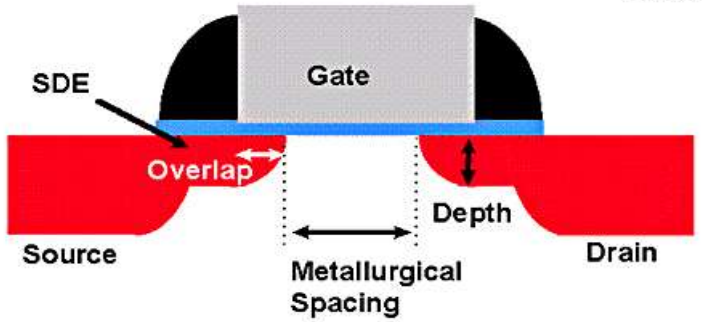
Keep the dimension of the space charge around the drain in the body as short as possible!

Short channel effects:
Action 1: Shallow junction

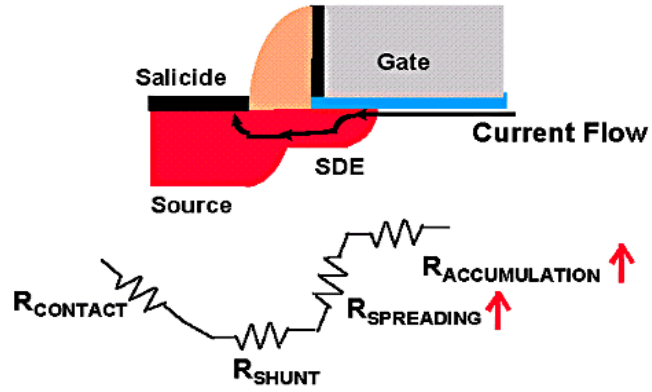
Intel TJ Q3'98



Intel TJ Q3'98



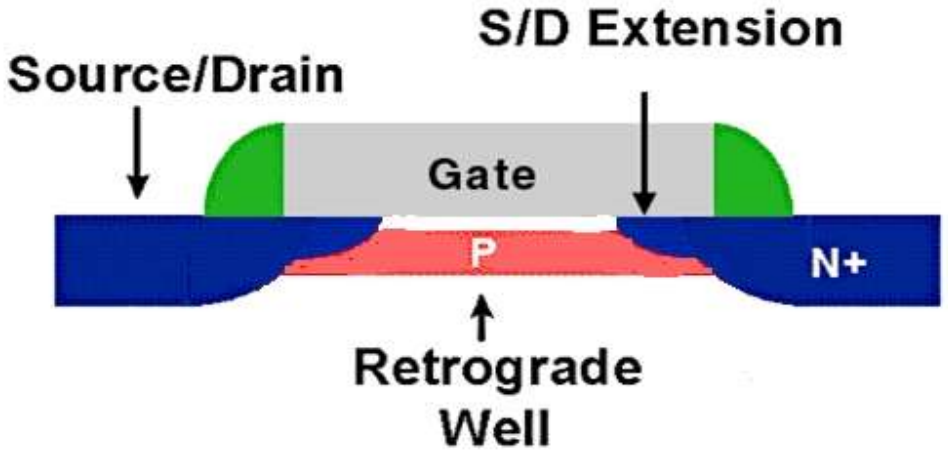
Intel TJ Q3'98



External resistance

Short channel effects:

Action 2: Retrograde doping of a sub 0.18 µm MOSFET

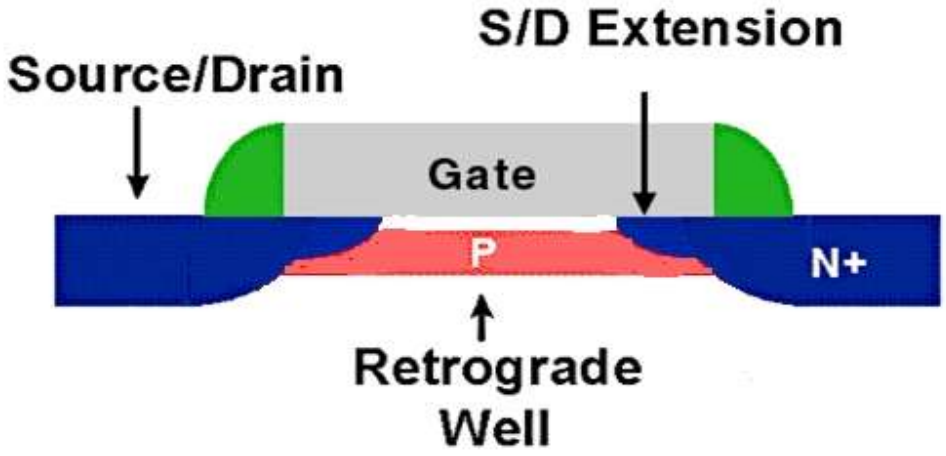


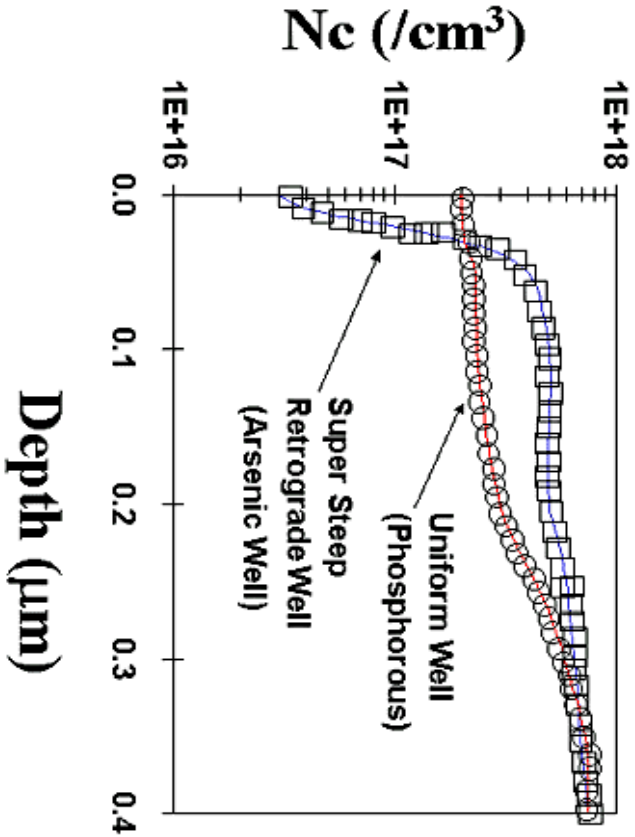
Required are Super Steep Doping Profiles to confine the cannel and drain depletion zones

- Accuracy of Implantation
- Advanced Healing and Activation

Short channel effects:

Action 2: Retrograde doping of a sub 0.18 µm MOSFET





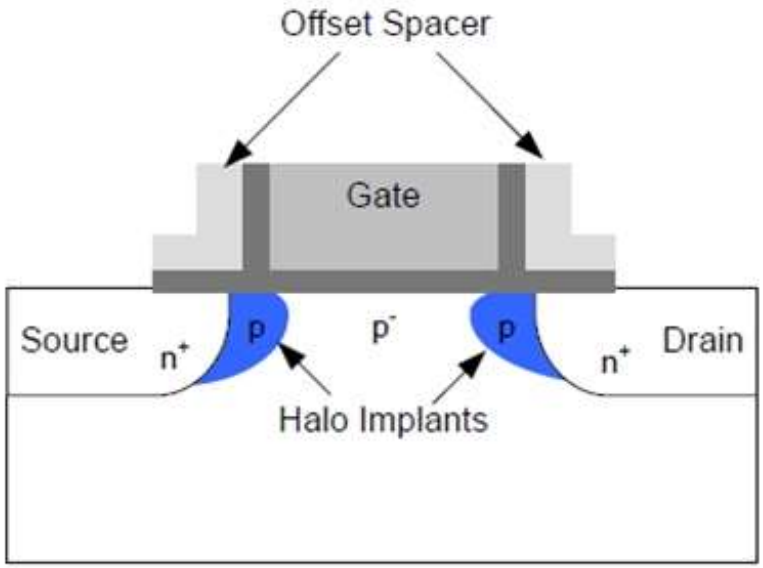
Required are Super Steep Doping Profiles to confine the cannel and drain depletion zones

- Accuracy of Implantation
- Advanced Healing and Activation

Short channel effects:
Action 3: Halo Implant

- Halo Implants
  - High doped regions near source and drain areas
  - → Reduced Drain Induced Barrier Lowering

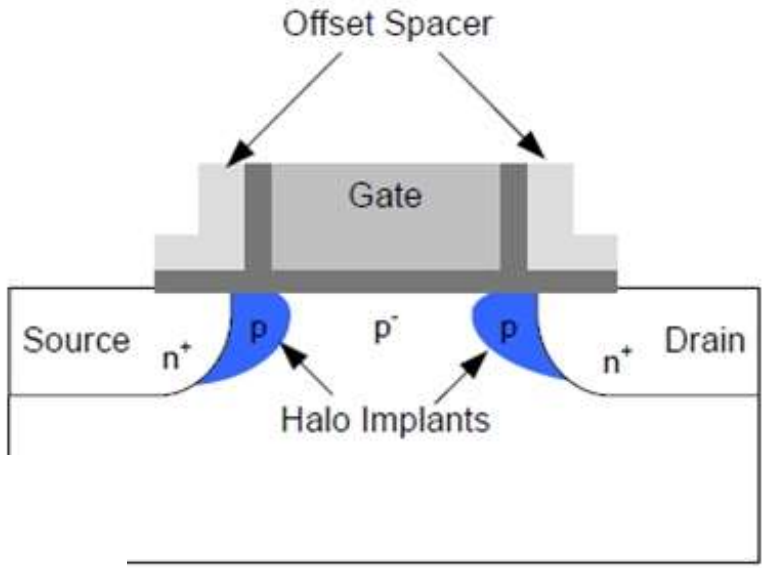
Taken from F. Sill Micro transductors 08

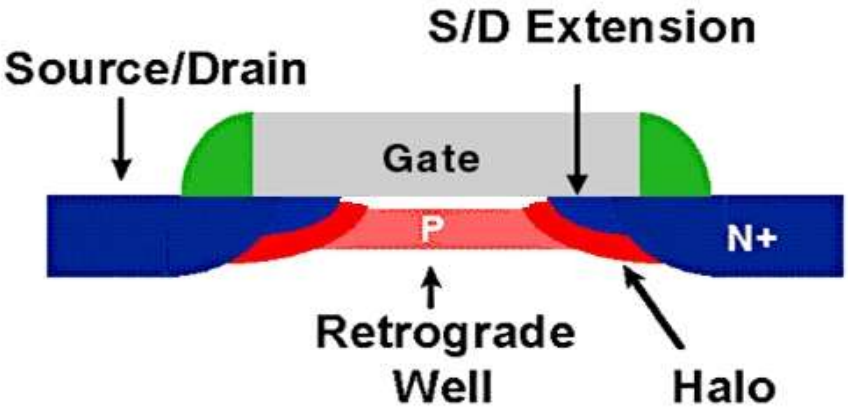


Short channel effects:
Action 3: Halo Implant

- Halo Implants
  - High doped regions near source and drain areas
  - → Reduced Drain Induced Barrier Lowering

Taken from F. Sill Micro transductors 08





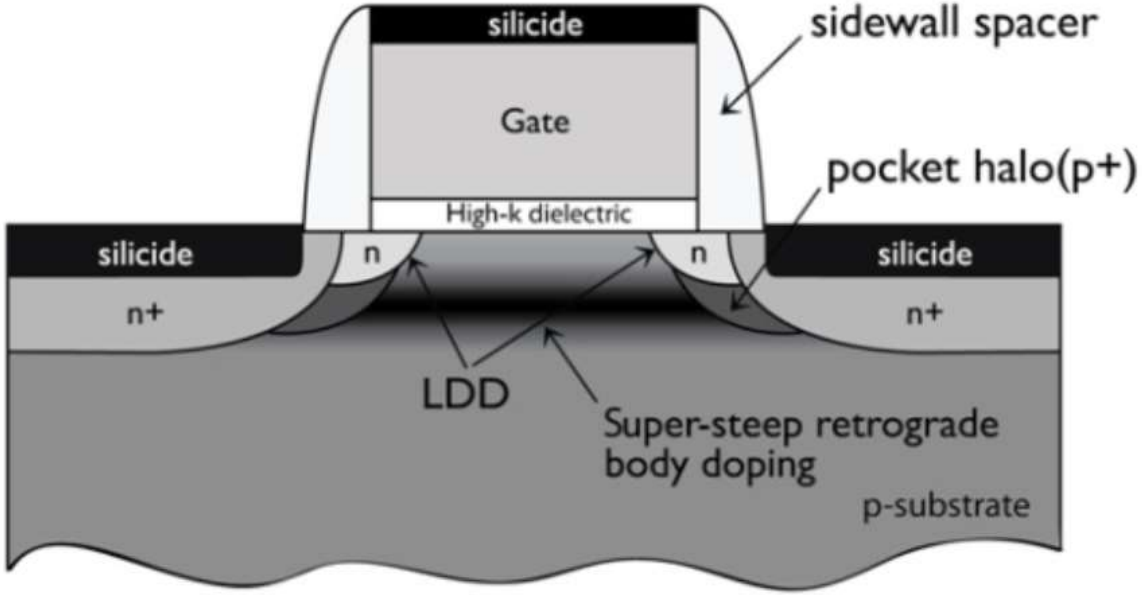


Fig. 5. Cross-section of an advanced MOSFET.

TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 11, No. 3, pp. 93-105, June 25, 2010

Invited Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: 10.4313/TEEM.2010.11.3.093

Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics

Yong-Bin Kim†
Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115, USA

Received April 26, 2010; Accepted May 3, 2010

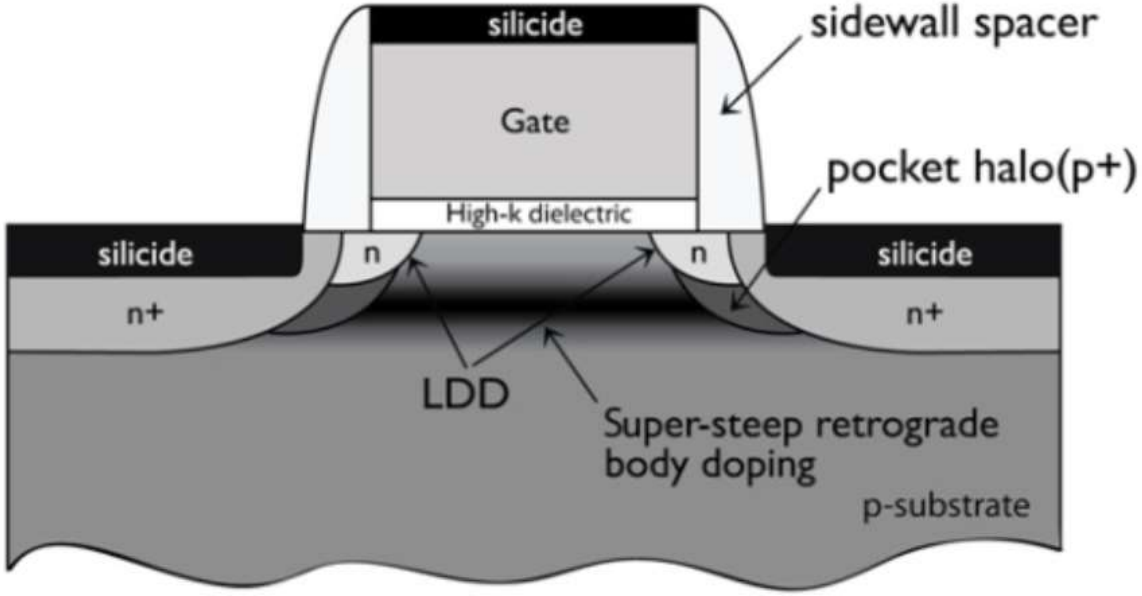


Fig. 5. Cross-section of an advanced MOSFET.

Confinement of the space charge by Retrograde Well plus Halo

TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 11, No. 3, pp. 93-105, June 25, 2010

Invited Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: 10.4313/TEEM.2010.11.3.093

Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics

Yong-Bin Kim†
Department of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115, USA

Received April 26, 2010; Accepted May 3, 2010

Ultimate Solution: FDSOI see next!

Technology approach: SOI

Continue "SCT_SS20_13.03" 30:45

VIDEO CAMPUS SACHSEN

SOI = Silicon on insulator

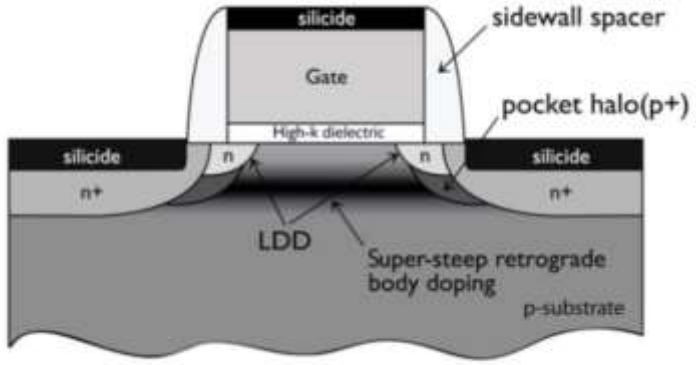
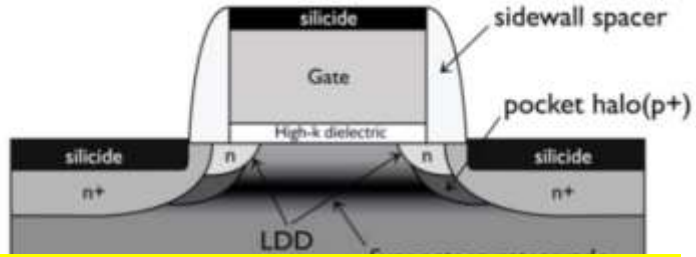


Fig. 5. Cross-section of an advanced MOSFET.

Technology approach: SOI

Continue "SCT_SS20_13.03" 30:45

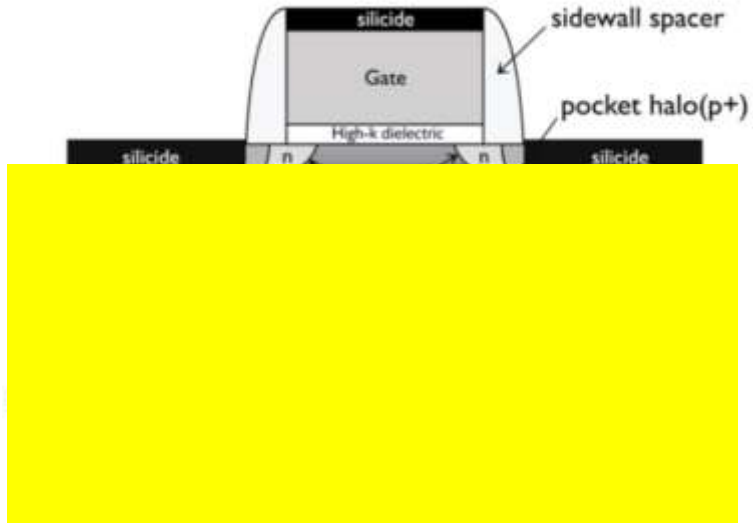
SOI = Silicon on insulator



Technology approach: SOI

Continue "SCT_SS20_13.03" 30:45

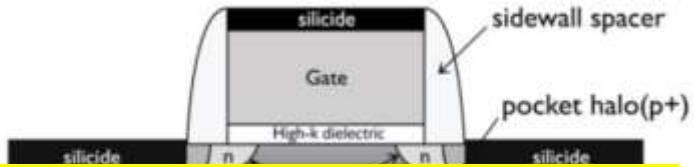
SOI = Silicon on insulator

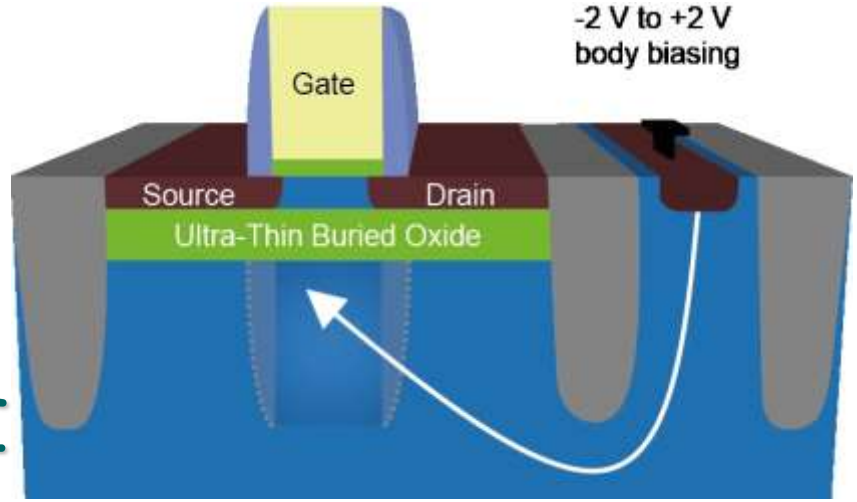


Technology approach: SOI

Continue
"SCT_SS20_13.03" 30:45

SOI = Silicon on insulator





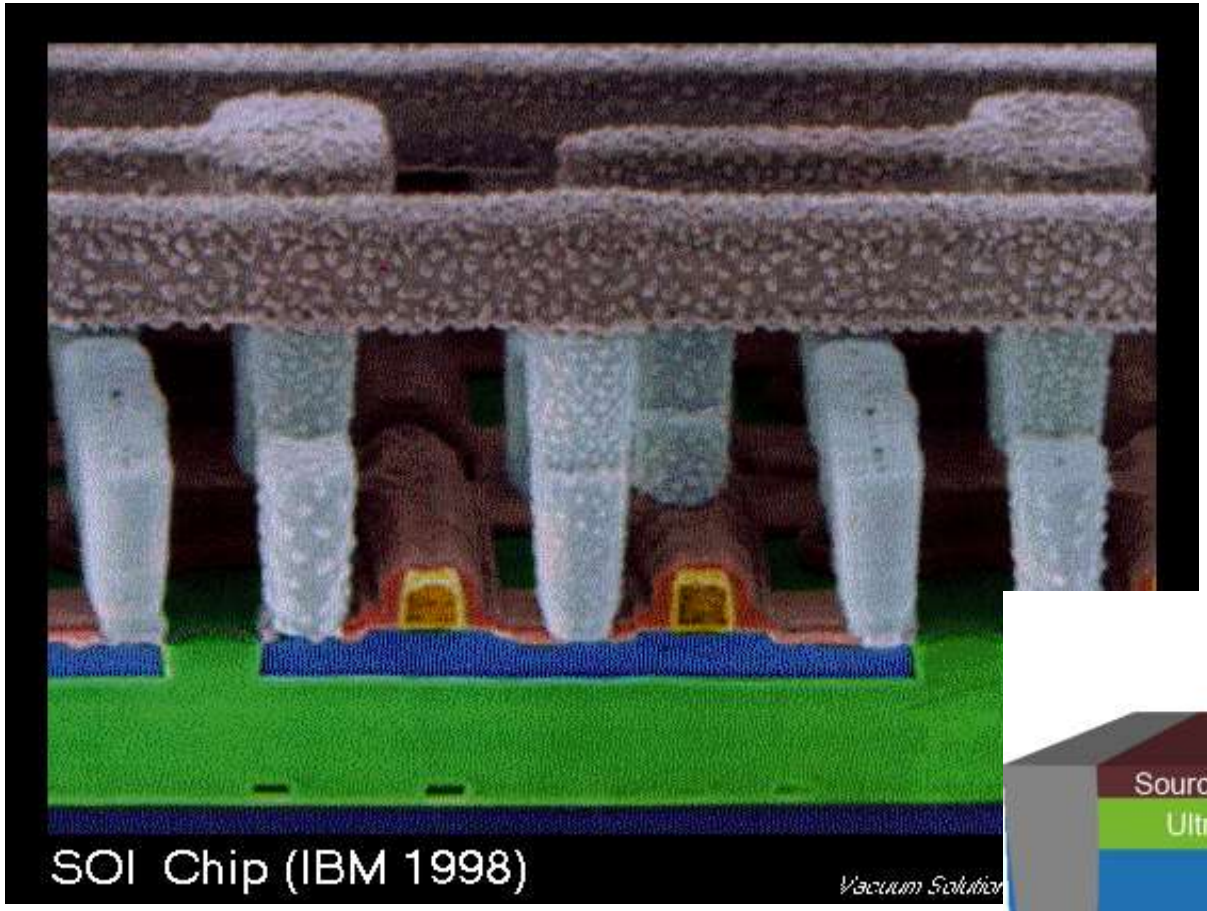
FDSOI

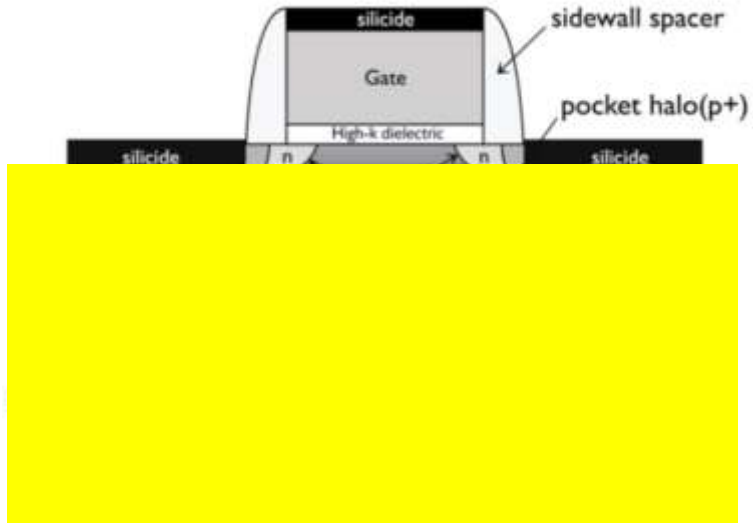
Technology approach: SOI

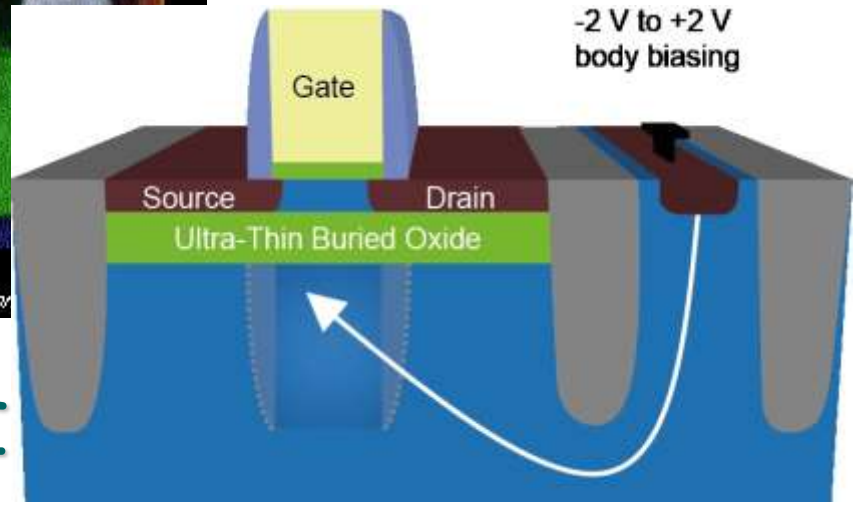
Continue "SCT_SS20_13.03" 30:45

VIDEO CAMPUS SACHSEN

SOI = Silicon on insulator

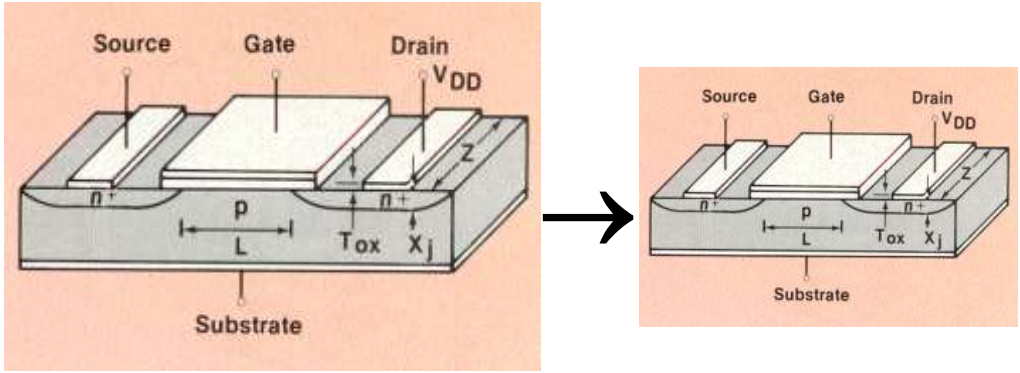






FDSOI

Gate dielectric and leakage



Robert H. Dennard, IBM 1974

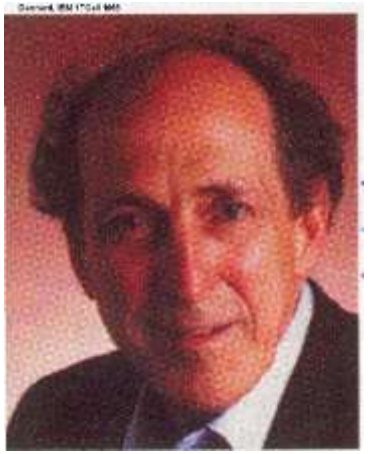
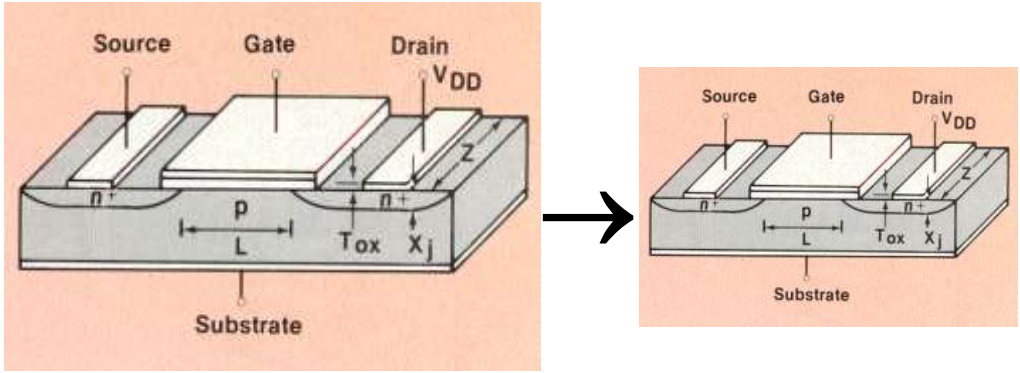


Table II—Scaling Factor

Scaling Factor	$S>1$
Lateral Dimensions	$L \rightarrow L/S$ $Z \rightarrow Z/S$
Vertical Dimensions	$T_{OX} \rightarrow T_{OX}/S$ $X_j \rightarrow X_j/S$
Supply Voltage	$V_{DD} \rightarrow V_{DD}/S$
Substrate Doping Concentration	$N_A \rightarrow SN_A$

Gate dielectric and leakage



Robert H. Dennard, IBM 1974

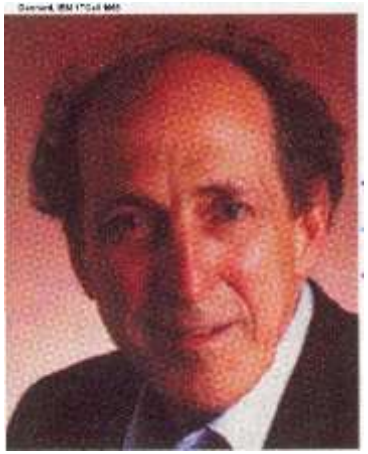


Table II—Scaling Factor

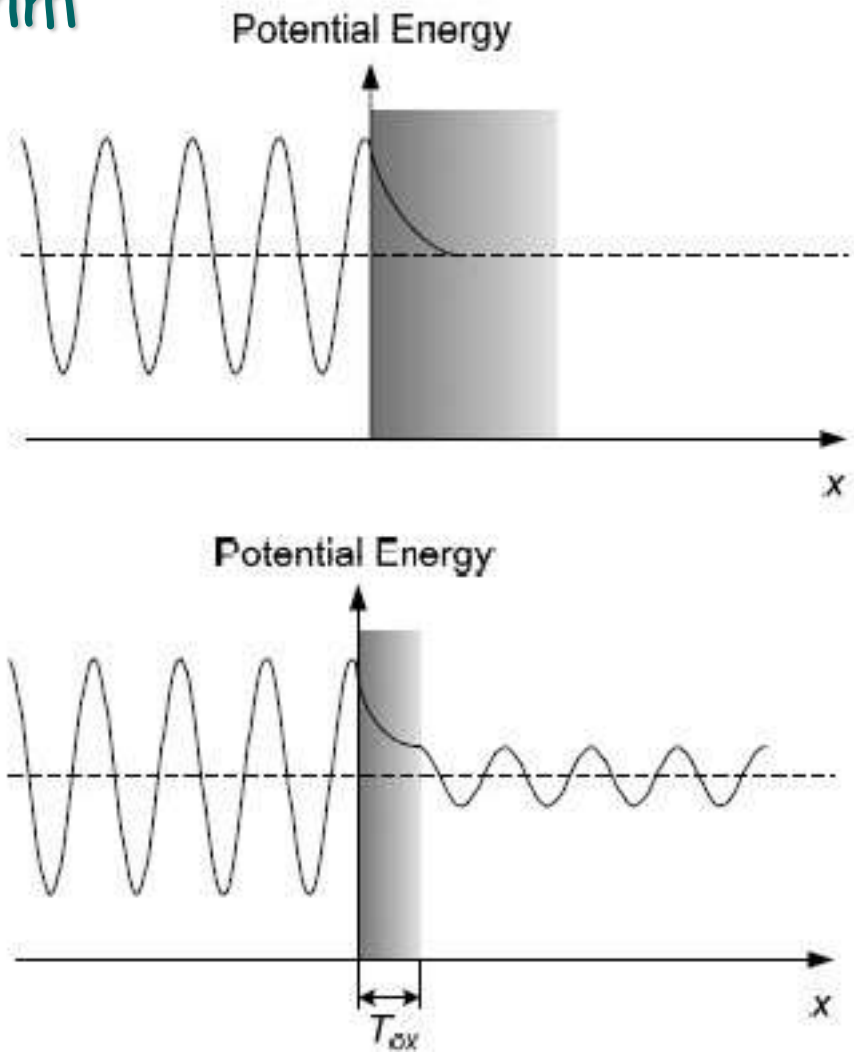
Scaling Factor	$S > 1$
Lateral Dimensions	$L \rightarrow L/S$
	$Z \rightarrow Z/S$
Vertical Dimensions	$T_{OX} \rightarrow T_{OX}/S$
	$X_j \rightarrow X_j/S$
Supply Voltage	$V_{DD} \rightarrow V_{DD}/S$
Substrate Doping Concentration	$N_A \rightarrow SN_A$

Result of scaling: Tunnel Current

Significant when d_{ox} <~ 2-3 nm

The tunnel probability depends strongly on the physical width of the barrier!

How to proceed scaling?!



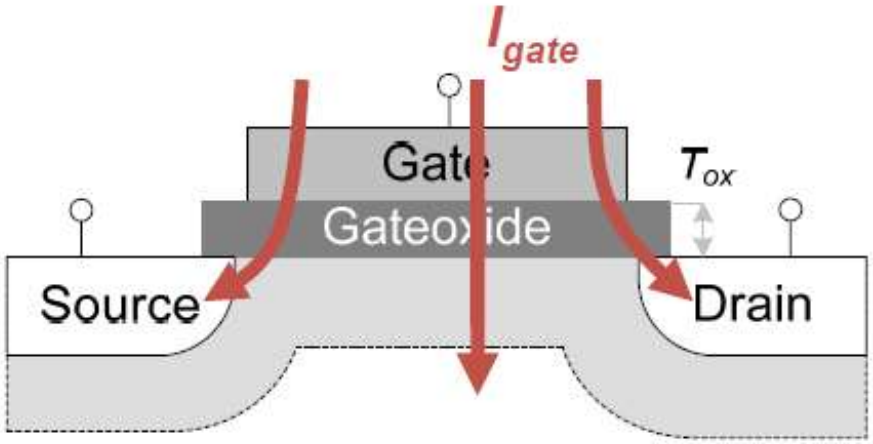
Taken from F. Sill Micro transductors 08

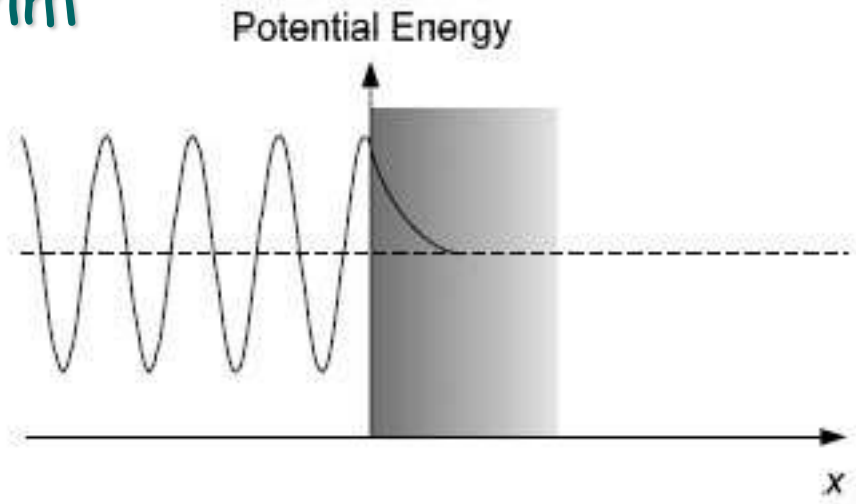
Result of scaling: Tunnel Current

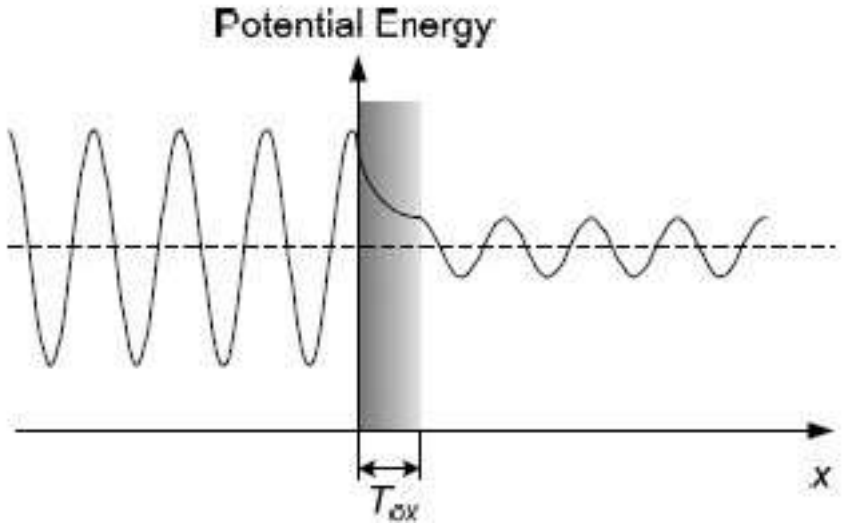
Significant when d_{ox} <~ 2-3 nm

The tunnel probability depends strongly on the physical width of the barrier!

How to proceed scaling?!





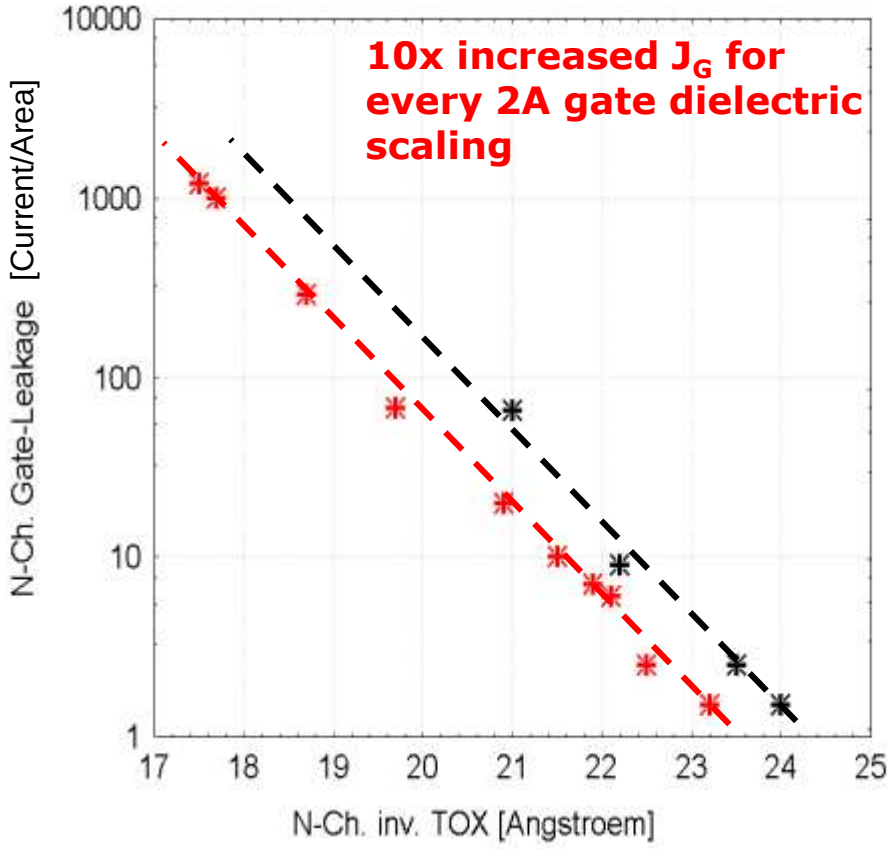


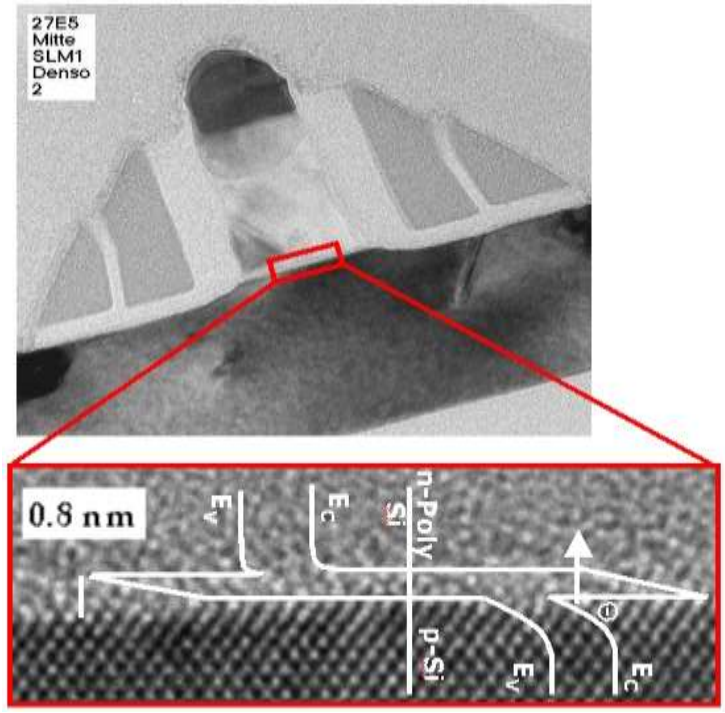
Taken from F. Sill Micro transductors 08

FEOL: Conventional GOX Scaling Limitations

Thinning Gate Oxides lead to an „explosion" of gate leakage

The key is to control Gate oxide leakage (Nitrogen , High k materials)

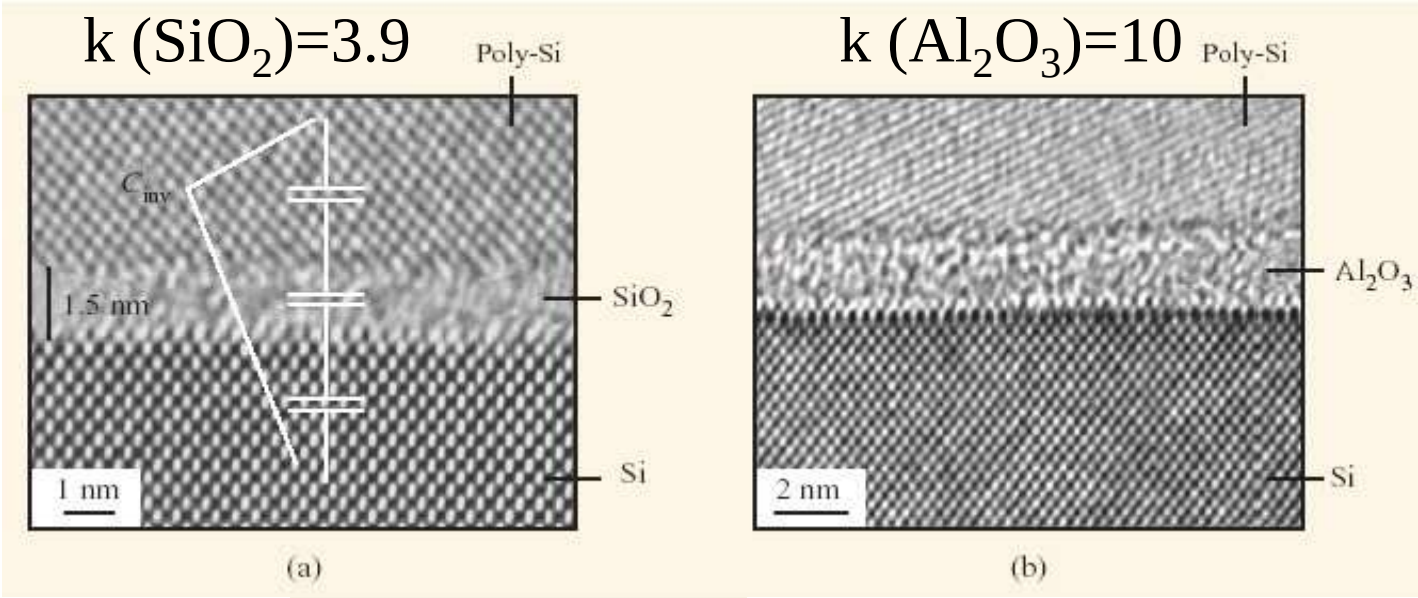




$C=\varepsilon A/d$

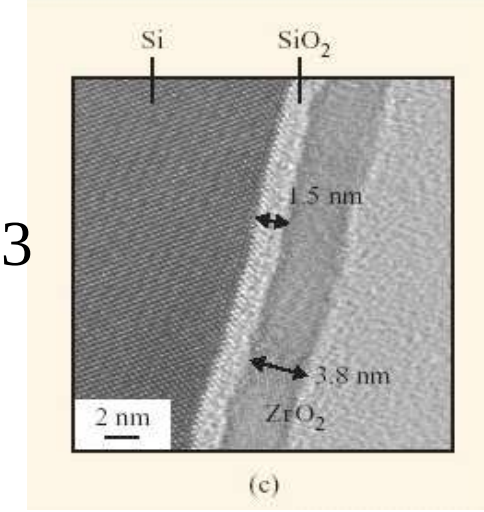
Taken from Horstmann DMA 2008

5.1.2. Material equivalent scaling



$$t_{eq} = \left(\frac{k_{ox}}{k}\right) t_{phys}$$

Source: IBM JRD

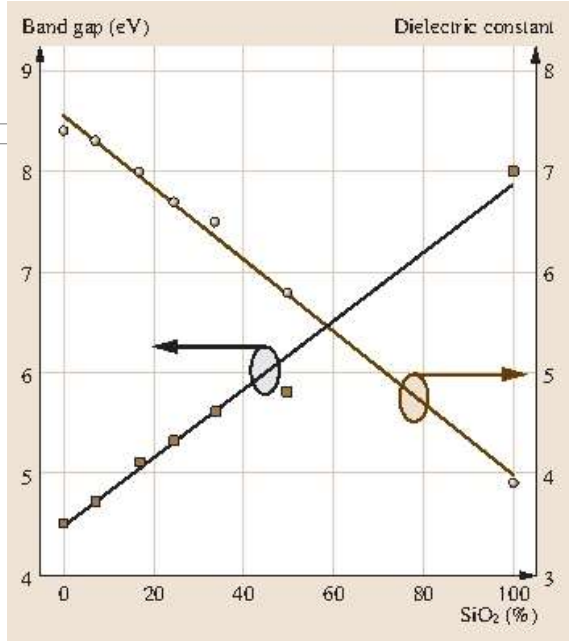


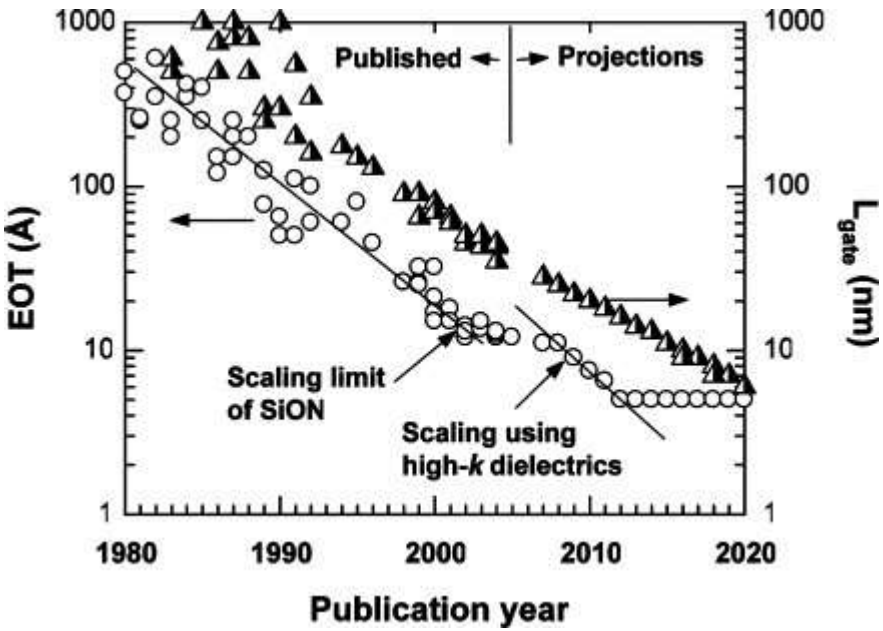
k (ZrO_2)=23

Equivalent Oxide Thickness: EOT

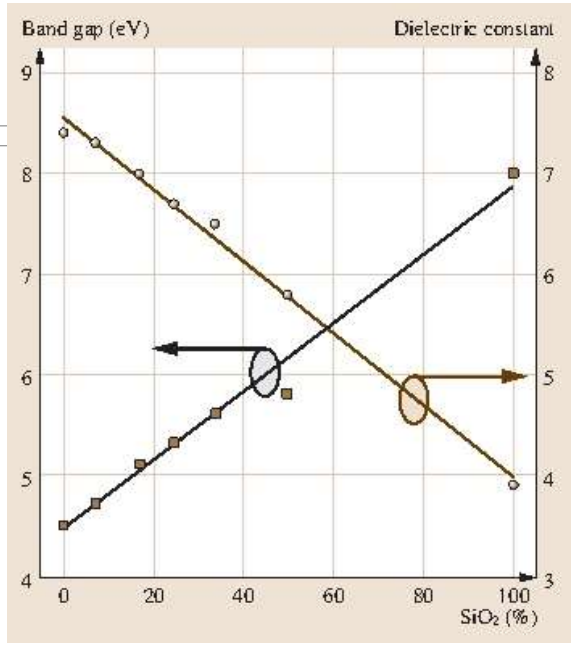
By using a high k dielectric the physical thickness of the dielectric can be thicker without reducing the capacitance!

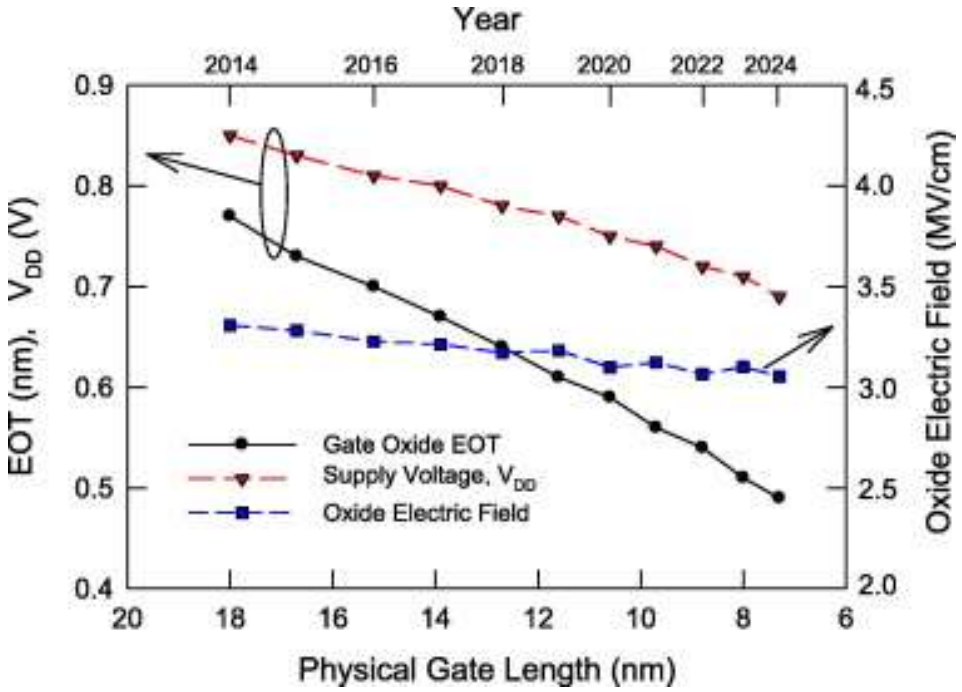
Initial step to raise k was to incorporate Si_3N_4 into the SiO_2 gate ox called SION



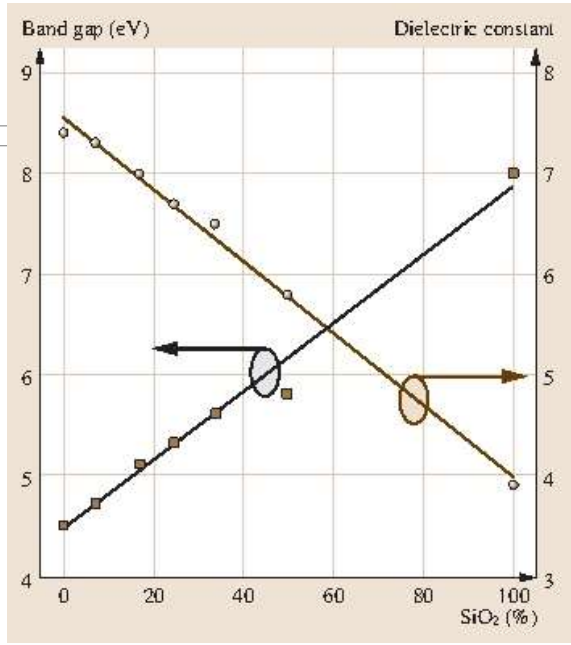


Initial step to raise k was to incorporate Si_3N_4 into the SiO_2 gate ox called SION

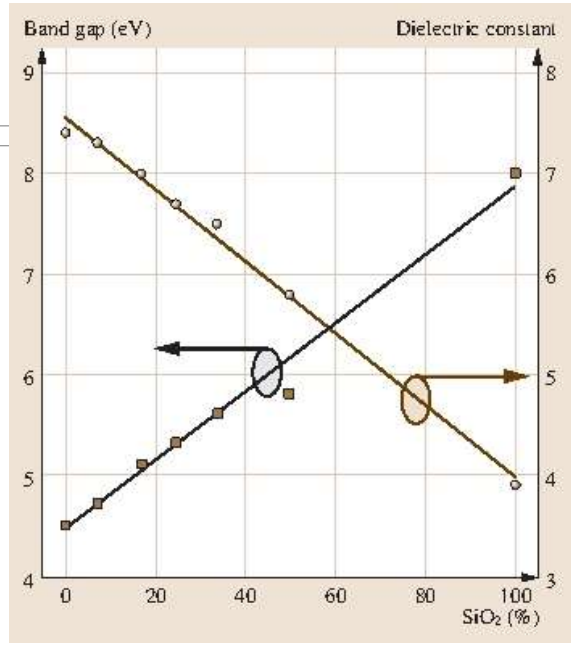


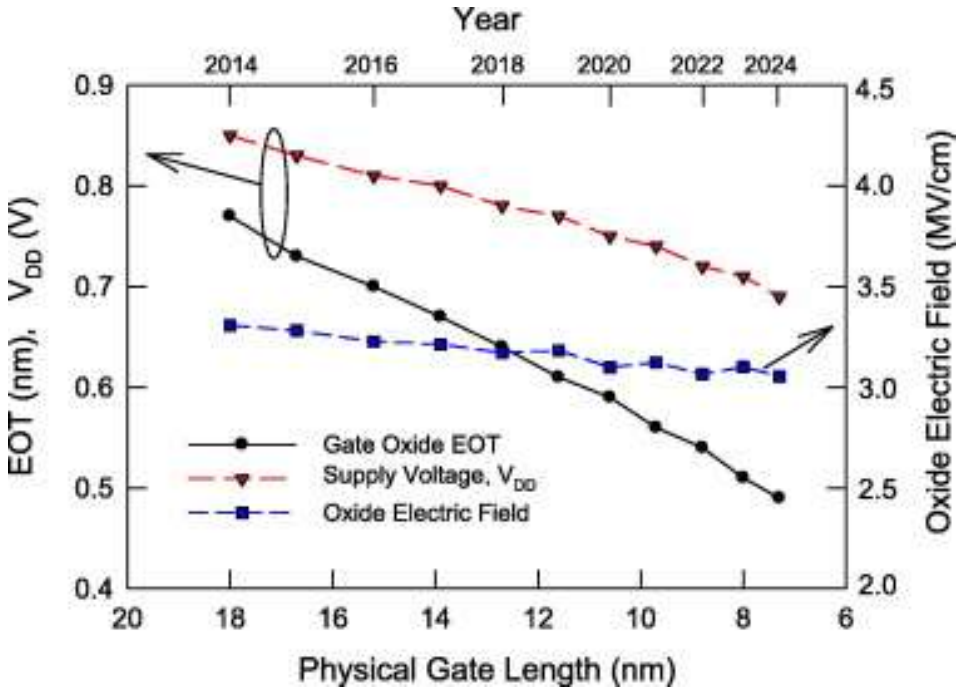


Initial step to raise k was to incorporate Si_3N_4 into the SiO_2 gate ox called SION



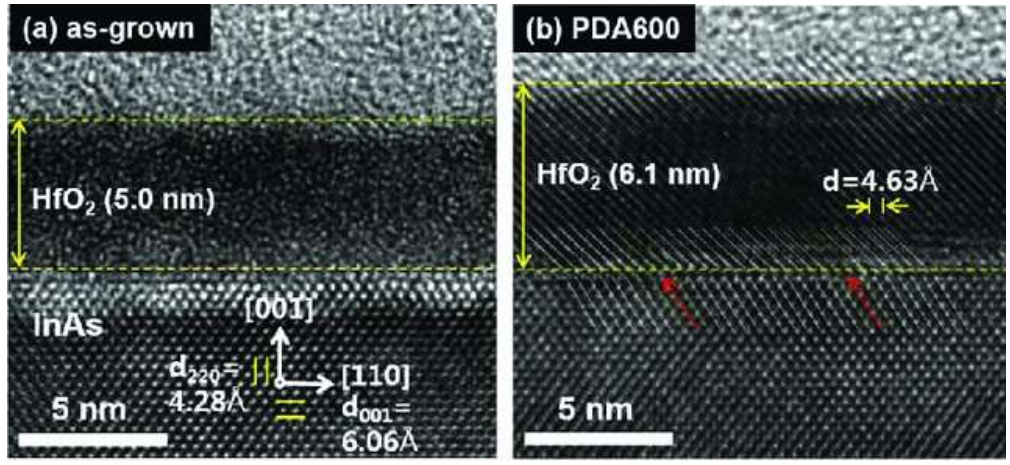
Initial step to raise k was to incorporate Si_3N_4 into the SiO_2 gate ox called SION





Today HfO_2 is established as common High-k dielectric for MOSFETs

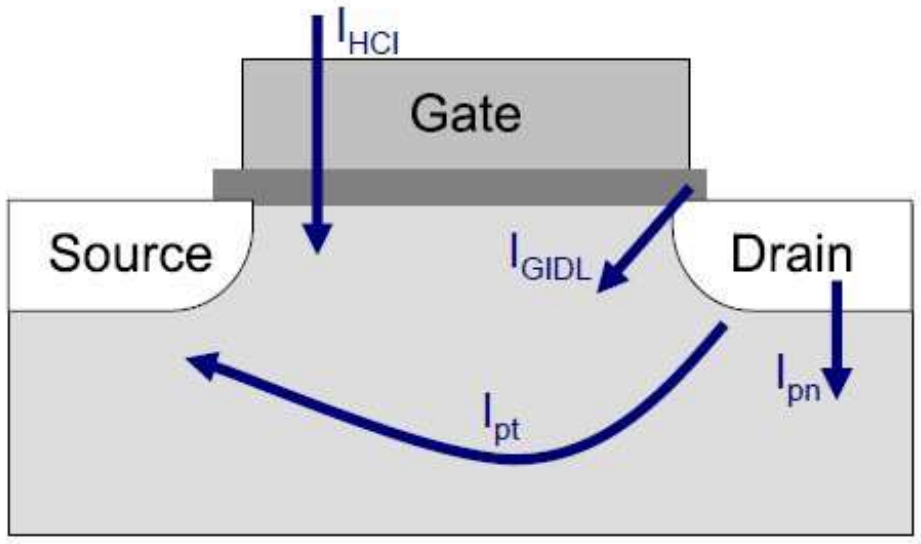
$k_{HfO2} \sim 20$



Equivalent Oxide Thickness: EOT = (3,9/20) 6,1 nm = 1,2 nm

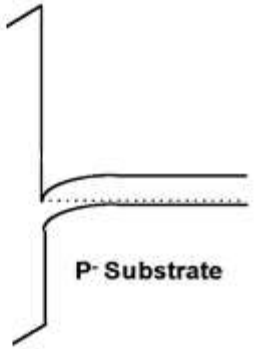
Further leakage mechanisms

- Reverse bias pn junction conduction I_{pn}
- Gate induced drain leakage I_{GIDL}
- Drain source punchthrough I_{PT}
- Hot carrier injection I_{HCI}

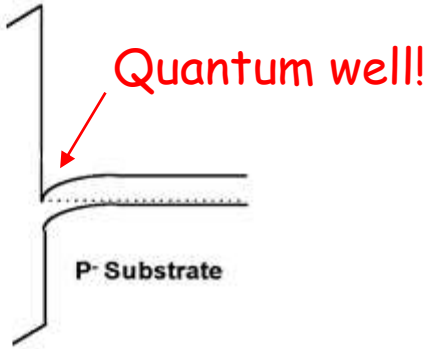


Taken from F. Sill Micro transductors 08

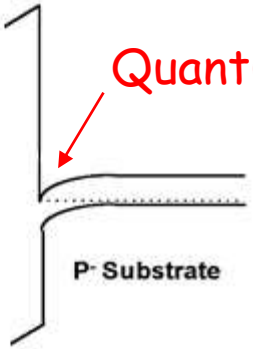
Effect of d_{ox} scaling is weaker than expected!

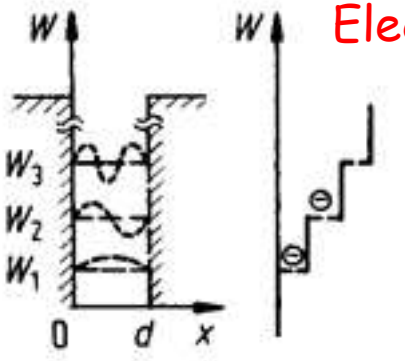


Effect of d_{ox} scaling is weaker than expected!



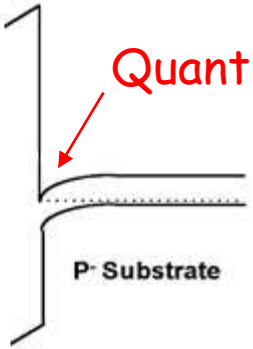
Effect of d_{ox} scaling is weaker than expected!

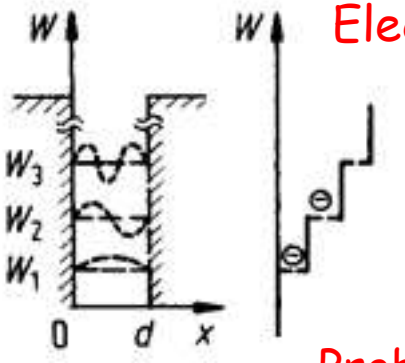




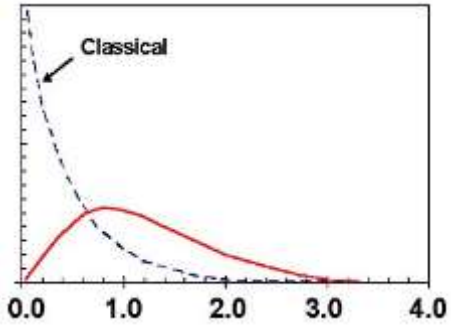
Electron states!

Effect of d_{ox} scaling is weaker than expected!

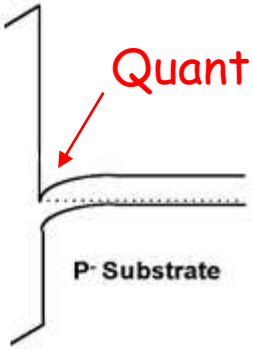




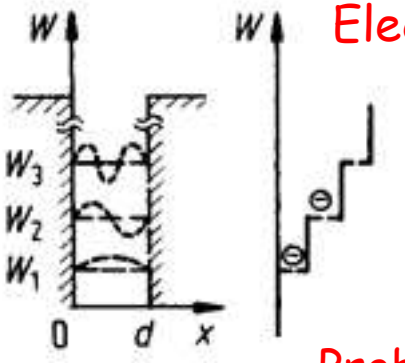
Probability function!



Effect of d_{ox} scaling is weaker than expected!

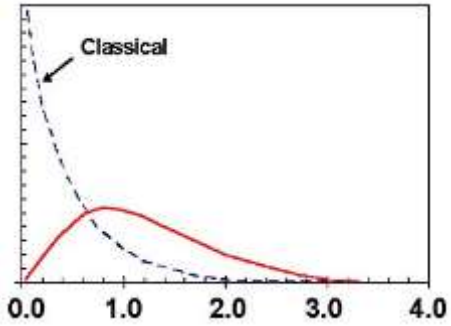


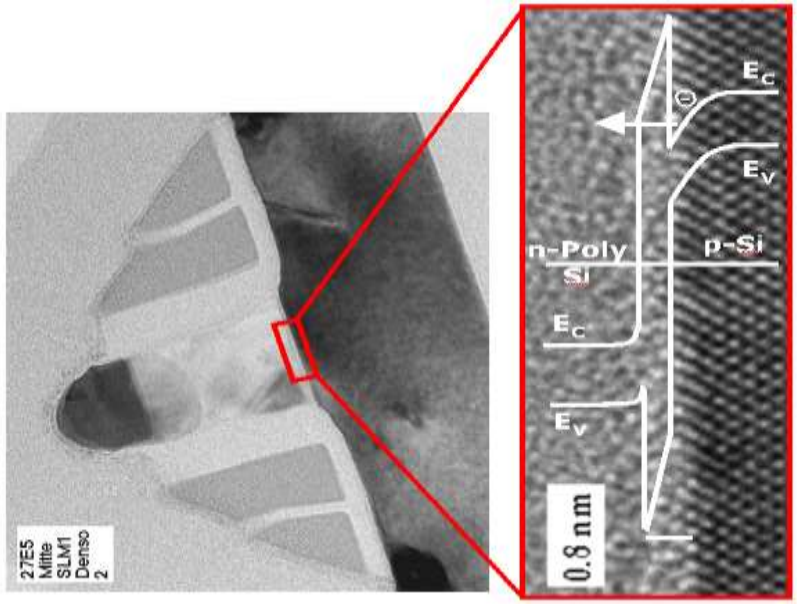
Quantum well!



Electron states!

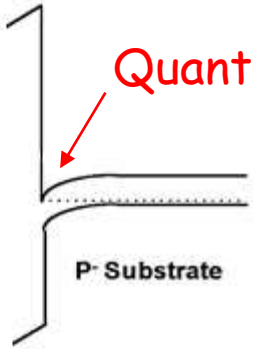
Probability function!

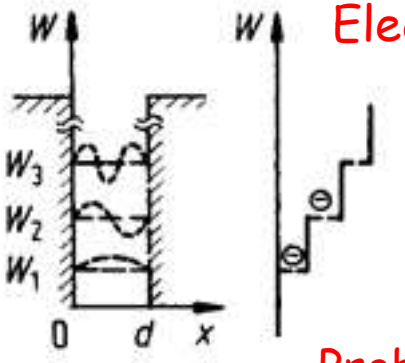




Si-Gate has two quantum wells!

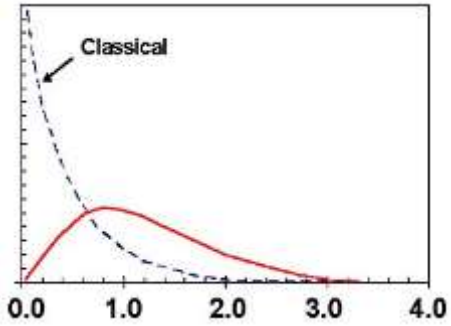
Effect of d_{ox} scaling is weaker than expected!

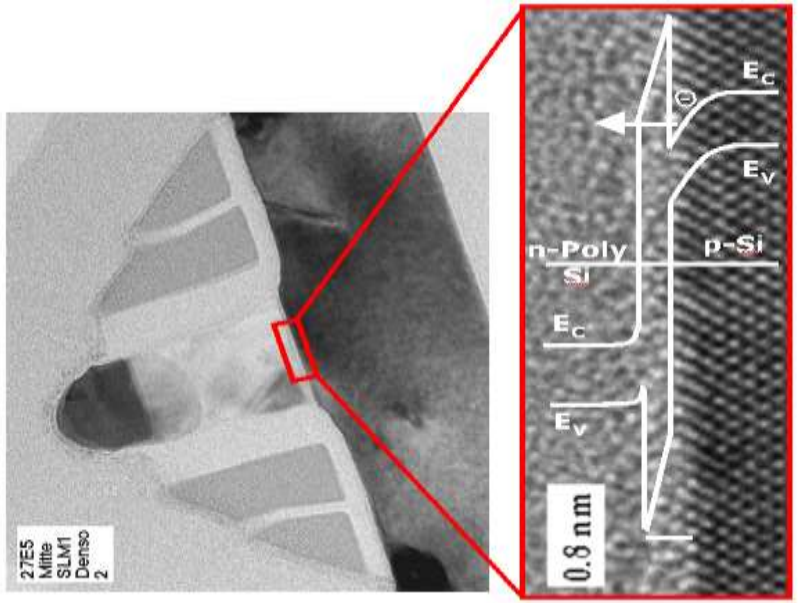




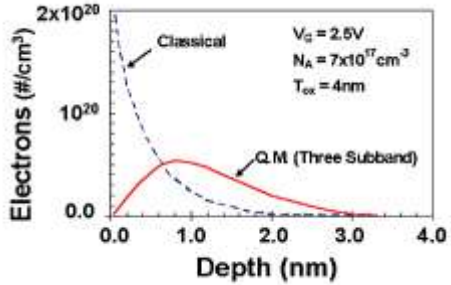
Electron states!

Probability function!

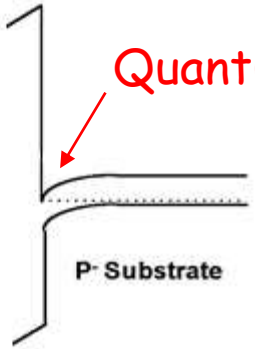


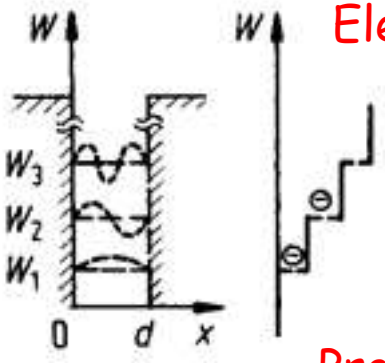


Si-Gate has two quantum wells!



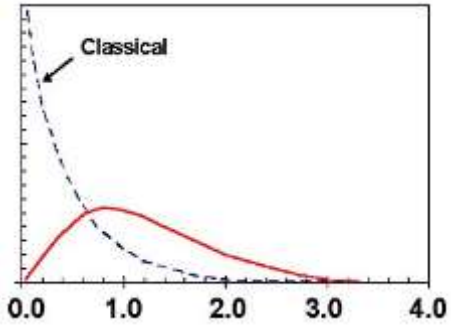
Effect of d_{ox} scaling is weaker than expected!

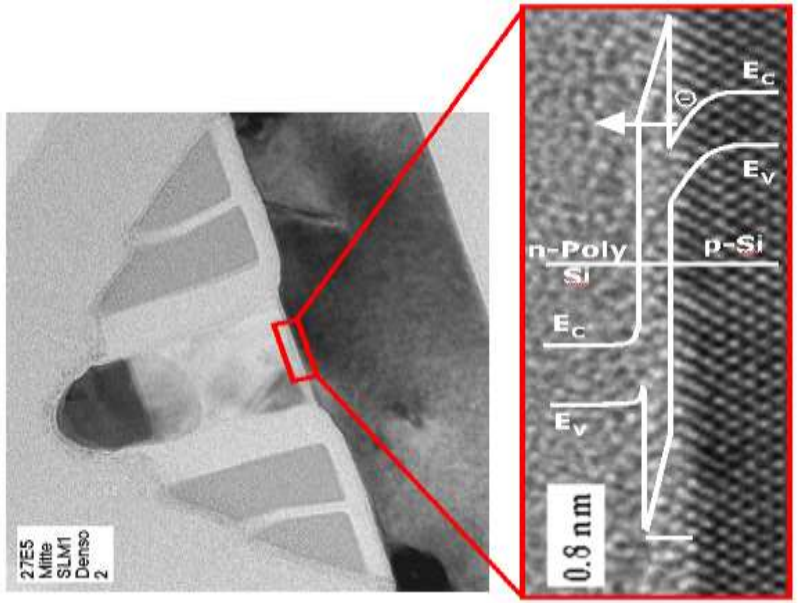




Electron states!

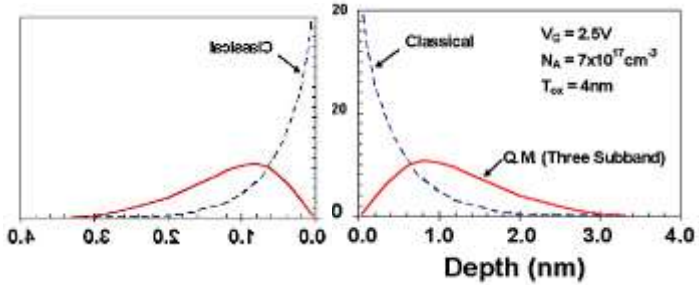
Probability function!



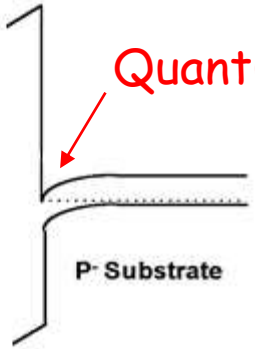


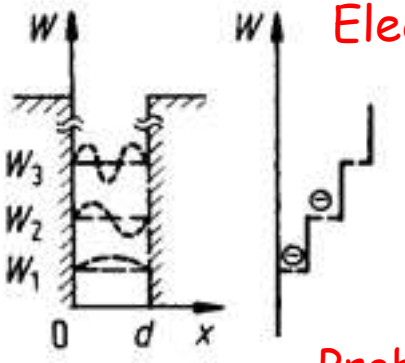
Si-Gate has two quantum wells!

poly depletion



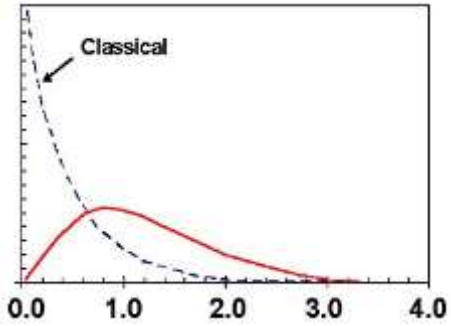
Effect of d_{ox} scaling is weaker than expected!

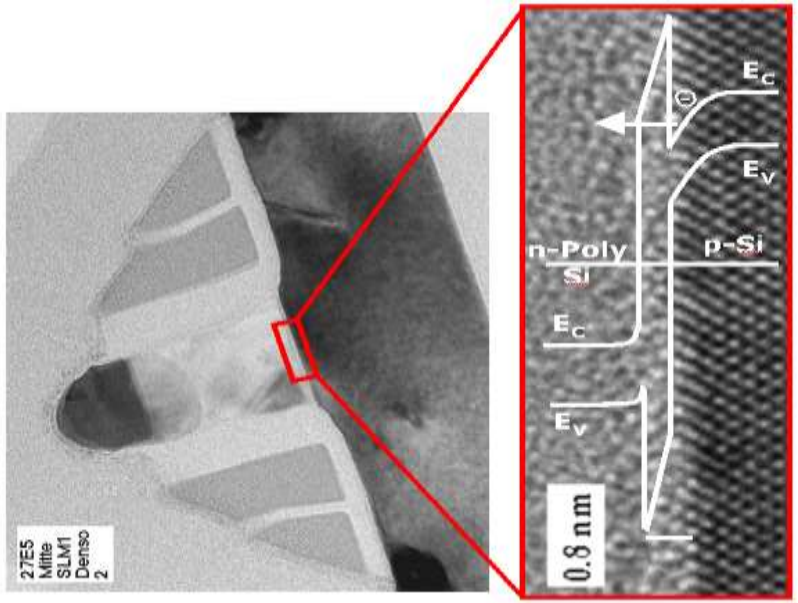




Electron states!

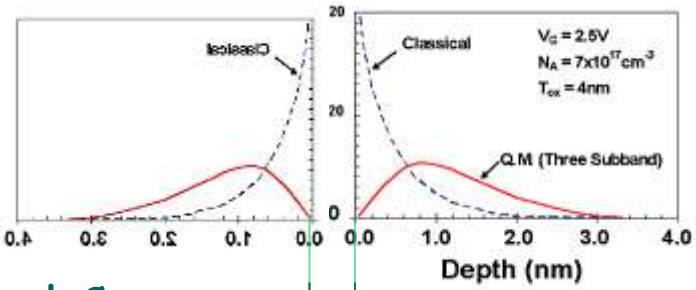
Probability function!





Si-Gate has two quantum wells!

poly depletion

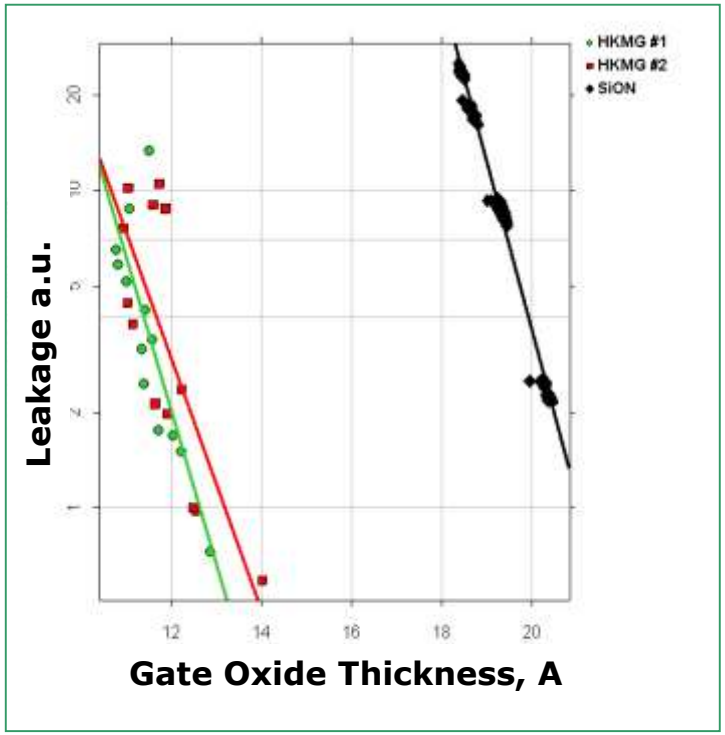


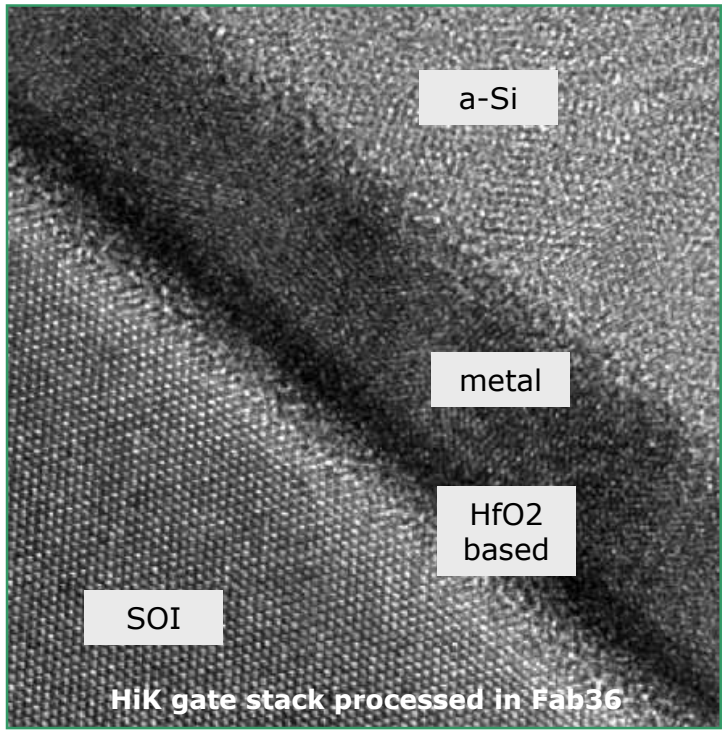
Classical Cap not real!

Real Si gate Cap

Metal gate Cap Better!

Motivation for HKMG – Gate Stack





High-k/Metal Gate (HKMG) reduces gate leakage by multiple orders of magnitude

Allows further shrink and subsequently more I_{on} at a given I_{off}

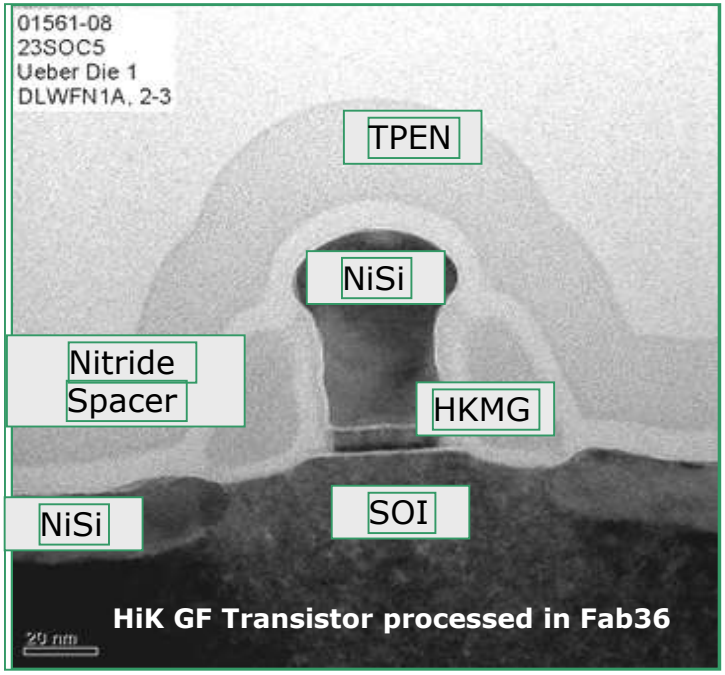
Gives more space between the metal/poly gate and the contact

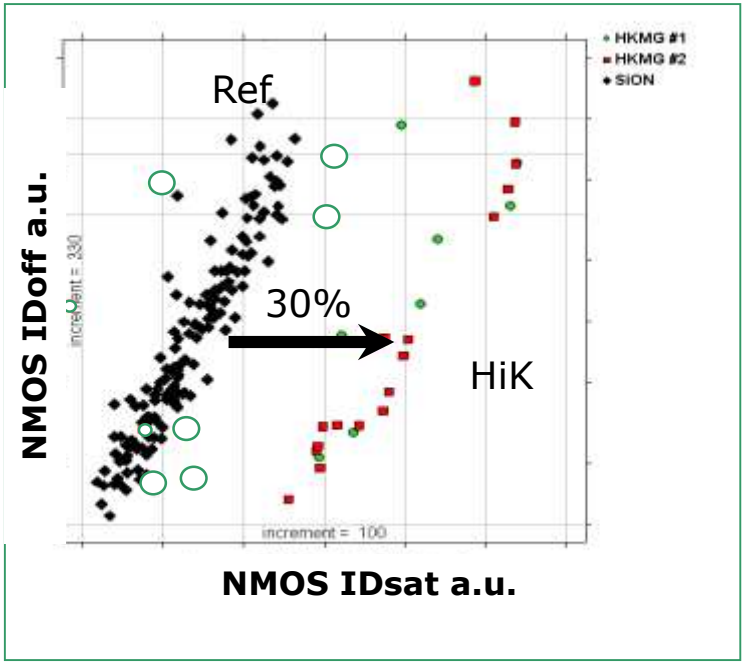
Reduces power consumption.

Can be combined with known stressors, like eSiGe and DSL

Taken from Horstmann DMA 2008

Initial High-K/Metal Gate @ AMD Dresden





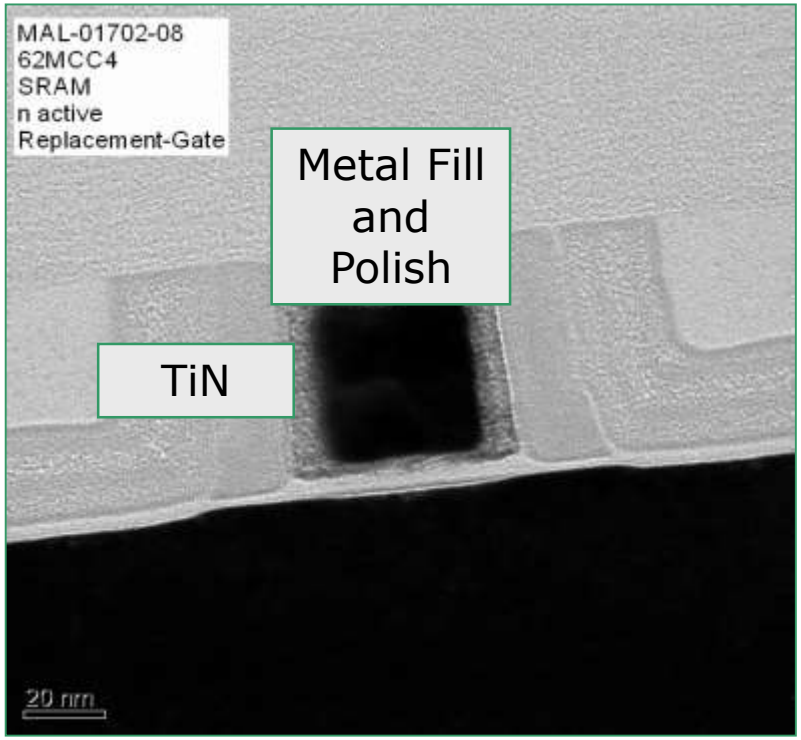
- GF* integration uses HKMG (including High K, Wf material, metal gate and poly) done in the FEoL. The materials see multiple high-temperature processes.
- It is a kind of straight replacement of the SiON/poly by Hik/metal
- 30% improvements in CMOS DC performance

*Gate First

Taken from Horstmann DMA 2008

High-K/Metal Gate @ AMD Dresden cont.

Alternative concept: Replacement Gate (RG)



HiK RG Transistor processed in Fab36

RG integration does the HiK/barrier/poly in the FEoL however it replaces the poly by metal fill and polish in the MoL

This material sees only low-temperature processes

New process steps are necessary to remove the poly and refill the gate cavities with several metals

Enhances stress effects

Taken from Horstmann DMA 2008

Challenges associated with sub100nm scaling:

Short channel effects

- DIBL
  - Shallow junction
  - Retrograde well
  - Halo Implant
  - SOI
- Leakage + I_{on}/I_{off}
  - High-k and Metal Gate

Challenges associated with sub100nm scaling:

Short channel effects

- DIBL
  - Shallow junction
  - Retrograde well
  - Halo Implant
  - SOI
- Leakage + I_{on}/I_{off}
  - High-k and Metal Gate

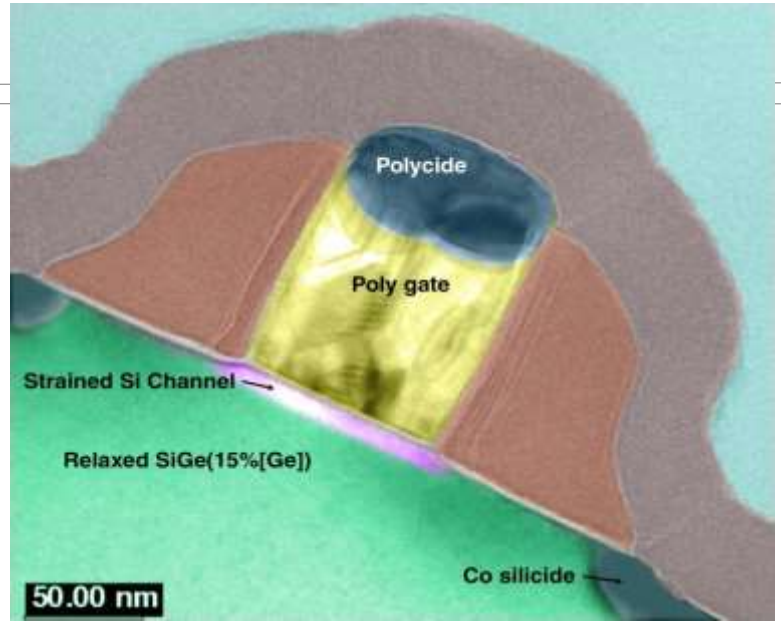
Continue
"SCT_SS20_13.04" 10:12
VIDEO CAMPUS SACHSEN

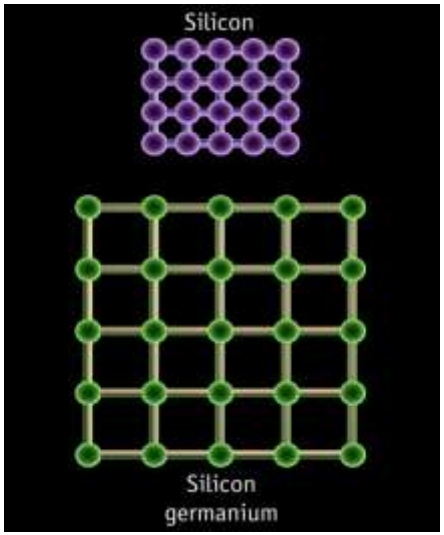
$$I_{Dsat} = \frac{\mu \varepsilon_0 \varepsilon_r}{2 d_{ox}} \frac{W}{L} (V_G - V_T)^2$$

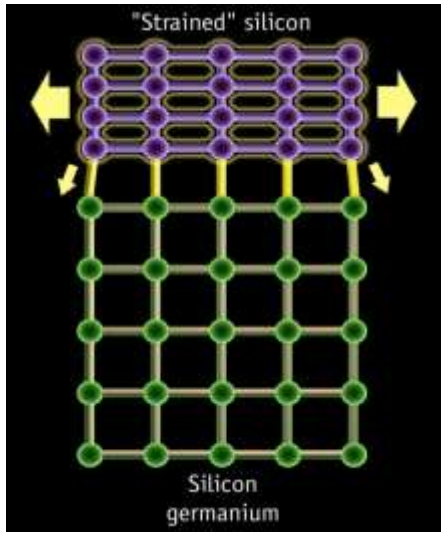
„Strained Silicon“:

Significant gain in charge carrier mobility by application of 2D lattice strain. Compressive enhances hole mobility, Tensile enhances electron mobility!

IBM 5/2001



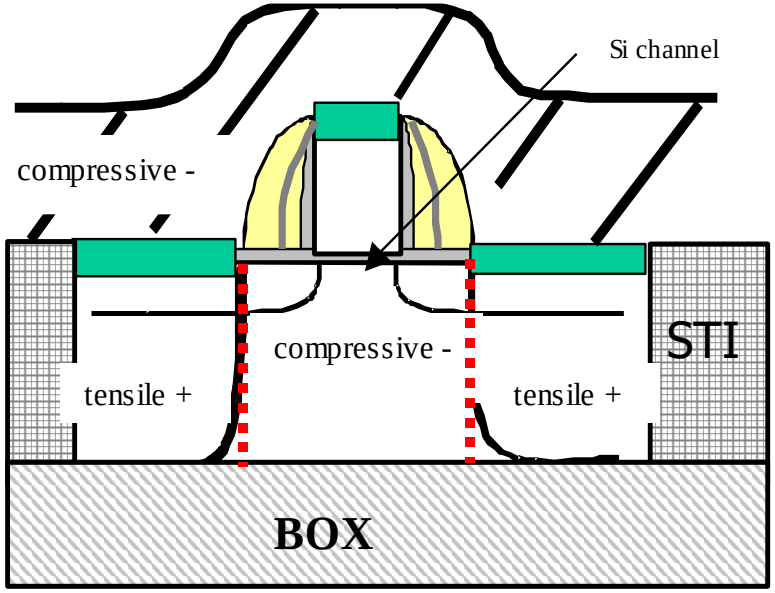




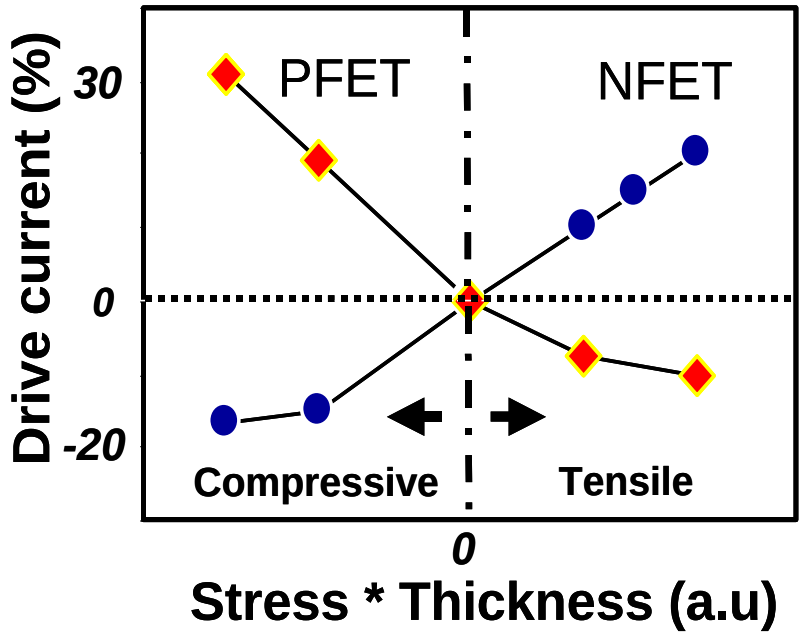
Local strain: Stressed Liner Films (Mechanical stress)

H.S. Yang, Horstmann et al., Proc. IEDM 2004

Tensile (NMOS) and Compressive (PMOS) PECVD SIN films



PMOS shown as example

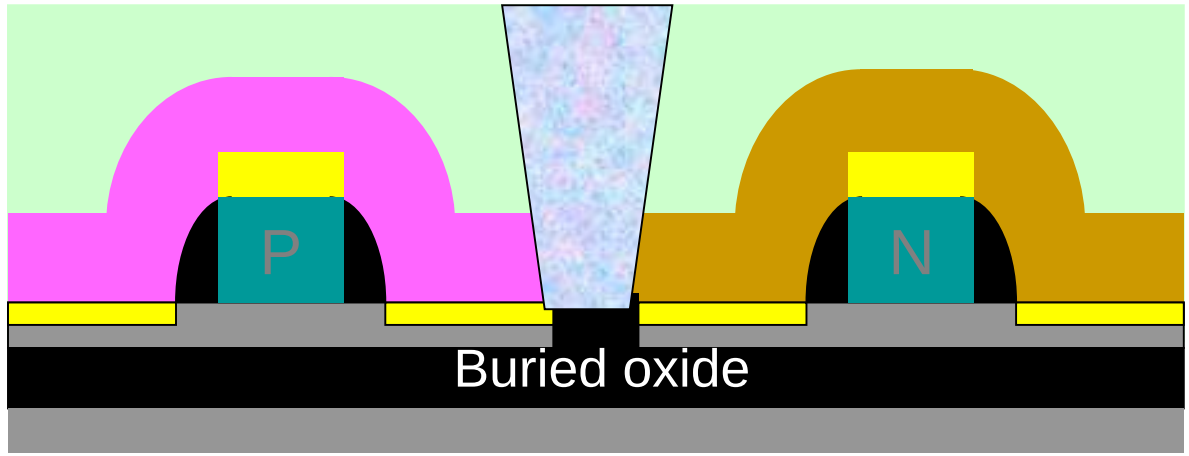


Dual Stressed Liner process: simultaneous improvement of NMOS and PMOS by tensile and compressive stressed overlayer films

Taken from Horstmann DMA 2008

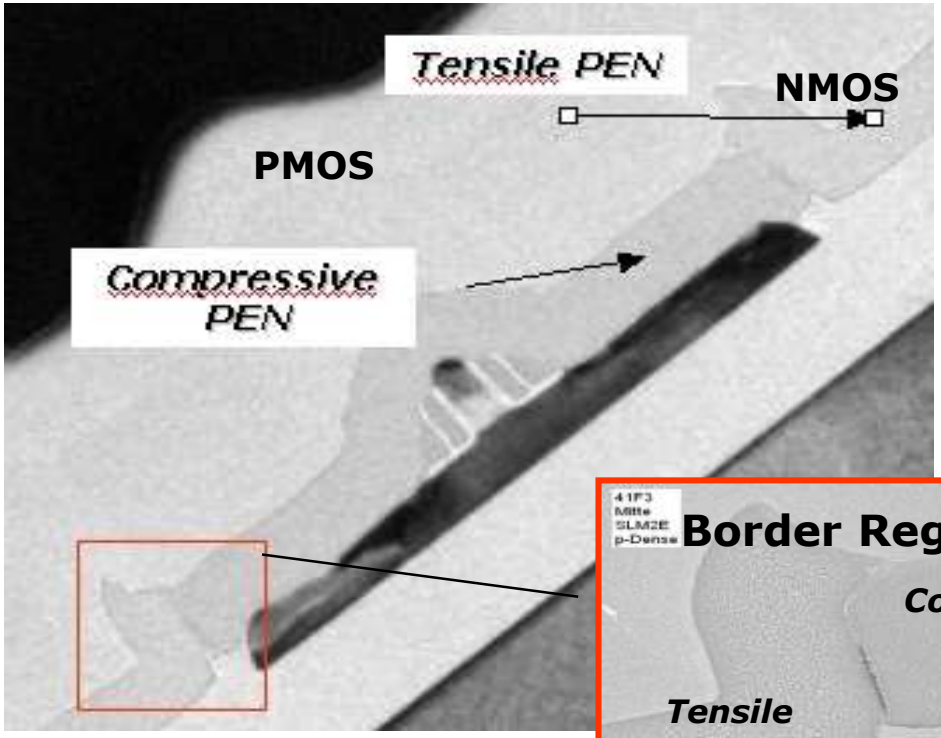
Dual Stressed Liner: Process flow

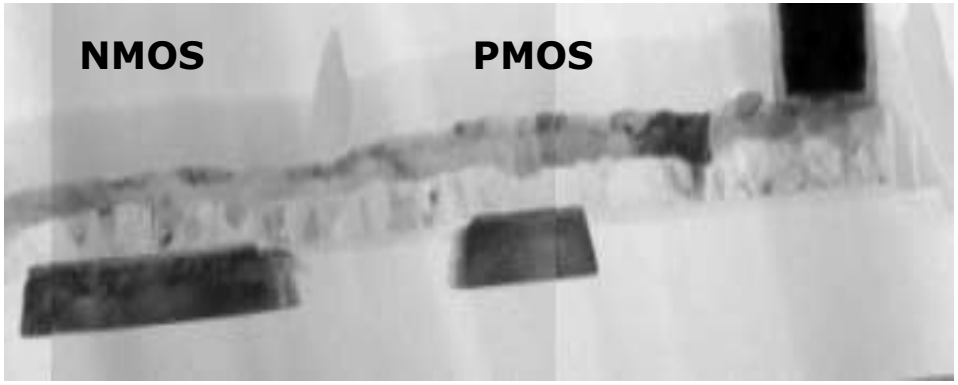
- Silicide formation
- Compressive Stressed Overlayer Film
- Mask / Etch
- Tensile Stressed Overlayer Film
- Mask / Etch
- ILD dep / Contact



Taken from Horstmann DMA 2008

DSL: X-Sectional Overview



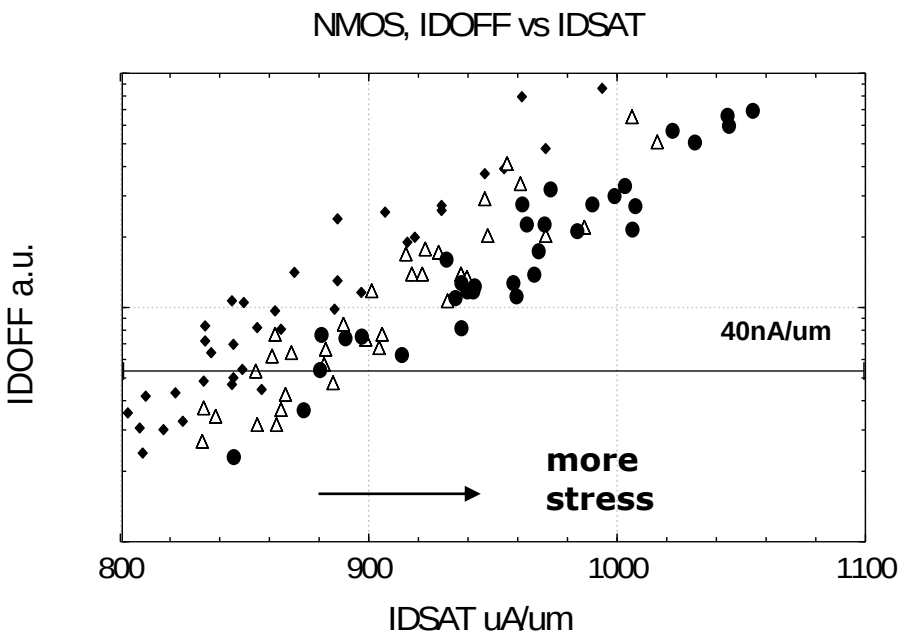


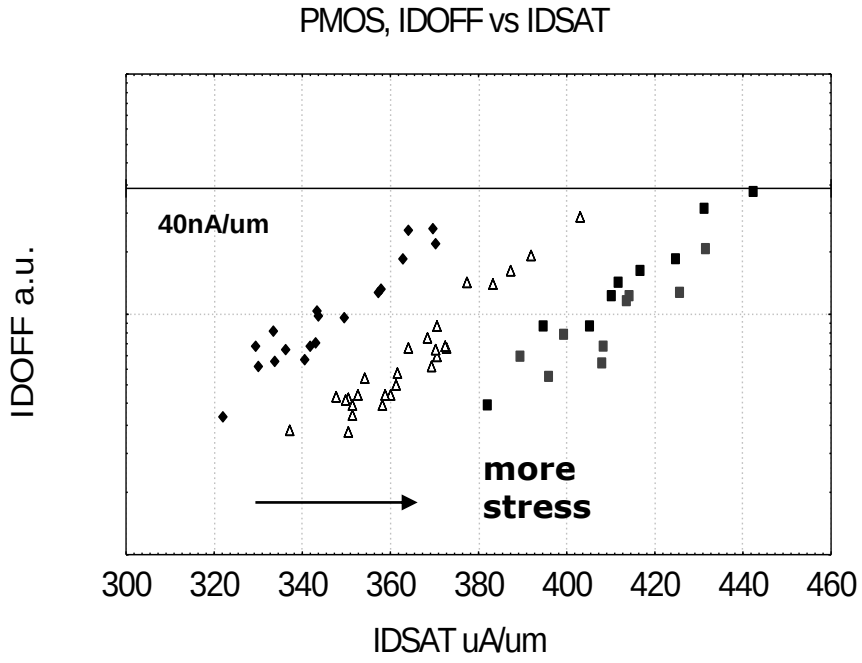
Inverter

DSL process is used in 90nm,65nm, 45nm manufacturing and is extendable down to 32nm technology

Taken from Horstmann DMA 2008

DSL: NMOS DC Performance



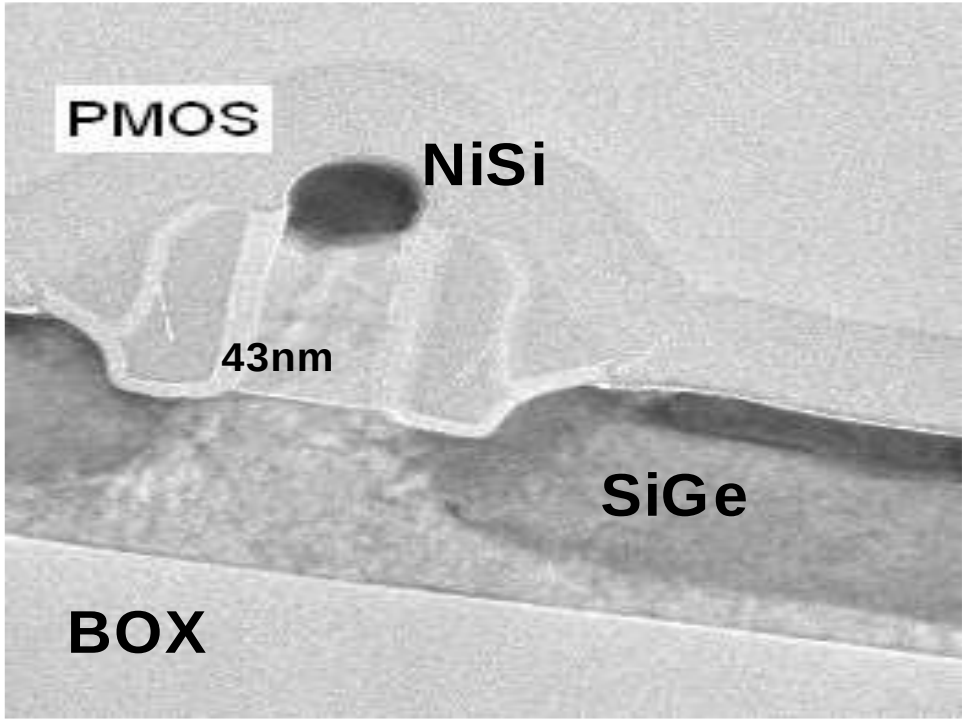


The NMOS and PMOS universal curves (Idsat vs Ioff) depends strongly on the tensile and compressive stress, respectively

Taken from Horstmann DMA 2008

AMD's eSiGe PMOS Transistor on SOI

M. Horstmann, A.Wei et al., Proc. IEDM 2005



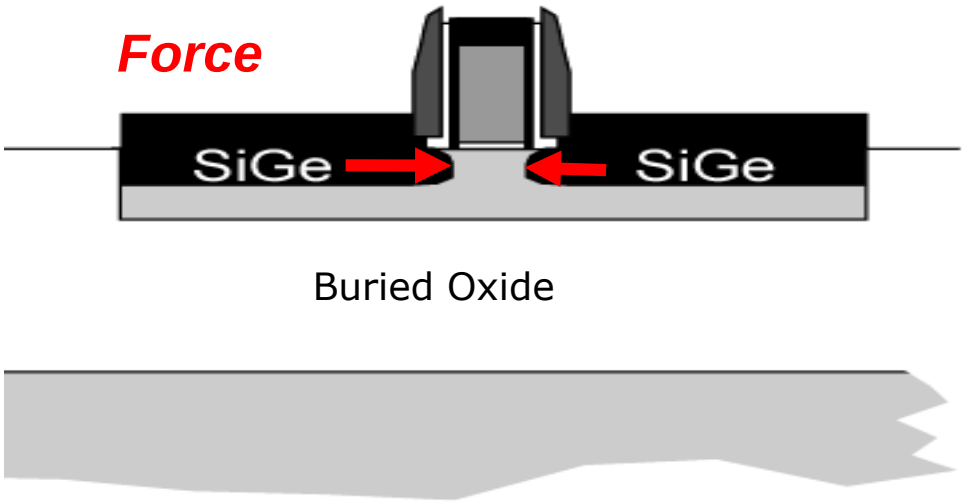
Key parameters for yield & performance:
- Proximity
- Cavity shape
- SiGe quality (defects)

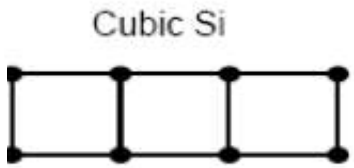
SiGe flow:

- **Gate Formation**
- **Disposable Spacer**
- **Hardmask for NMOS**
- **Cavity Etch**
- **SiGe-Epitaxy (undoped)**
- **Dispose Spacer**
- **Standard Processing**

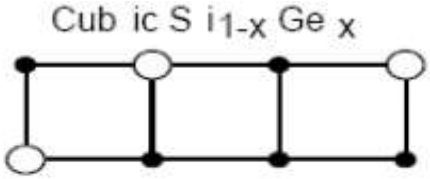
Taken from Horstmann DMA 2008

Local strain: embedded SiGe (lattice stress)

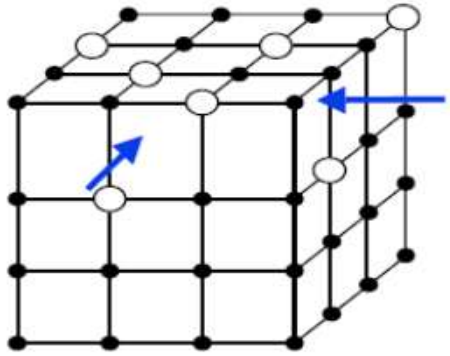




$a_{Si} = 5.431$ Å



$$mismatch = \frac{a_{Si} - a_{Ge}}{a_{Si}} \sim 4.1\%$$



Strained SiGe on Si

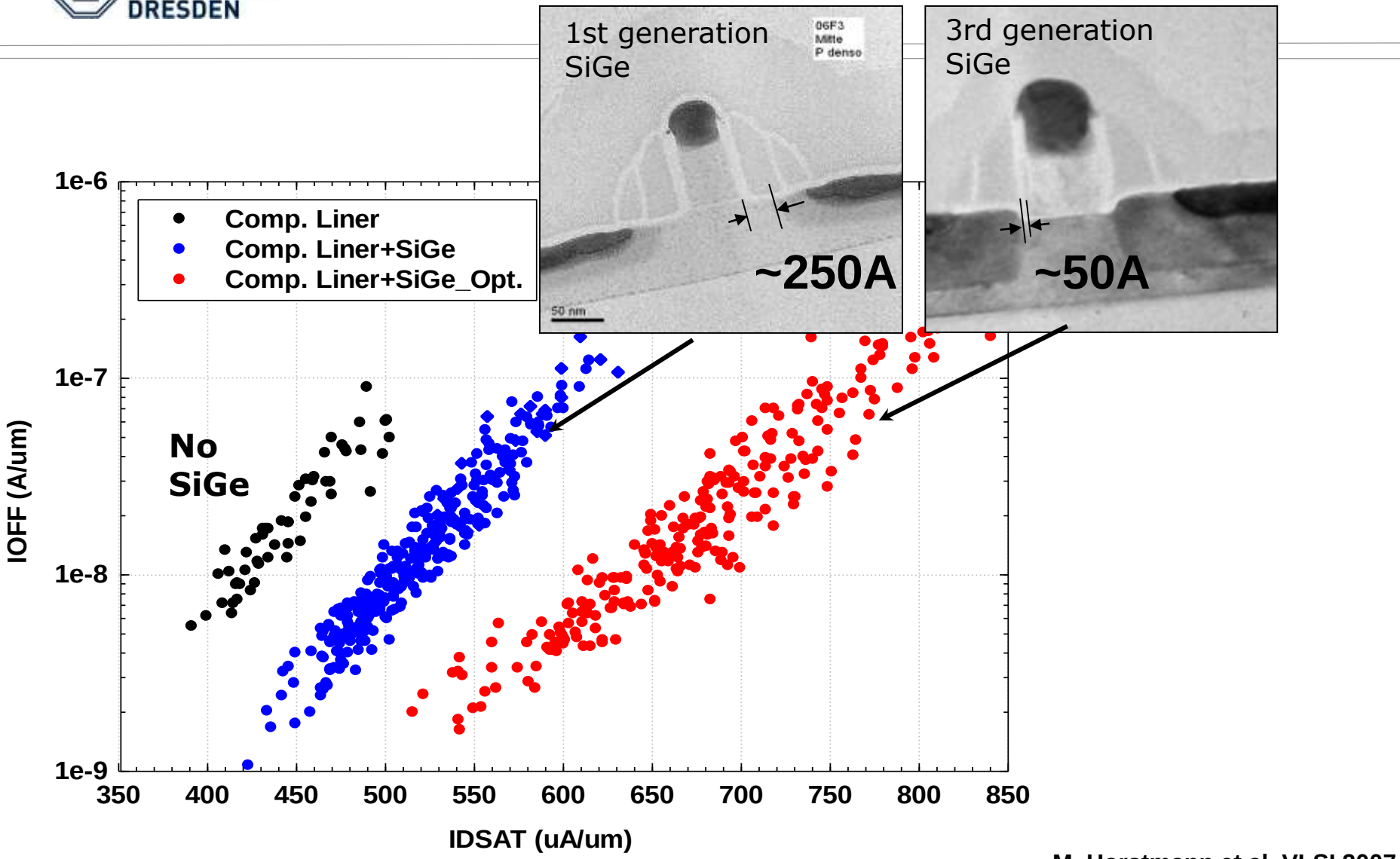
-> the epitaxialy grown SiGe is strained due to the lattice mismatch

-> tries to regain its „natural" lattice constant

-> uniaxial force <u>compressing</u> the channel region

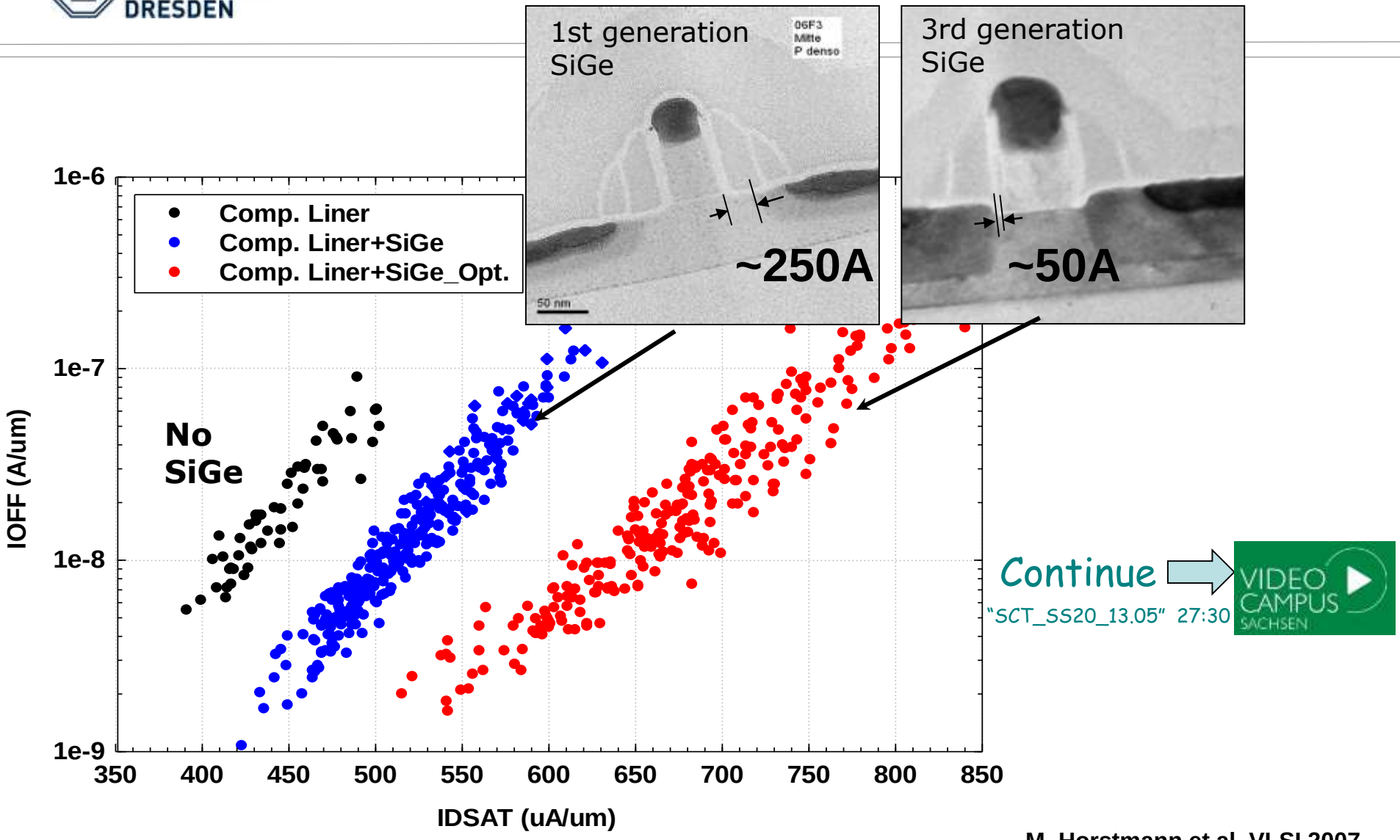
Taken from Horstmann DMA 2008

Embedded SiGe for PMOS



M. Horstmann et al. VLSI 2007

Embedded SiGe for PMOS



Continue "SCT_SS20_13.05" 27:30

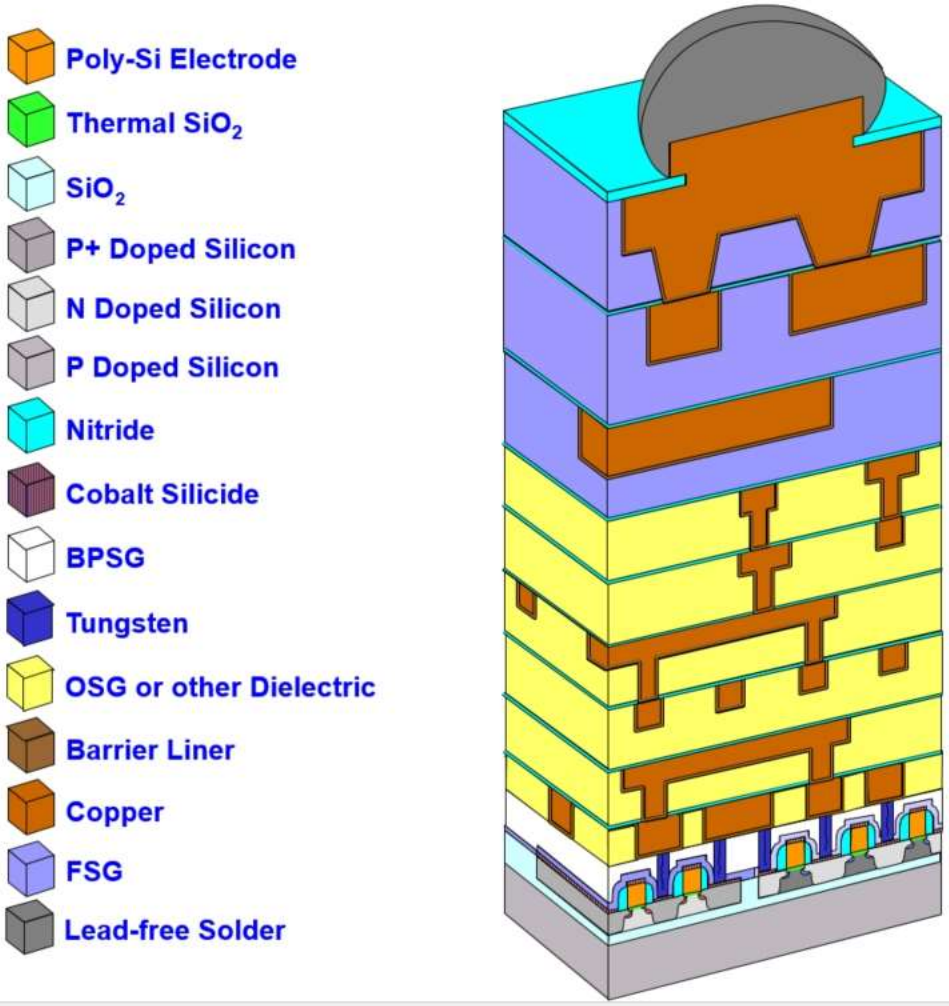
M. Horstmann et al. VLSI 2007

I have the permission to show the following slides in the class. However please understand that due to copyrights I am not allowed to hand out the slides.

The Logic Manufacturing Process Flow

Ernest Levine- Prof.-College of Nanoscale Science and Engineering, University at Albany---

*Format obtained from presentation by Conrad Sorenson of Prax Air. Modifications in Power Point done by Jobert Van Eisden. Build sequence represents a typical build of any no of different manufacturers at 90 nm node or smaller.



Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1.MOS Structure, MOS Capacitor
    2.Structure of a MOSFET
    3.I/V behavior
2. Circuits in Metal-Gate FET Technology
    1.Process sequence of N-MOSFET in Metal Gate
    2.From inverter to memory cell
    3.SRAM in NMOS Metal Gate
    4.The threshold voltage of the MOSFET
        1.Parasitic FET
        2.Enhancement/Depletion Transistor
        3.N-MOS Logic by E/D Transitors
        4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1.Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1.Example: Process flow of E/D SiGate LOCOS Inverter
        2.LOCOS Variation
        3.Shallow Trench Isolation
    3.Lightly doped drain
    4.SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4.Transition to CMOS Technology
    1.MOS Transistor Types
    2.CMOS Inverter
        1.Consideration NMOS E/D Inverter
        2.Comparison CMOS Inverter
    3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1.Scaling
        1. Challenges
        2.Material Equivalent Scaling
        3.Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

»Wissen schafft Brücken.«