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Lecture SCT2 - Process Integration

14. Web-based virtual Lecture: July 22 2021

Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here

"SCT_SS21_14.1" 1:02:49

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Outline

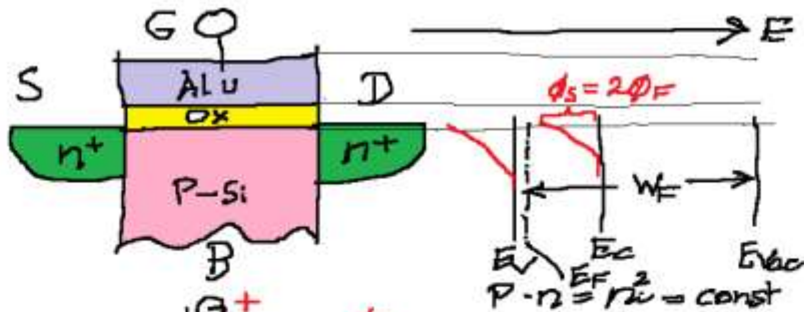
Review:
- SCT Basics
- MOS-Cap-CV
- MOS-FET (N-FET enh.)
- Al-Gate FET
- SRAM product (E/E)
- V_T adjust => Depl.
- E/D Logic
- Self aligned process
- ~180 nm CMOS Process
- Further Scaling

Today: Further Concepts and summary

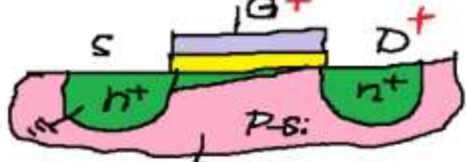
SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
    1. MOS Structure, MOS Capacitor
    2. Structure of a MOSFET
    3. I/V behavior
2. Circuits in Metal-Gate FET Technology
    1. Process sequence of N-MOSFET in Metal Gate
    2. From inverter to memory cell
    3. SRAM in NMOS Metal Gate
    4. The threshold voltage of the MOSFET
        1. Parasitic FET
        2. Enhancement/Depletion Transistor
        3. N-MOS Logic by E/D Transitors
        4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
    1. Metal Gate -> Si Gate
    2. Channel-Stop & LOCOS Technology
        1. Example: Process flow of E/D SiGate LOCOS Inverter
        2. LOCOS Variation
        3. Shallow Trench Isolation
    3. Lightly doped drain
    4. SALICIDE
    5. Self Aligned Contacts (SAC)
    6. Resist trimming
4. Transition to CMOS Technology
    1. MOS Transistor Types
    2. CMOS Inverter
        1. Consideration NMOS E/D Inverter
        2. Comparison CMOS Inverter
    3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
    1. Scaling
        1. Challenges
        2. Material Equivalent Scaling
        3. Further Concepts

http://www.computerhistory.org/siliconengine/timeline/



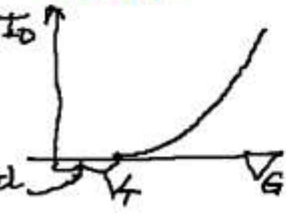
Self alignment
Al-Gate > Si-Gate
FOX > LOCOS > STI
LDD ~ source drain ext.
Polycide > Salicide
SAC & Resist Trim

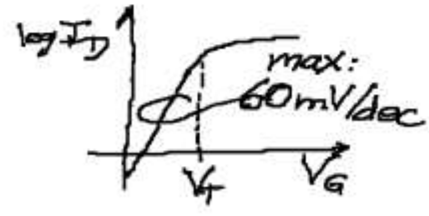


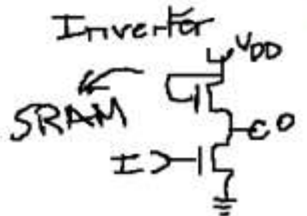
Shrinking!

$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{d_{ox}} \frac{W}{L} \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right]$

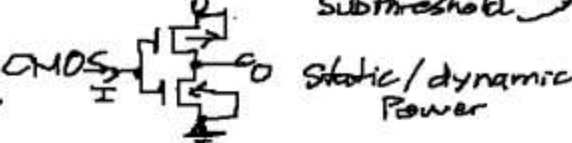
$I_{Dsat} = \frac{\mu \varepsilon_0 \varepsilon_r}{2 d_{ox}} \frac{W}{L} (V_G - V_T)^2$







ED



$W_G - W_{Si}$

$$V_T = \frac{d_{ox}}{\varepsilon_{ox}} \sqrt{2 \varepsilon_{Si}\, e N_A (2\phi_F + V_{SB})} + 2\phi_F - \frac{Q_{ox}}{C_{ox}} + \frac{\Delta W_F}{e}$$

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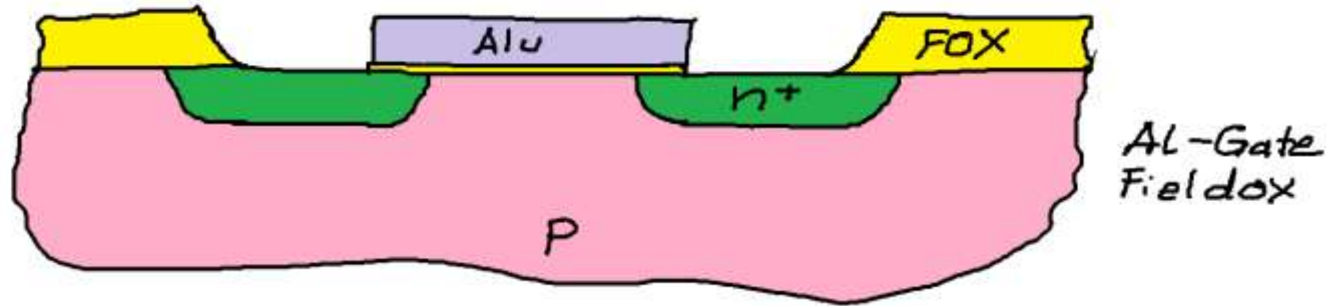
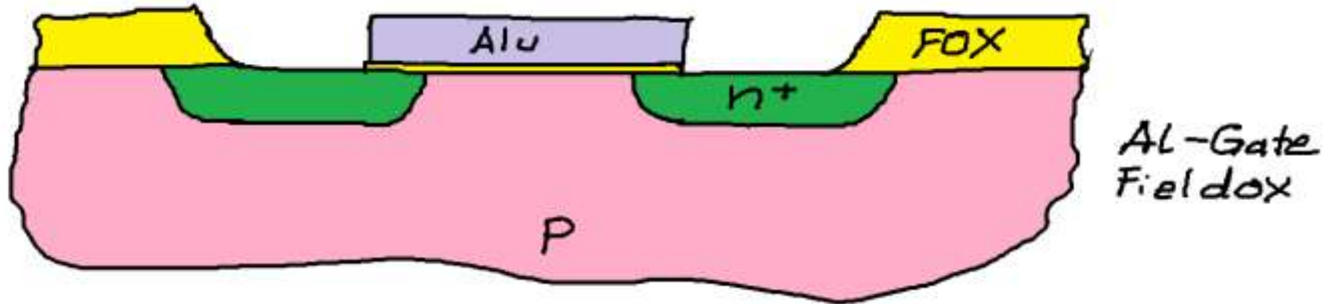
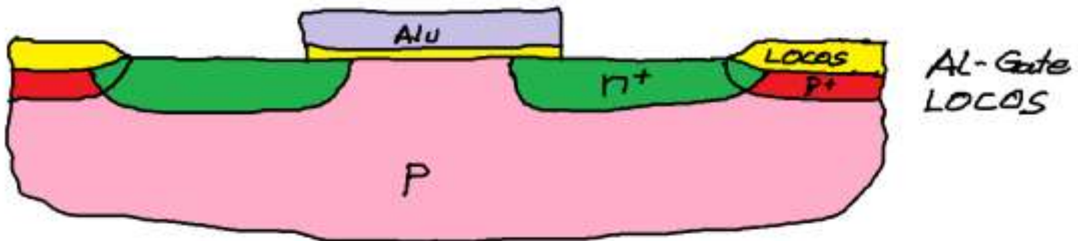
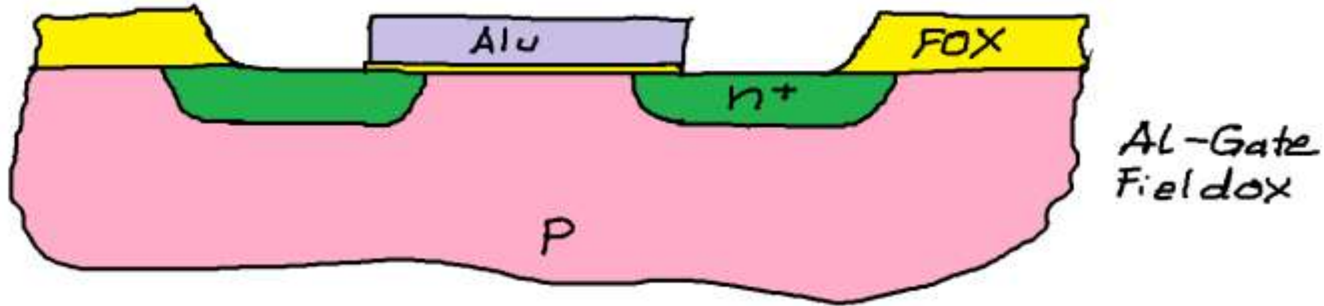
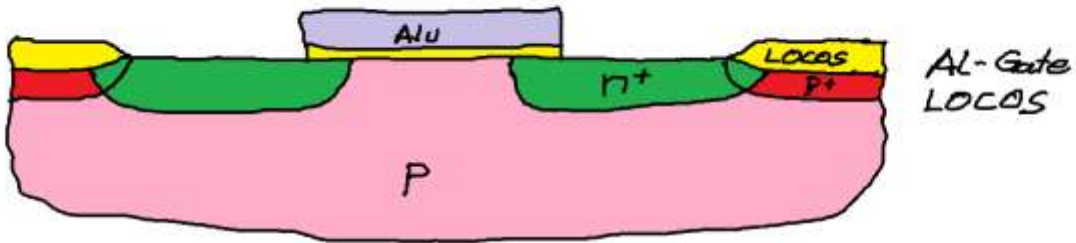
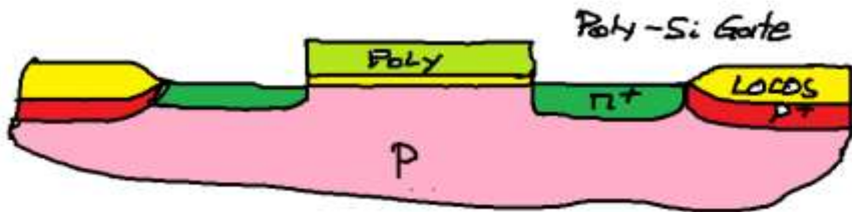

Alu
FOX
n+
P
Al-Gate
Fieldox

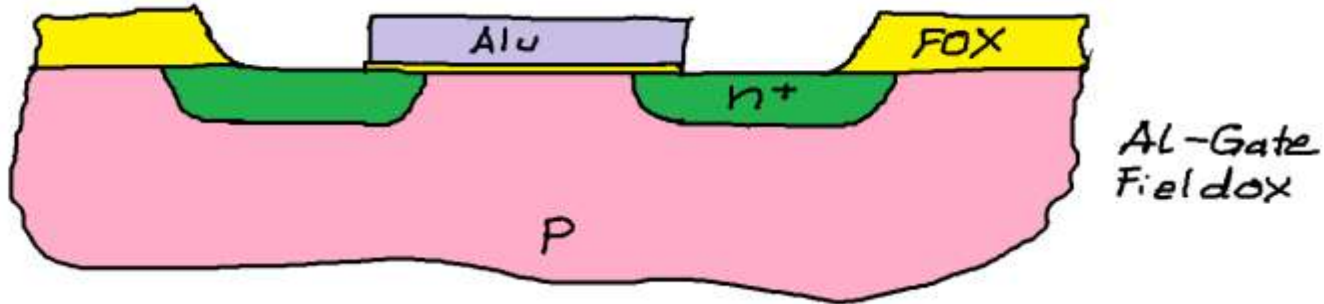

Alu
FOX
n+
P
Al-Gate
Fieldox

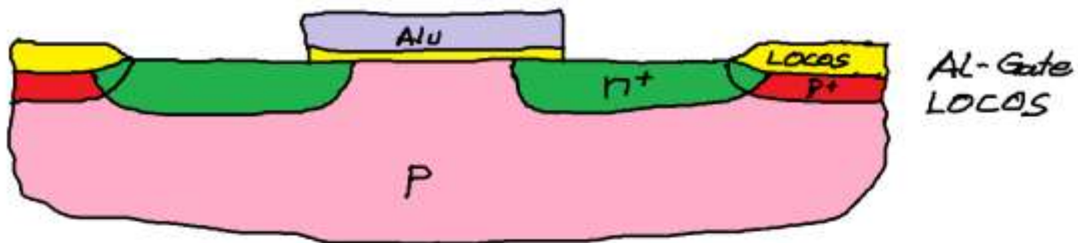

Alu
LOCOS
n+
p+
P
Al-Gate
LOCOS

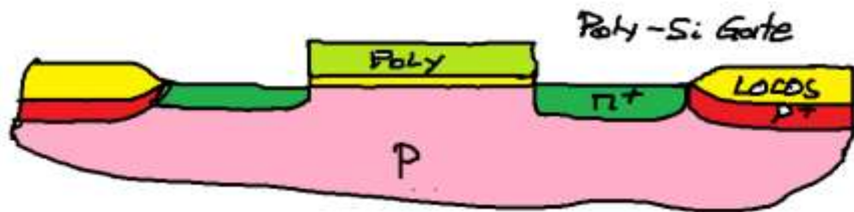

Alu
FOX
n+
P
Al-Gate
Fieldox

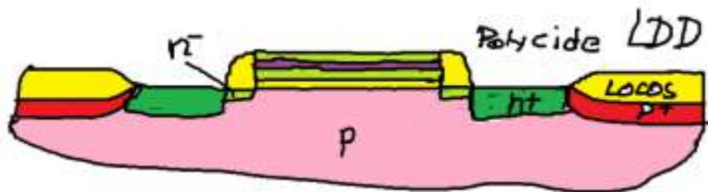

Alu
LOCOS
n+
p+
P
Al-Gate
LOCOS

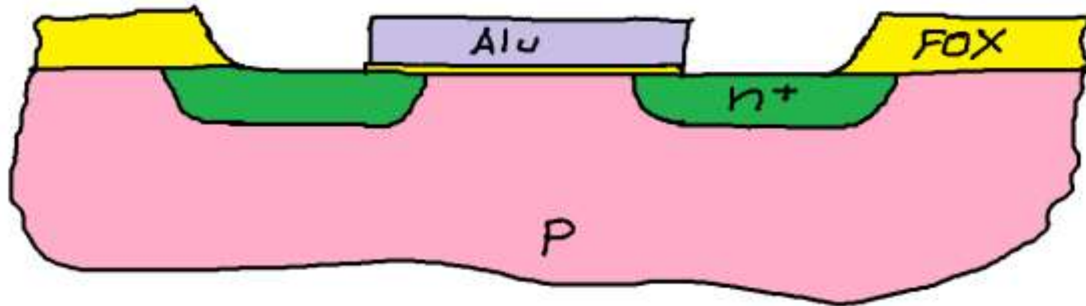

Poly-Si Gate
Poly
LOCOS
n+
p+
P

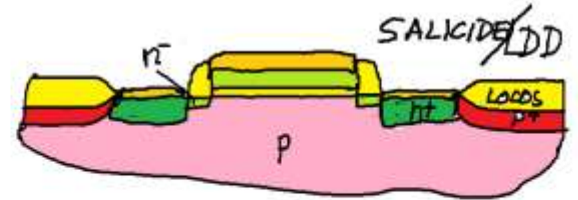

Alu
FOX
n+
P
Al-Gate
Fieldox

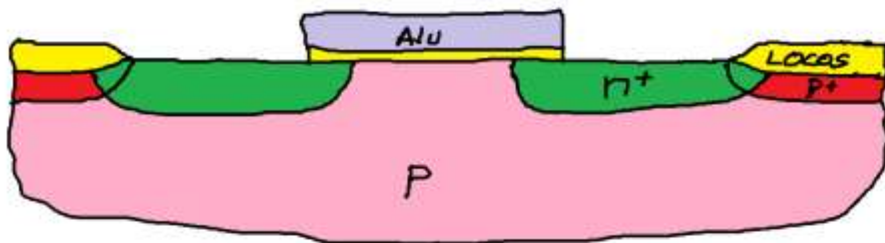

Alu
LOCOS
n+
p+
P
Al-Gate
LOCOS

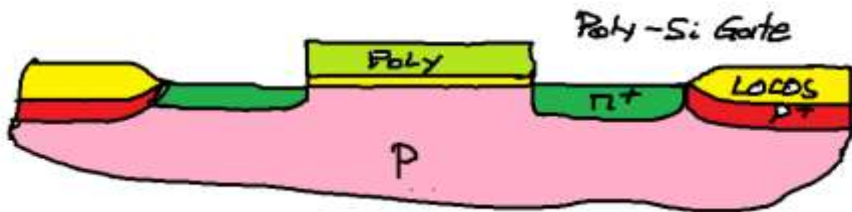

Poly-Si Gate
Poly
n+
LOCOS
p+
P

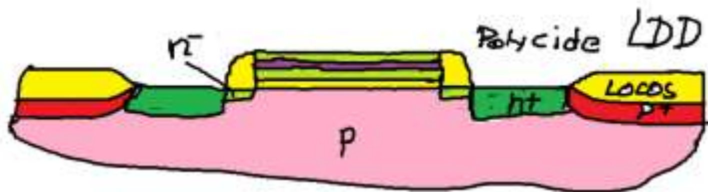

n-
Polycide LDD
LOCOS
n+
p+
p

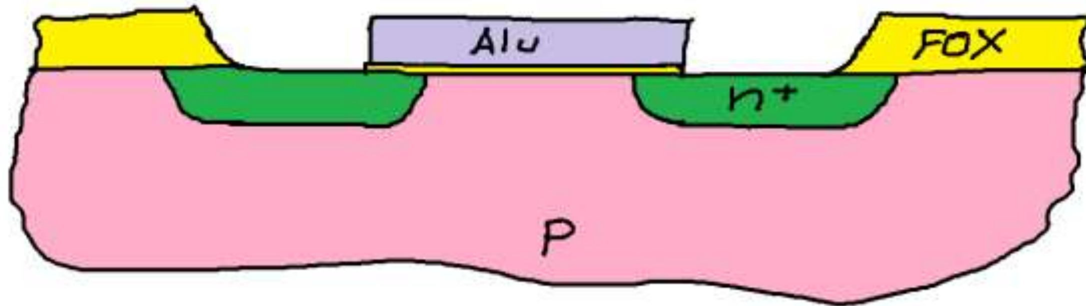

Alu
FOX
n+
P
Al-Gate
Fieldox


SALICIDE/LDD
n⁻
LOCOS
n+
p+
p

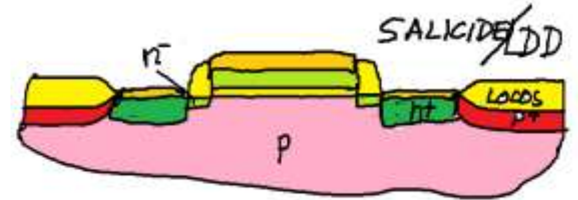

Alu
LOCOS
n+
p+
P
Al-Gate
LOCOS

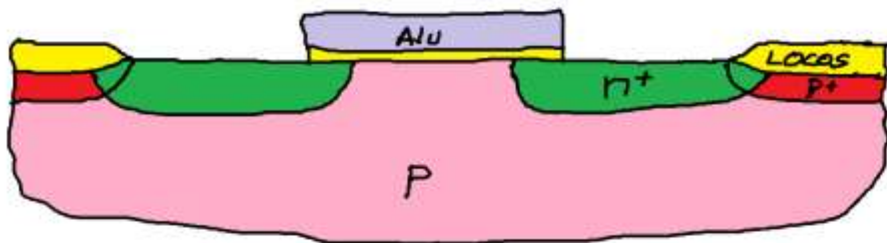

Poly-Si Gate
Poly
LOCOS
n+
p+
P


Polycide LDD
n⁻
LOCOS
n+
p+
p

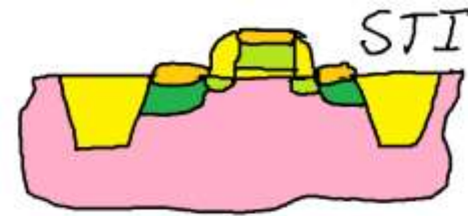


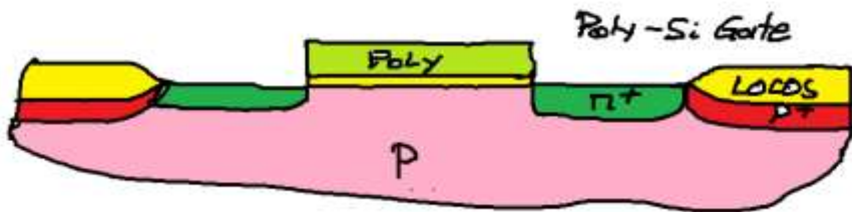
Al-Gate
Fieldox

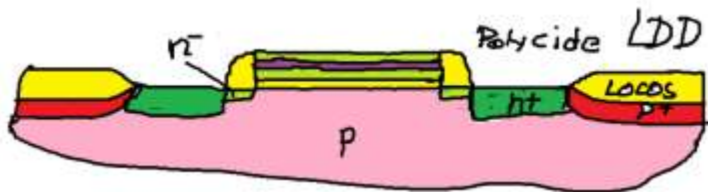


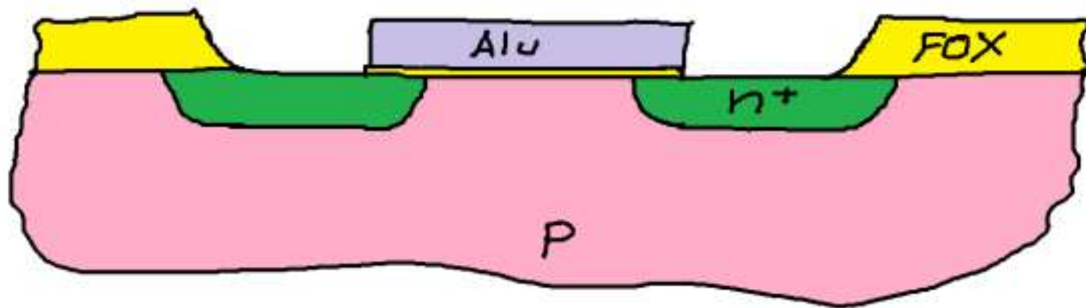


Al-Gate
LOCOS

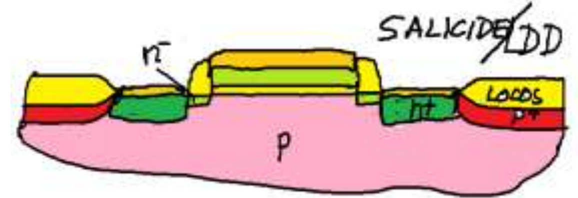


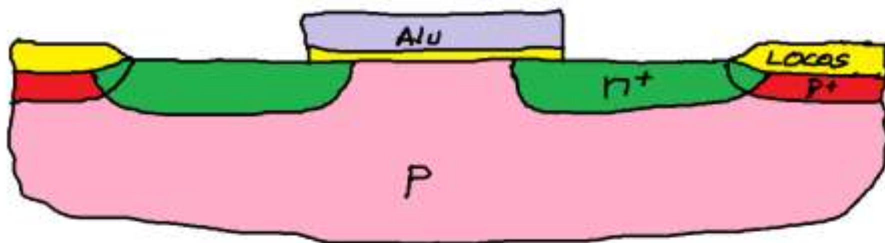




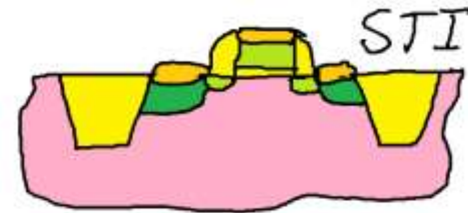


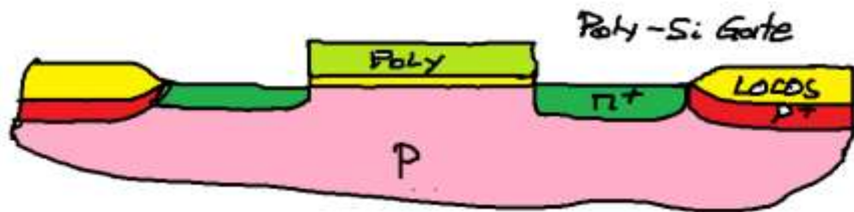
Al-Gate
Fieldox

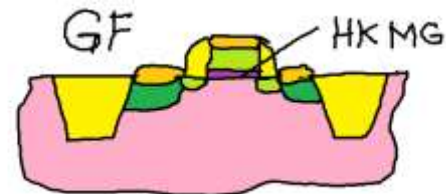


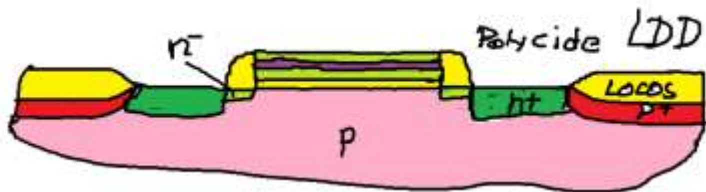


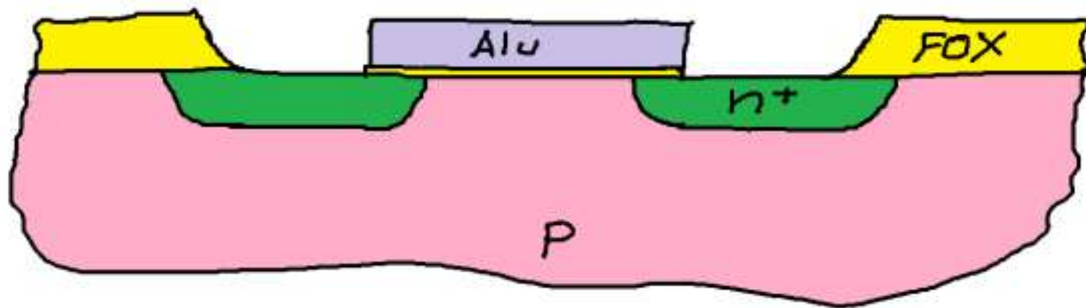
Al-Gate
LOCOS



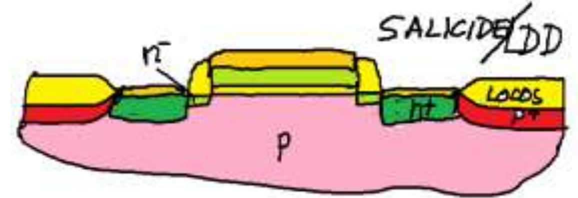


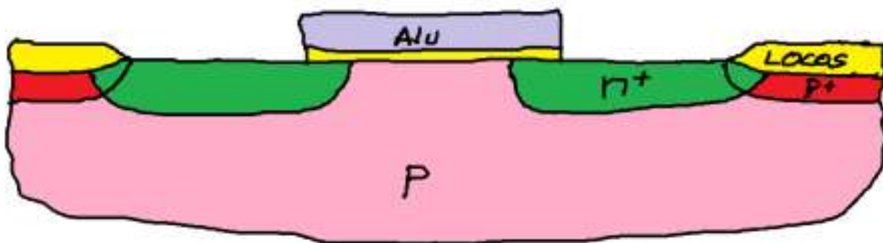




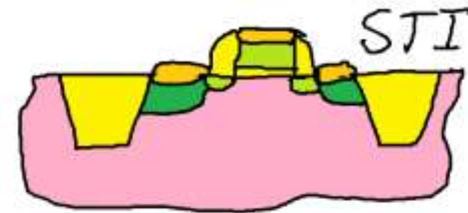


Al-Gate Fieldox

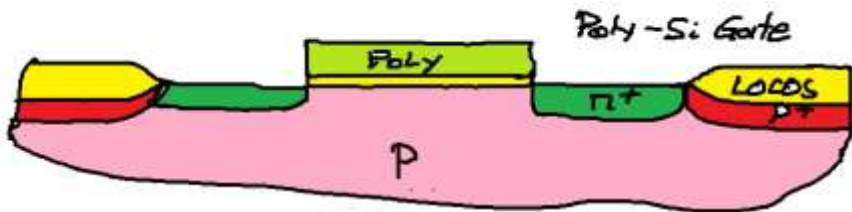


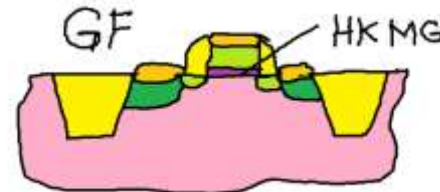


Al-Gate LOCOS

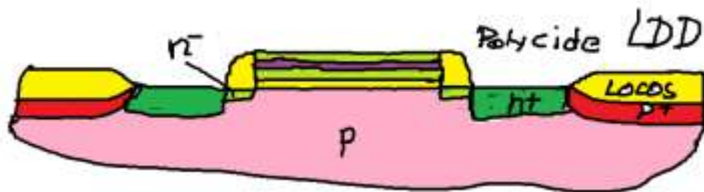


Poly-Si Gate





Polycide LDD



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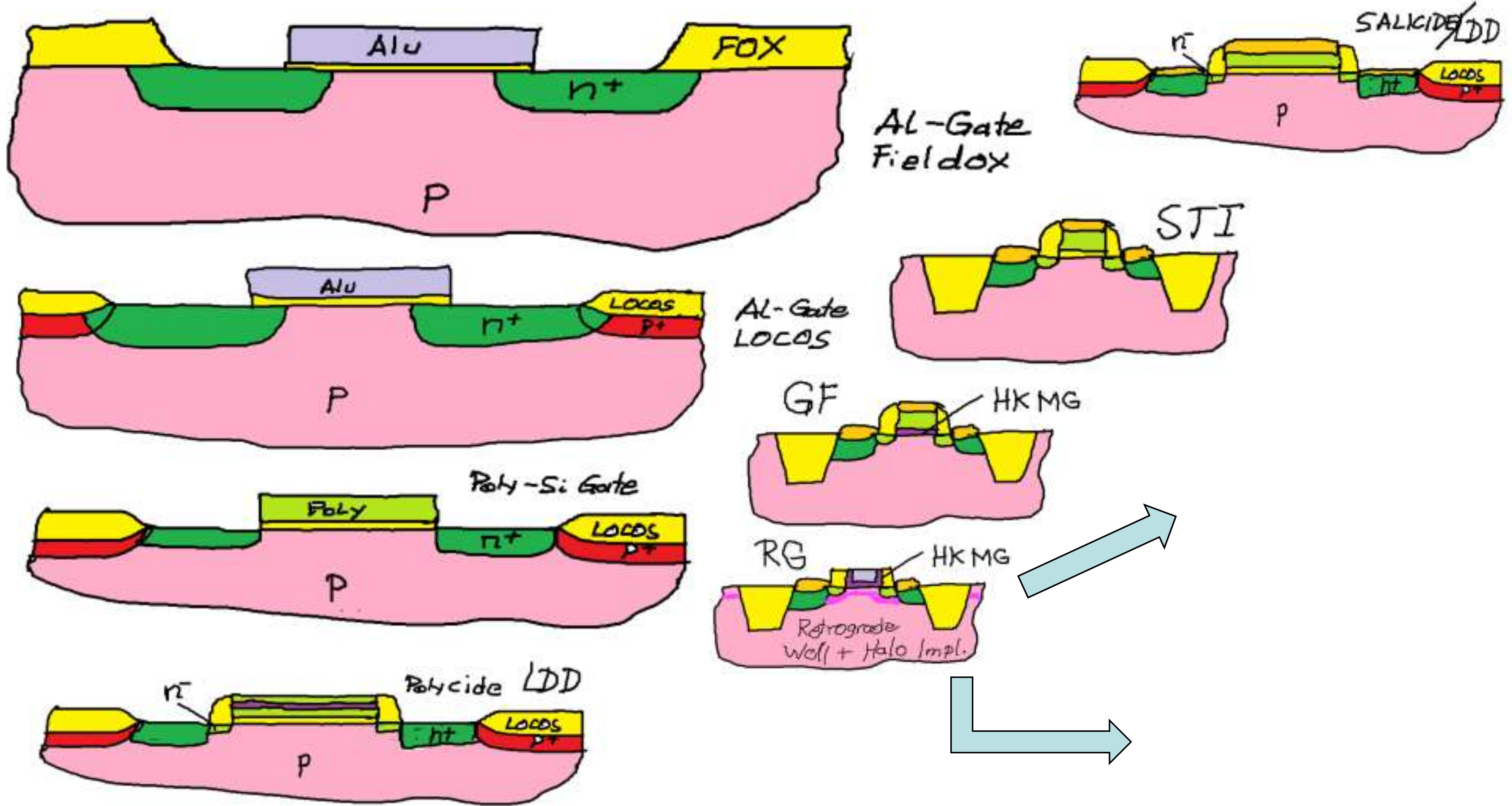
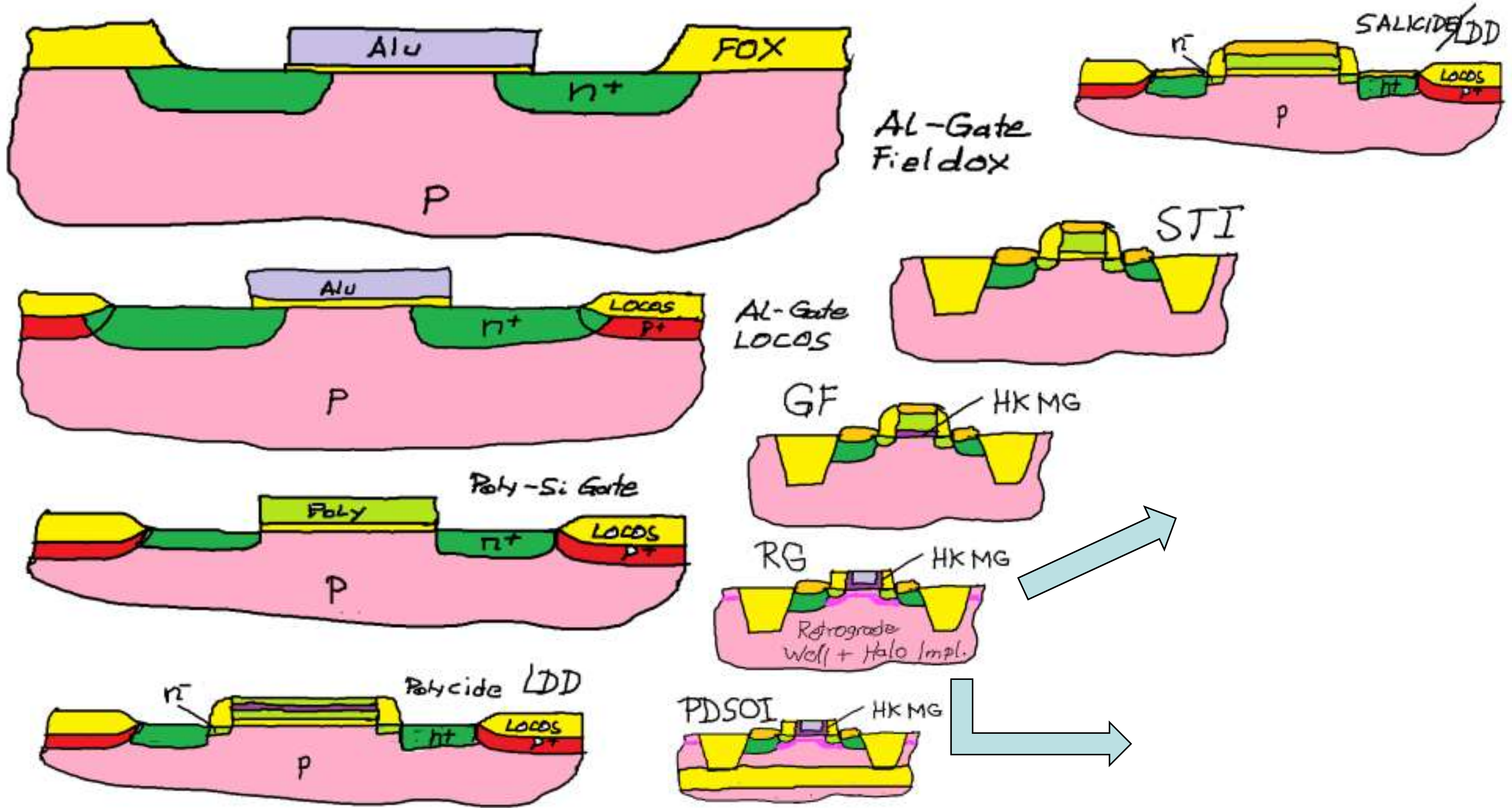
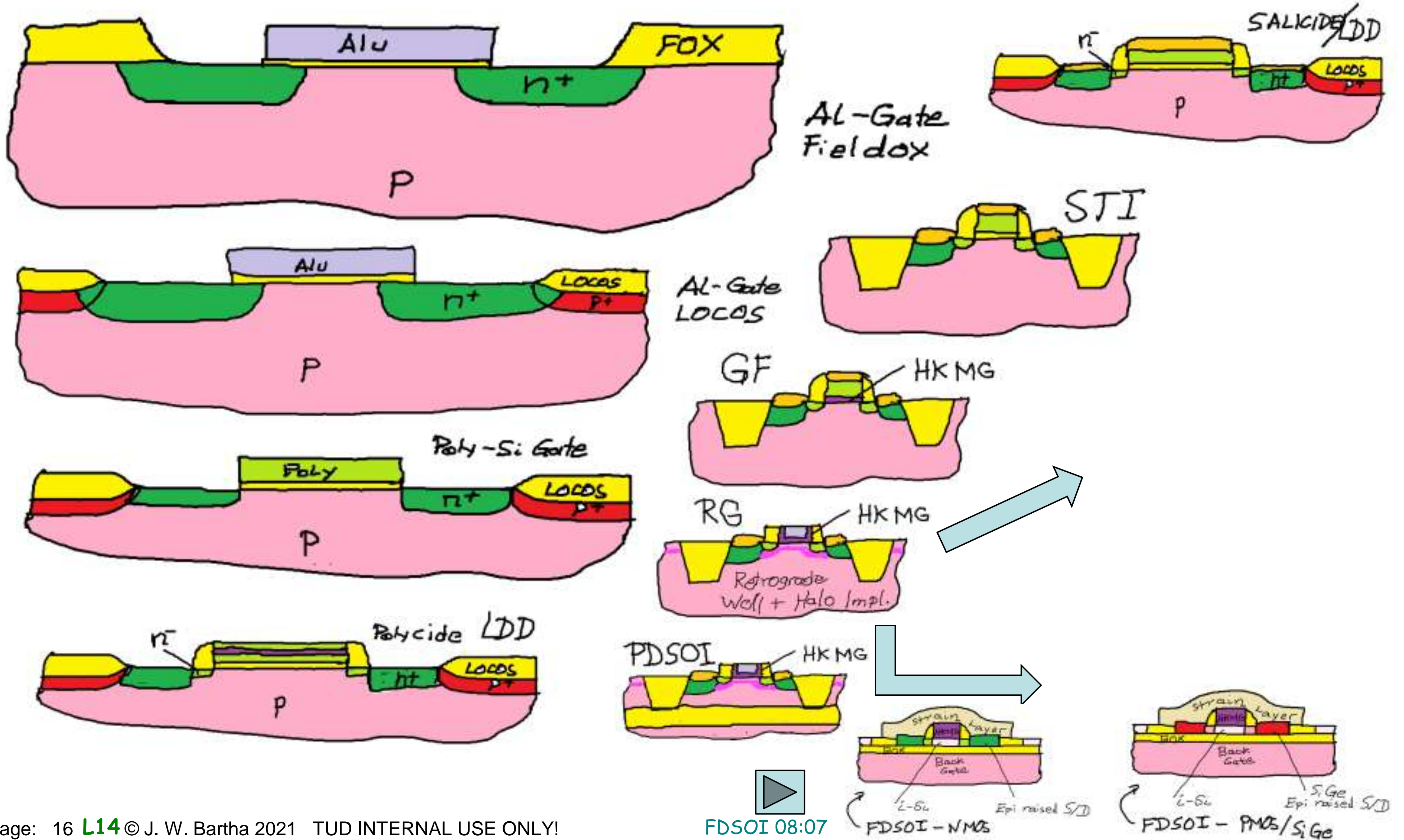

Alu
FOX
n+
P
Al-Gate
Fieldox
Alu
LOCOS
n+
p+
P
Al-Gate
LOCOS
Poly-Si Gate
Poly
n+
LOCOS
p+
P
Polycide LDD
n-
n+
LOCOS
p+
p
SALICIDE/LDD
n-
LOCOS
n+
p+
p
STI
GF
HKMG
RG
HKMG
Retrograde
Well + Halo Impl.



Alu
FOX
n+
P
Al-Gate
Fieldox
Alu
LOCOS
n+
p+
P
Al-Gate
LOCOS
Poly-Si Gate
Poly
n+
LOCOS
p+
P
n-
Polycide LDD
n+
LOCOS
p+
p
SALICIDE/LDD
n-
LOCOS
n+
p+
p
STI
GF
HKMG
RG
HKMG
Retrograde
Well + Halo Impl.
PDSOI
HKMG


Alu
FOX
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Al-Gate
Fieldox
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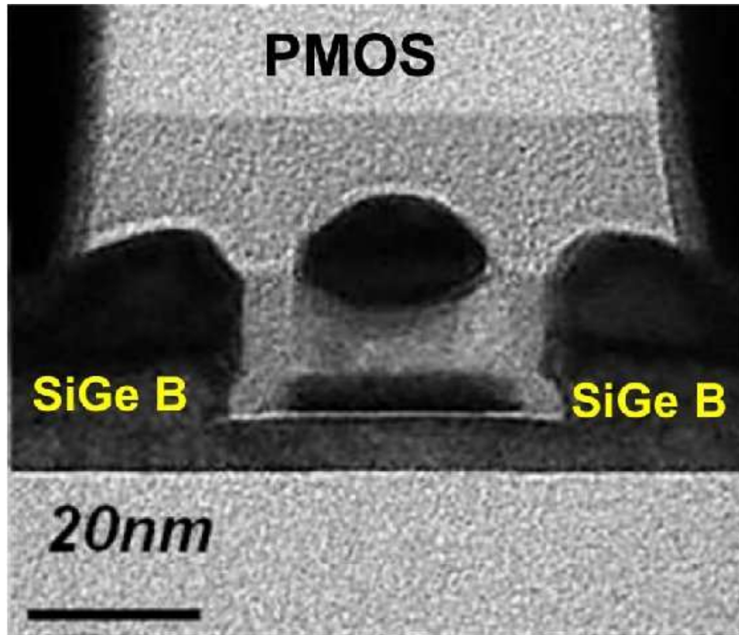
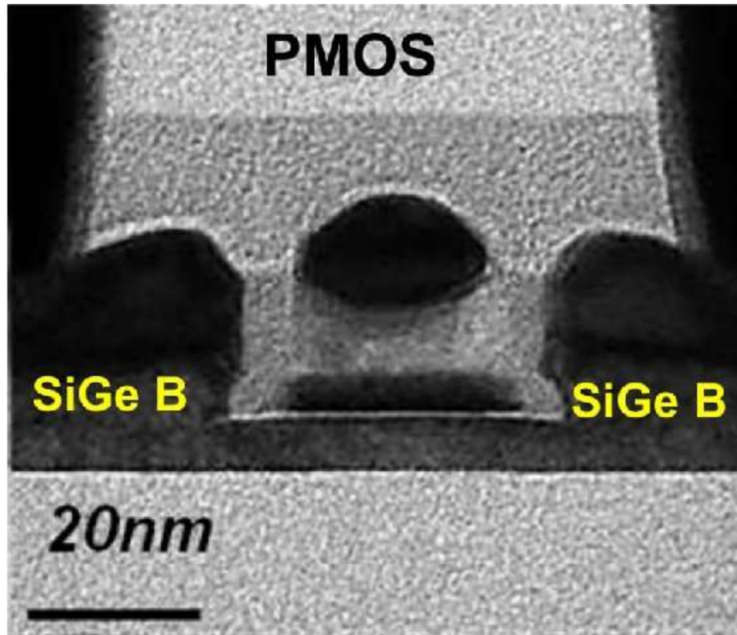
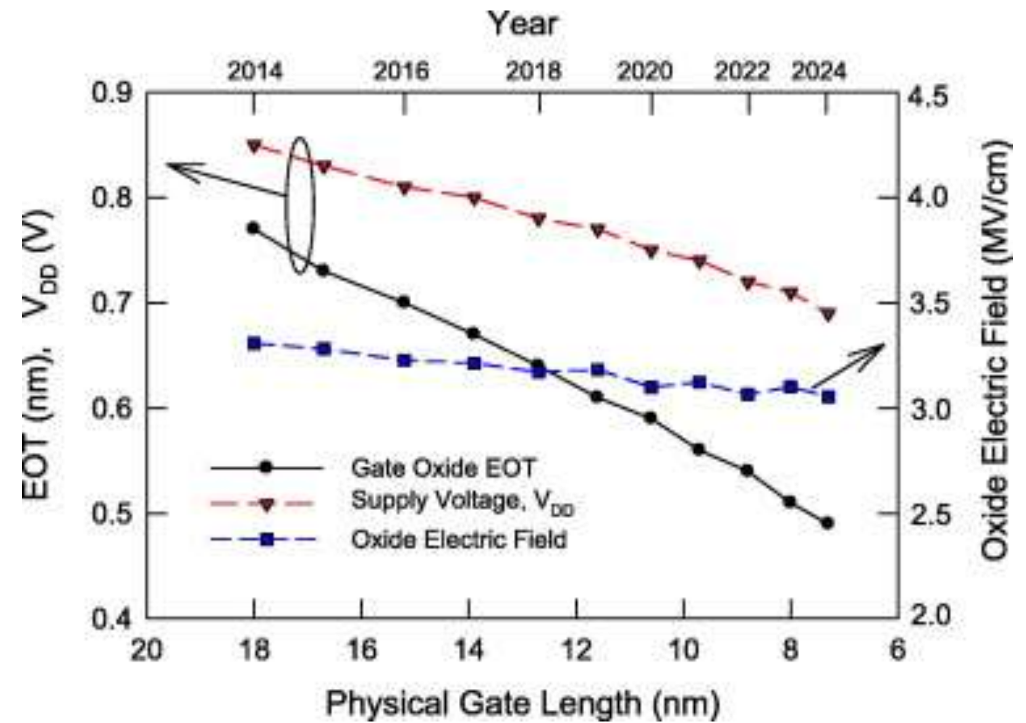
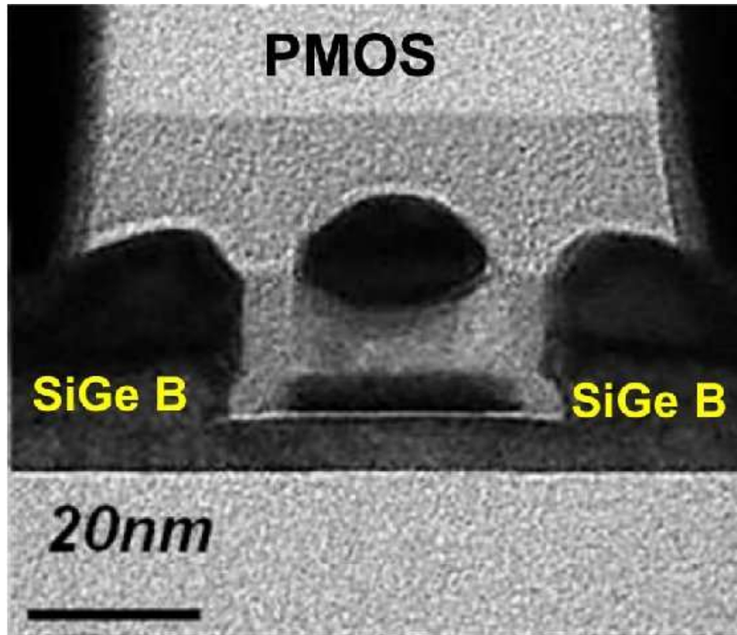
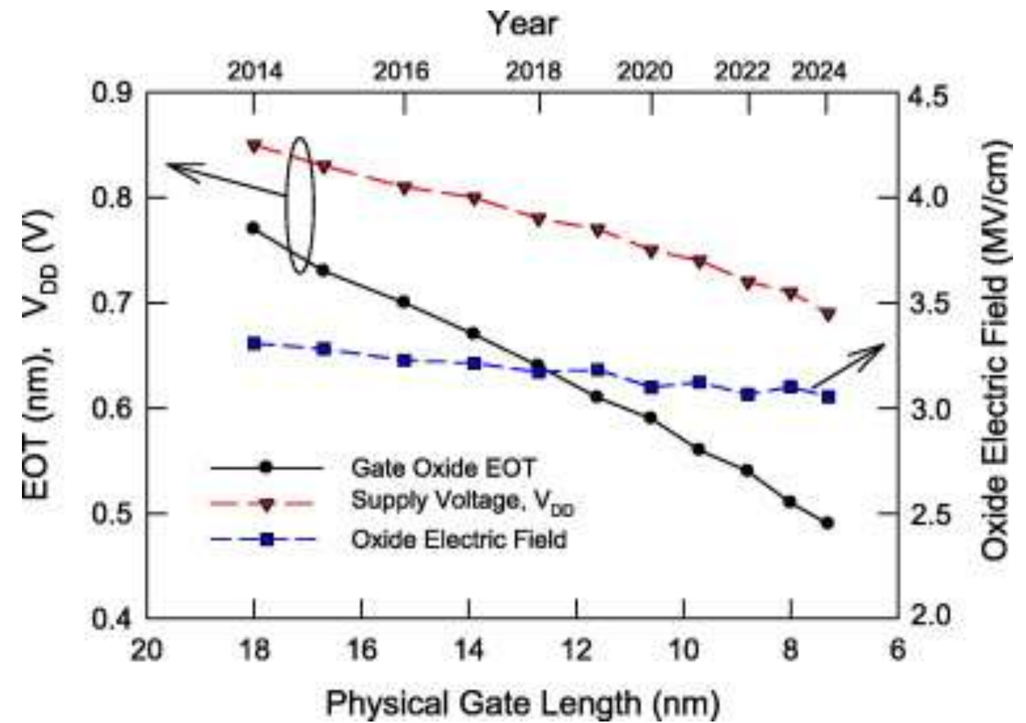
Al-Gate
LOCOS
Poly-Si Gate
Poly
n+
LOCOS
p+
P
n-
Polycide LDD
n+
LOCOS
p+
p
SALICIDE/LDD
n-
n+
LOCOS
p+
p
STI
GF
HKMG
RG
HKMG
Retrograde
Well + Halo Impl.
PDSOI
HKMG
Strain Layer
BOX
Back Gate
i-Si
Epi raised S/D
FDSOI – NMOS
Strain Layer
BOX
Back Gate
i-Si
SiGe
Epi raised S/D
FDSOI – PMOS/SiGe
FDSOI 08:07


PMOS
SiGe B
SiGe B
20nm


PMOS
SiGe B
SiGe B
20nm


Year
2014
2016
2018
2020
2022
2024
0.9
0.8
0.7
0.6
0.5
0.4
EOT (nm), V_DD (V)
4.5
4.0
3.5
3.0
2.5
2.0
Oxide Electric Field (MV/cm)
20
18
16
14
12
10
8
6
Physical Gate Length (nm)
Gate Oxide EOT
Supply Voltage, V_DD
Oxide Electric Field





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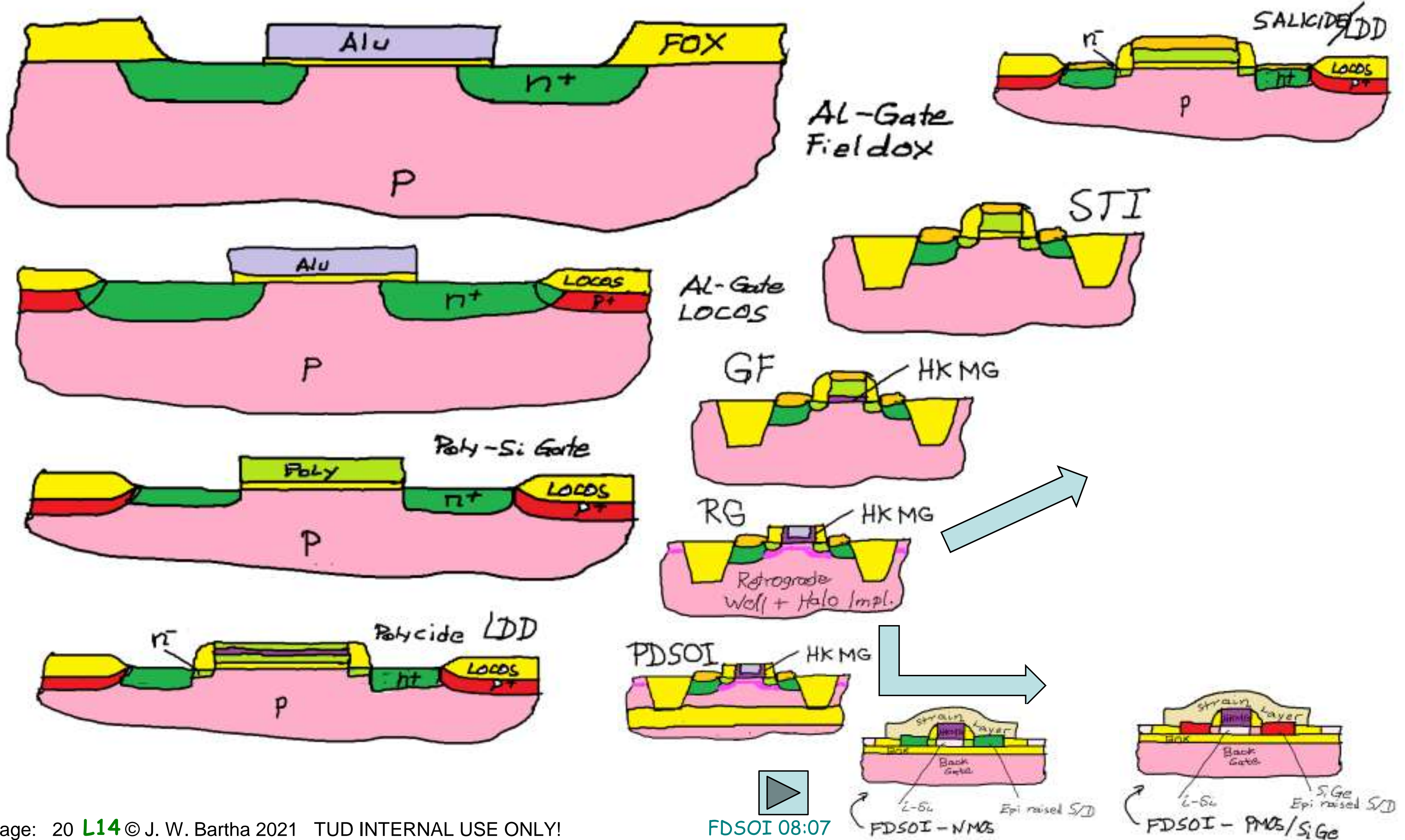
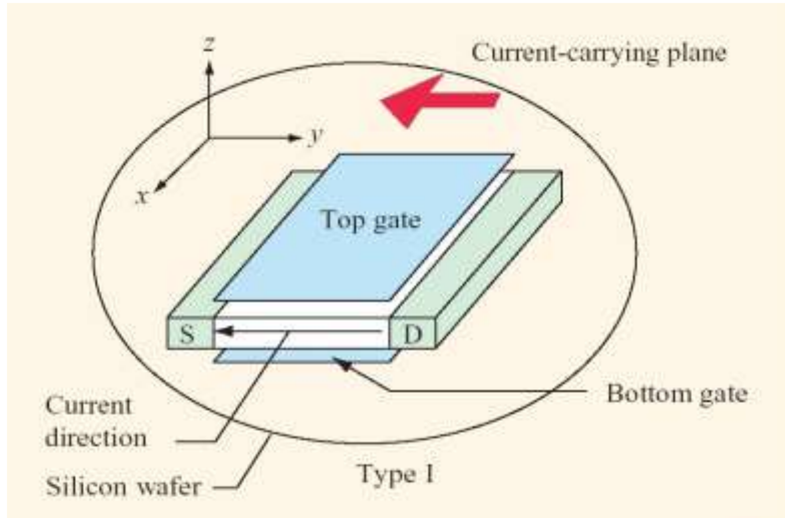
Further scaling approaches

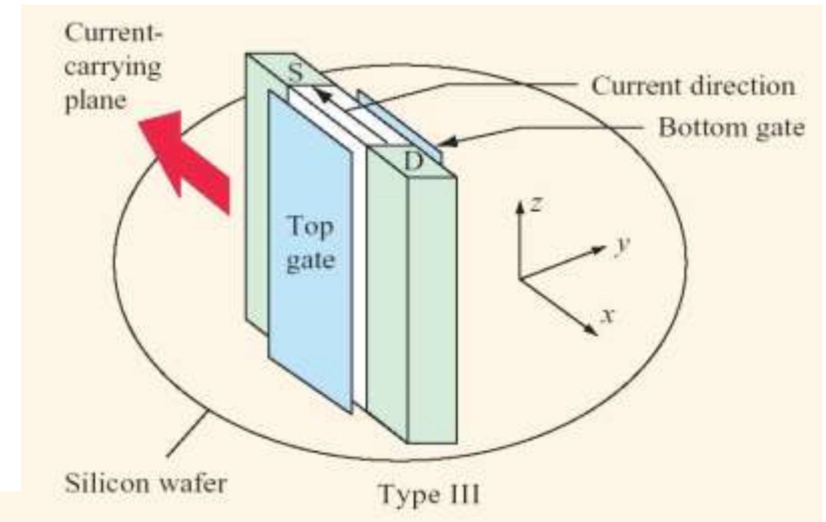


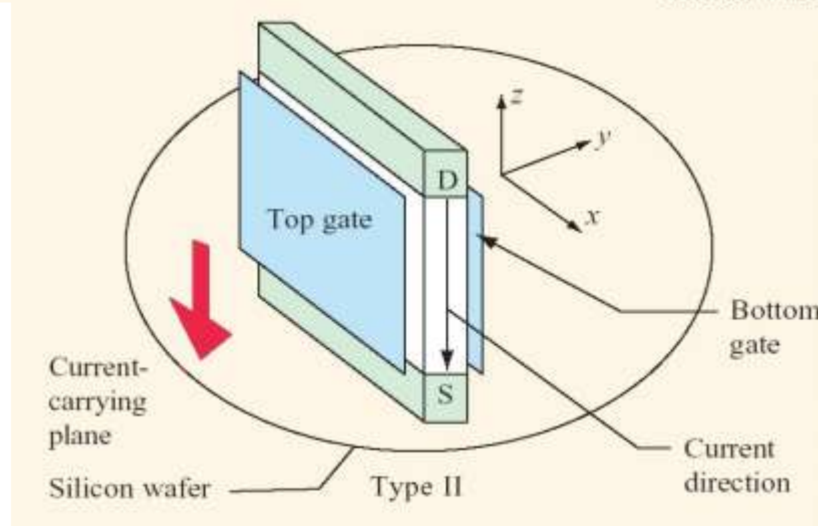
FDSOI 08:07

TECHNISCHE UNIVERSITÄT DRESDEN

3 basic types of double gate FET's

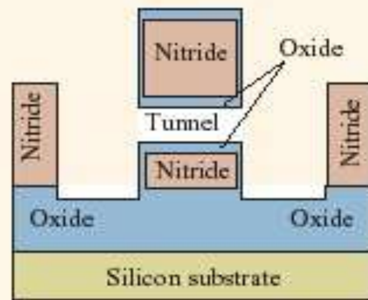


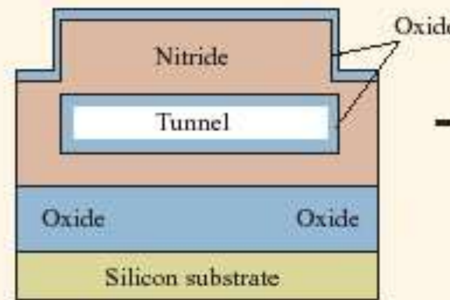




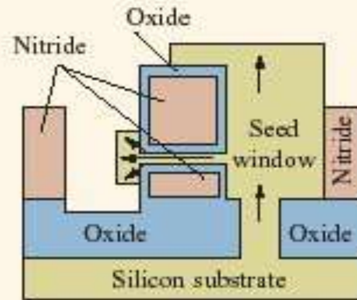
IBM JRD

Horizontal Double Gate MOSFET

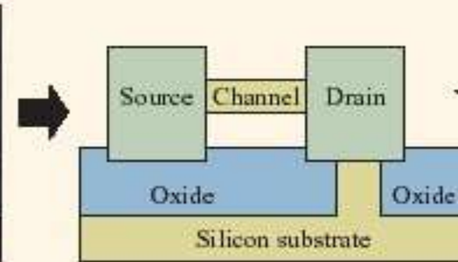




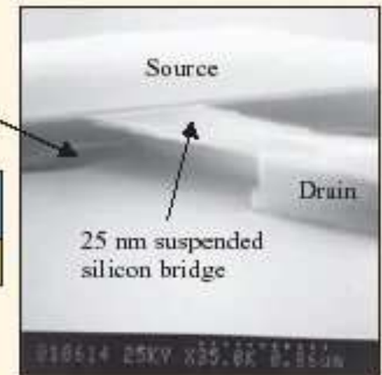
Form a tunnel by wet etch of dummy layer

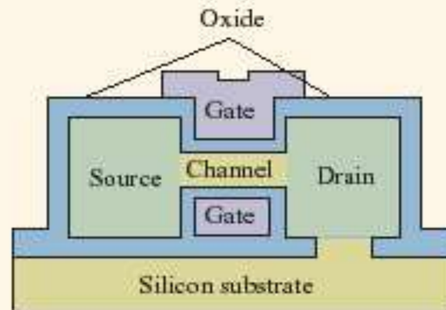


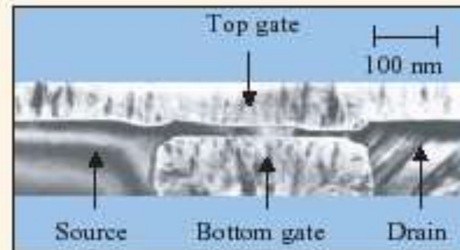
Grow selective epitaxial Si from one side of the tunnel

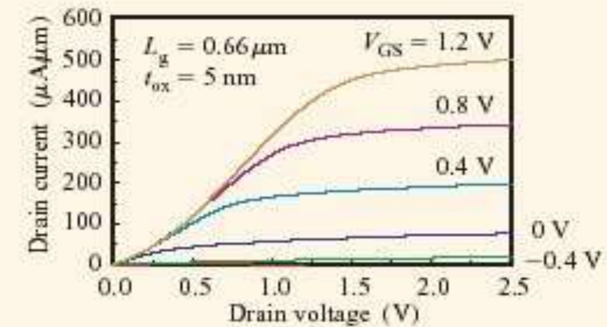


Remove nitride mold



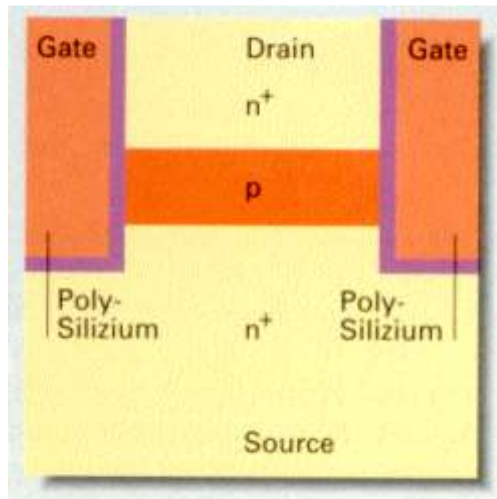




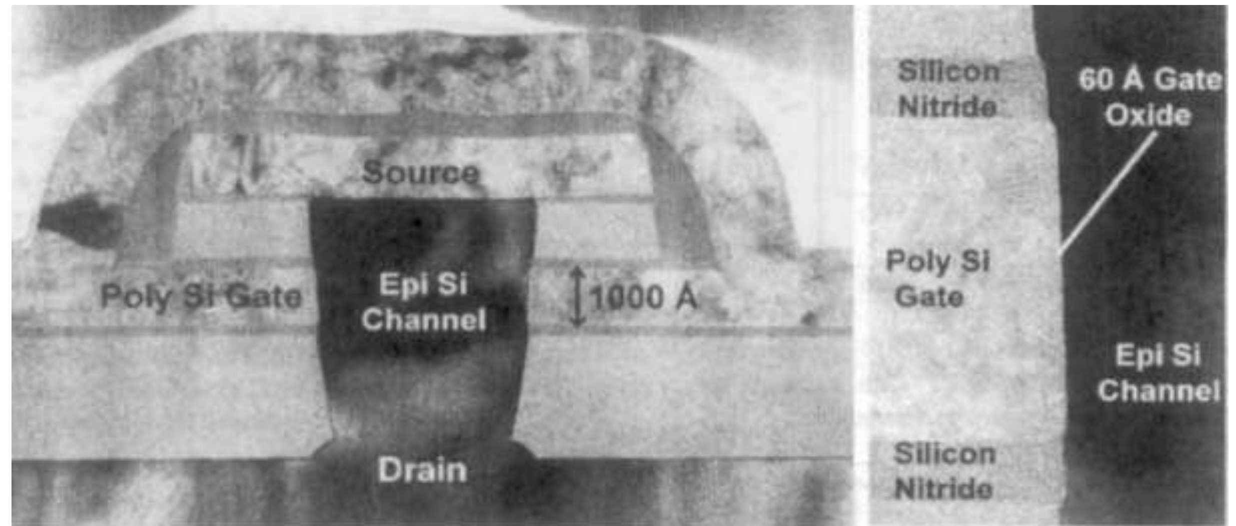


Wong, Chan & Taur, IBM 1997

Vertical structure: Definition of the Gate length via the thickness of an epitaxial layer



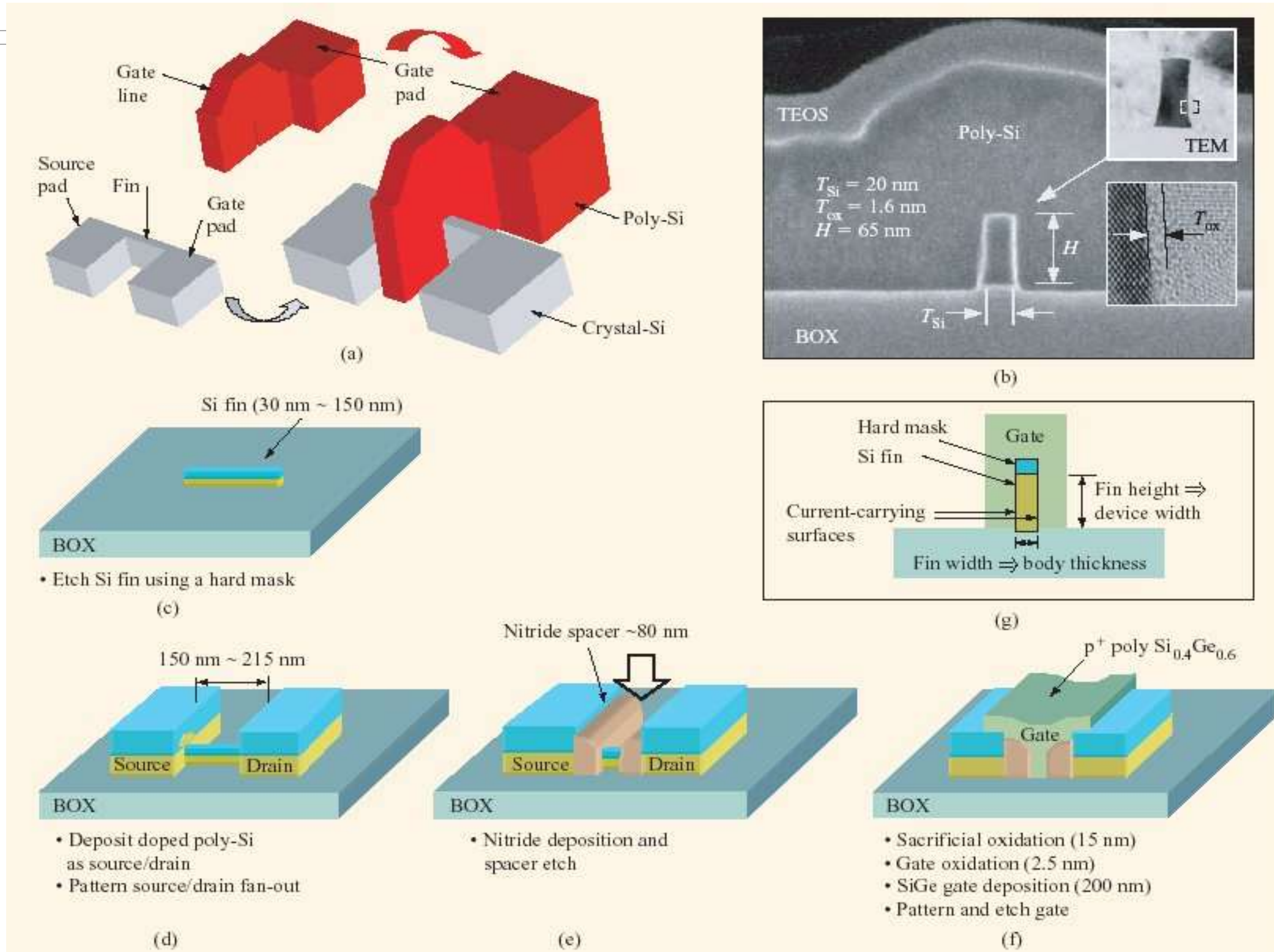
L. Risch, Infineon 96



Vertical Replacement-Gate (VRG) MOSFET

J.M. Hergenrother et al., Bell Labs, Lucent Techn. IEDM 99

FinFET double-gate Transistor



Kedzierski et. al IBM 2001

Benefits of FinFET

$$I_D = \frac{\mu \varepsilon_0 \varepsilon_r}{2 d_{ox}} \frac{W}{L} (V_G - V_T)^2$$

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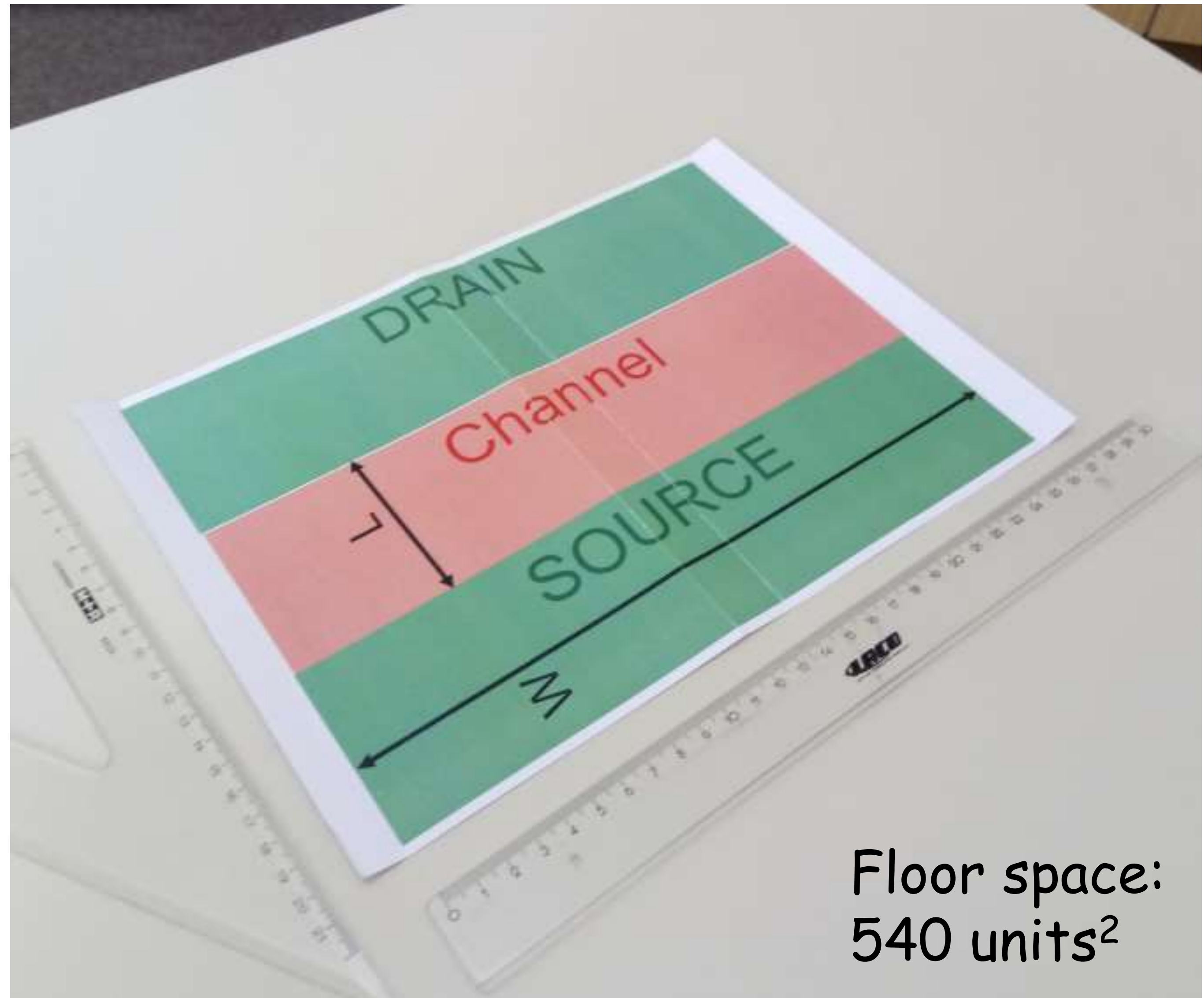

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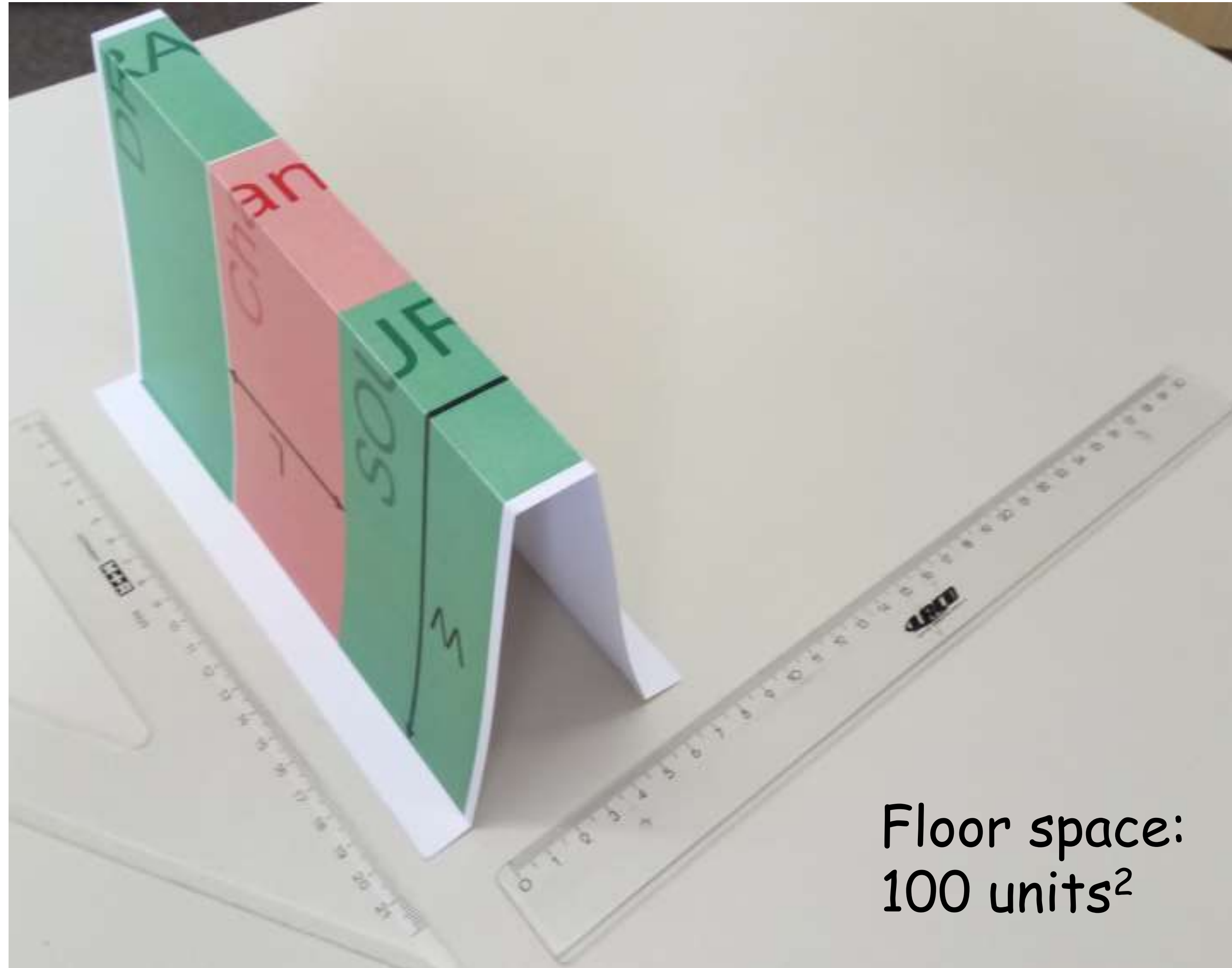
Significantly less floor space and much better electrostatic control of the body



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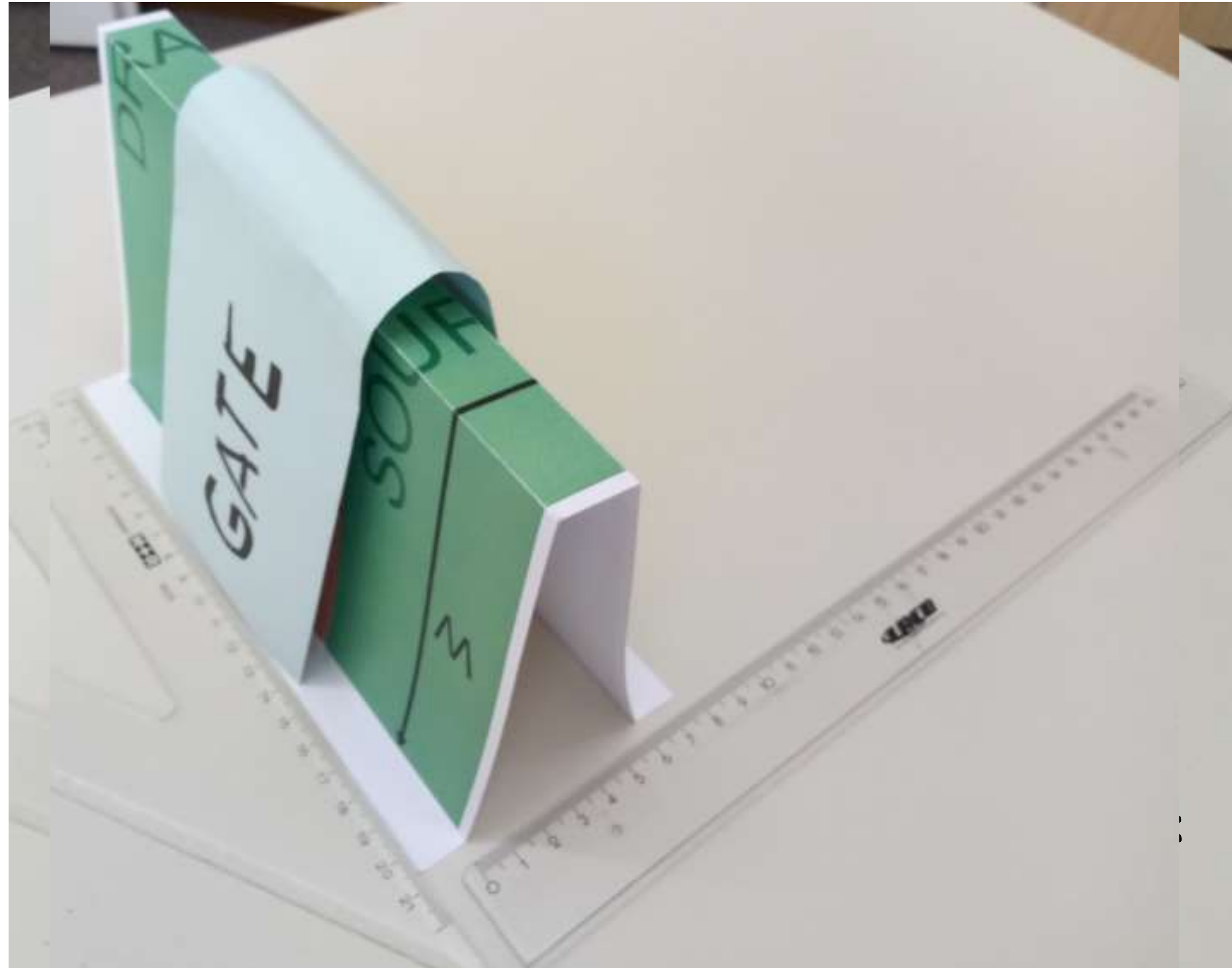

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"Equivalent Scaling Process Technologies Timing"

New for 2009

[PIDS/FEP – "Simplified Transistor Roadmap"] - [Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs (ENIAC Graphic)]

Gate stack

poly
SiON

metal
high k

['09: 2 co's (1st co: 2007)]

metal
high k [II, etc]

['11: 2 co's (1st co: 2009)]

Electrostatic control

bulk

PDSOI

FDSOI

MuGFET
MuCFET

Channel material

stressors

+ high μ SiGe materials

+ III/V High μ Alternative Channel Mat'ls

2009 ITWG Table Timing: 2007 2010 2013 2016 2019]

Source: 2009 ITRS - Exec. Summary Fig 7c
[Orig. Source: ITRS, European Nanoelectronics Initiative Advisory Council] (ENIAC)

MuGFET = Multiple gate FET
MuCFET = Multiple channel FET

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Gate stack
poly / SiON → metal / high k → metal / high k [II, etc]
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Electrostatic control
bulk → MuGFET MuCFET
PDSOI → FDSOI → MuGFET MuCFET

Channel material
stressors → + high μ SiGe materials
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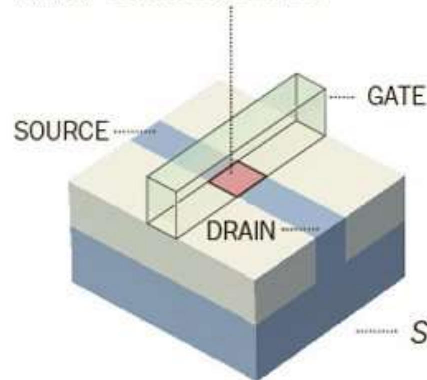
The New York Times May 5, 2011

New Transistor Grows in the Third Dimension

The new Intel transistor provides higher performance by increasing the conductive area between the source and drain regions of the chip, allowing more current to flow through.

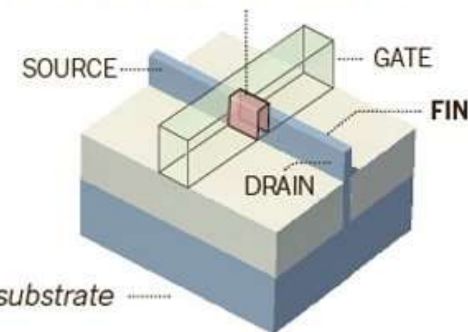
TRADITIONAL TRANSISTOR

Planar **conductive area**



NEW INTEL TRANSISTOR

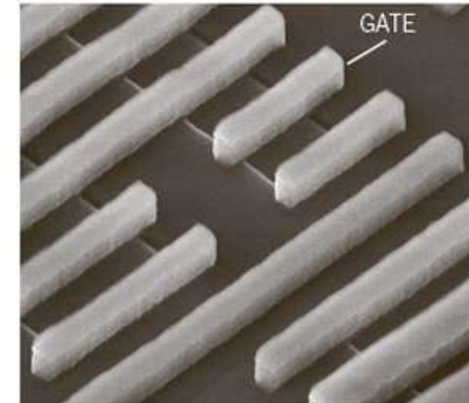
Conductive area is expanded on **three sides of a raised fin**



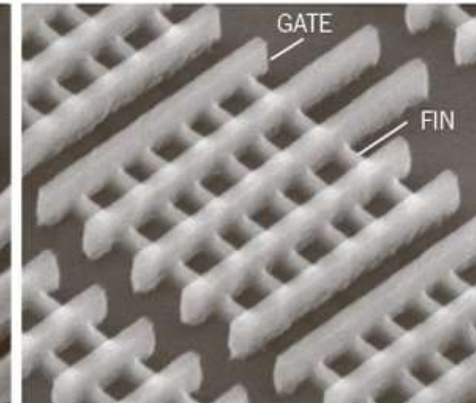
Silicon substrate

The new transistor with its raised **fin** requires a smaller footprint, allowing more of them to fit in a computer chip. The new design can also reduce power consumption, yielding better battery life on devices.

Traditional planar transistor

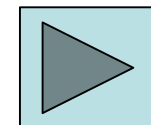


Intel Tri-Gate transistor



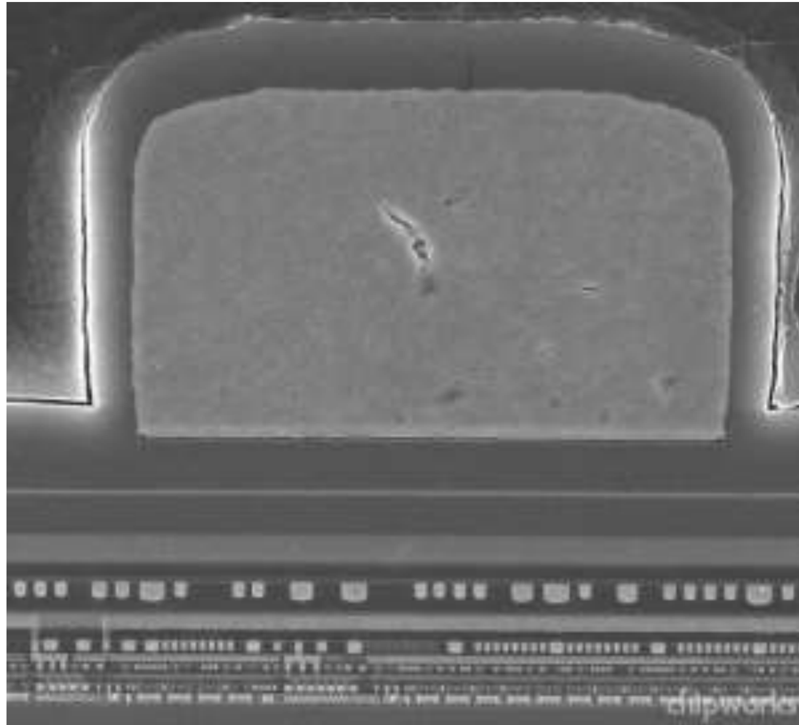
Source: Intel

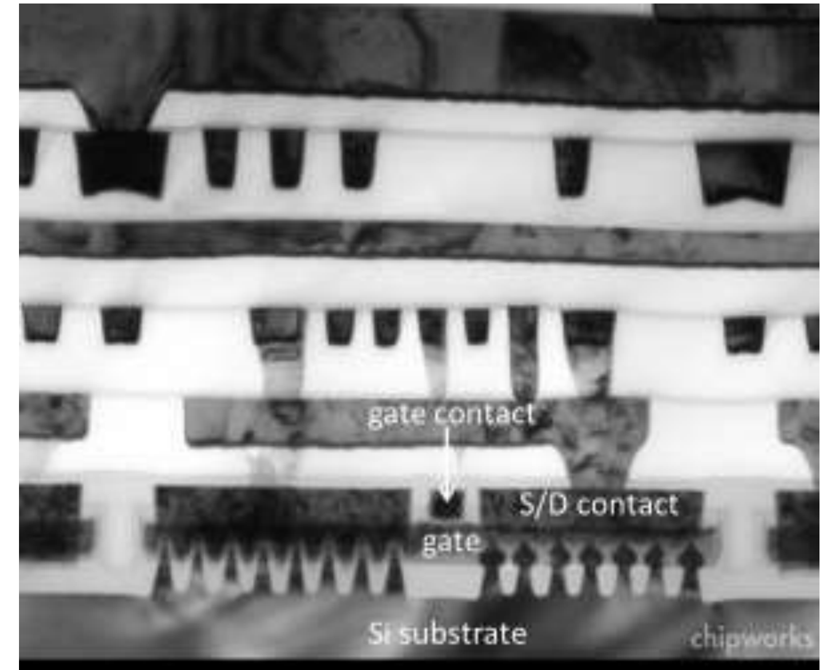
THE NEW YORK TIMES

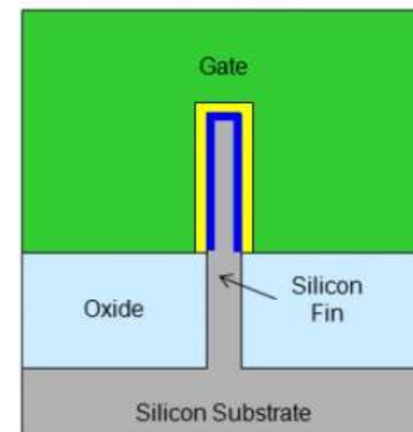


P FinFET 03:47

http://chipworksrealchips.blogspot.com/2012/04/intels-22-nm-trigate-transistors.html







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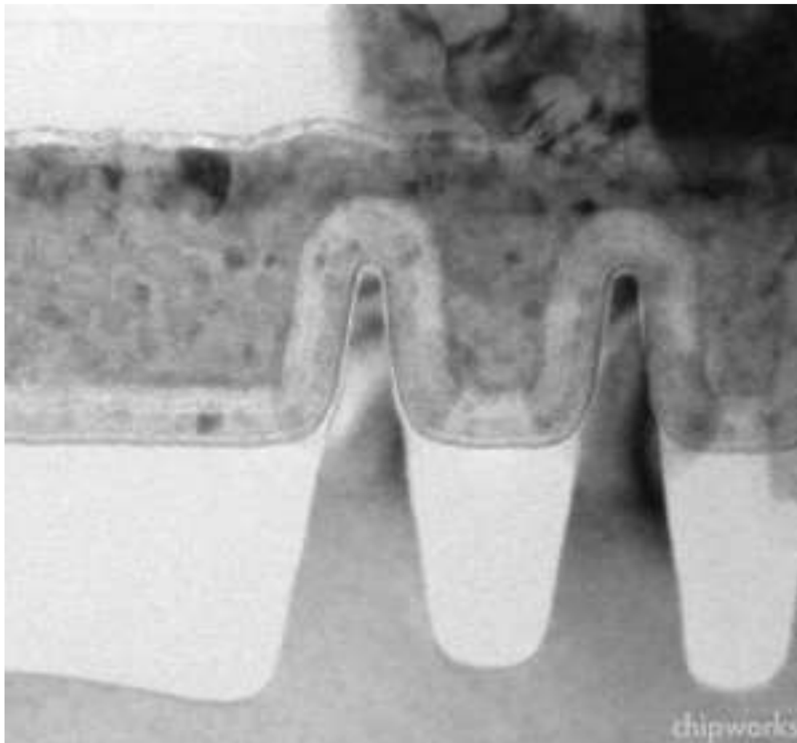
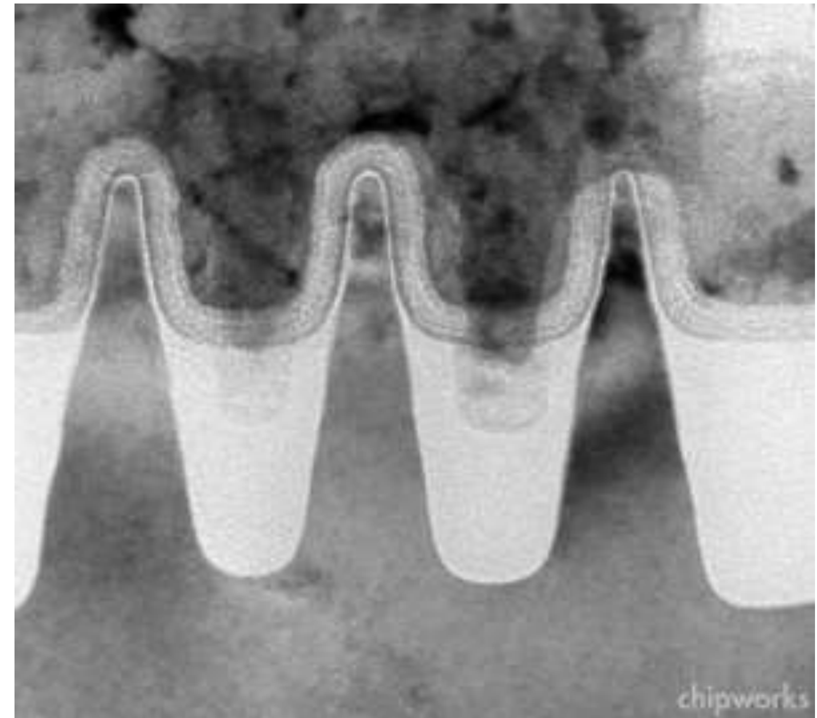
PMOS

NMOS





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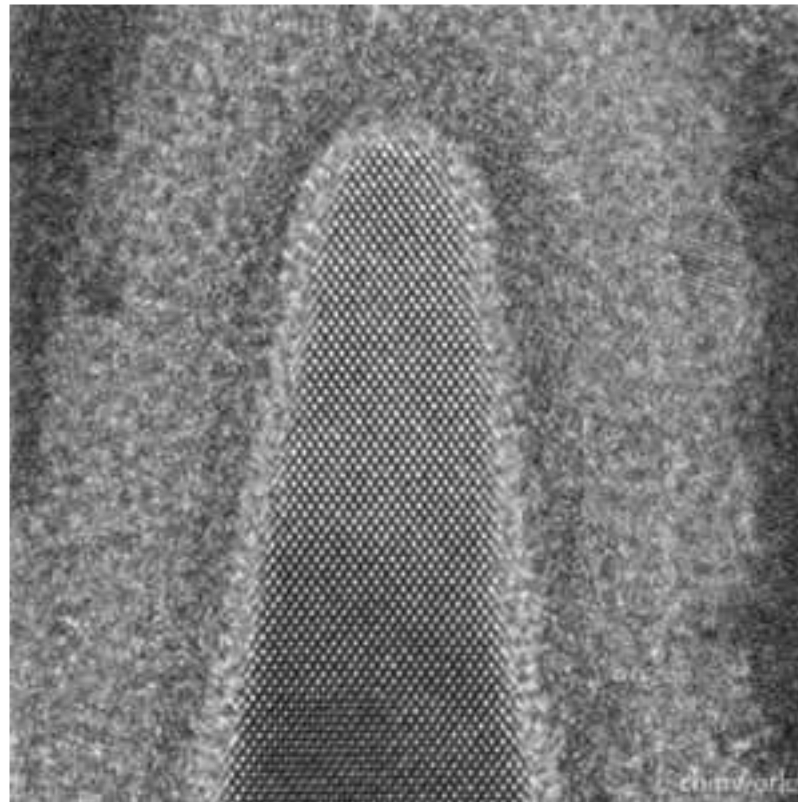

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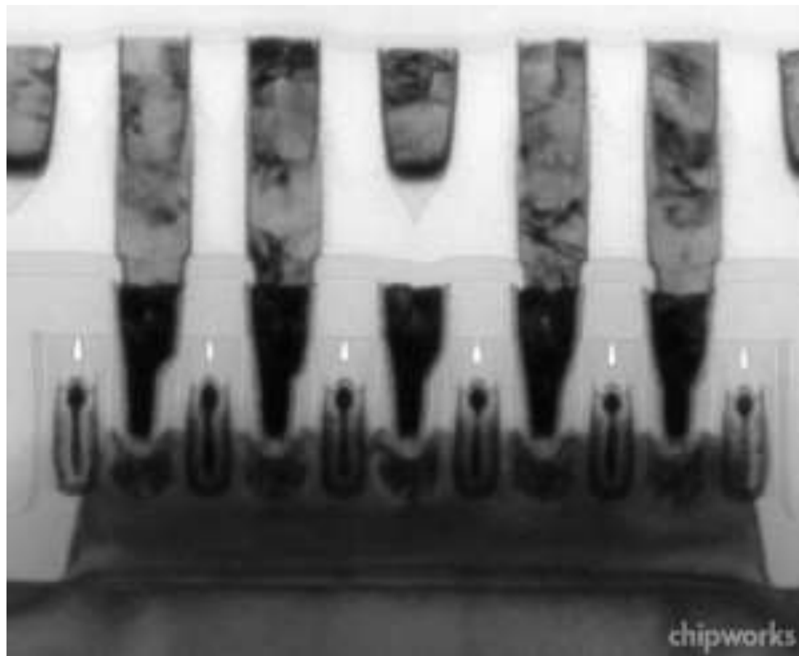

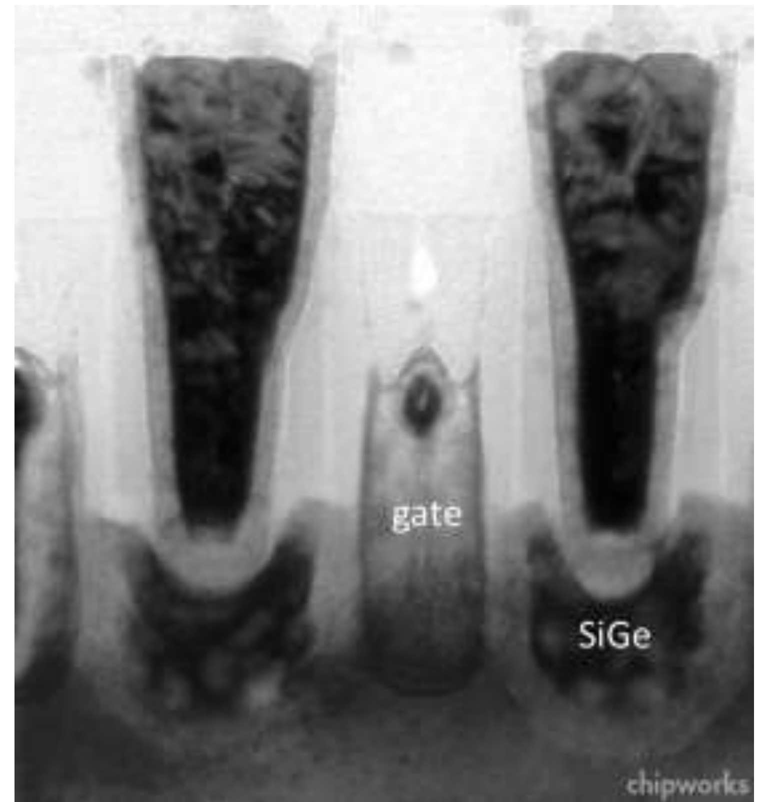

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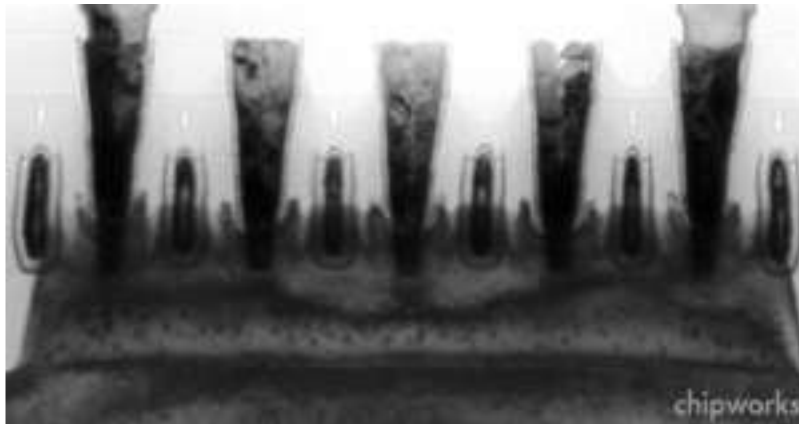
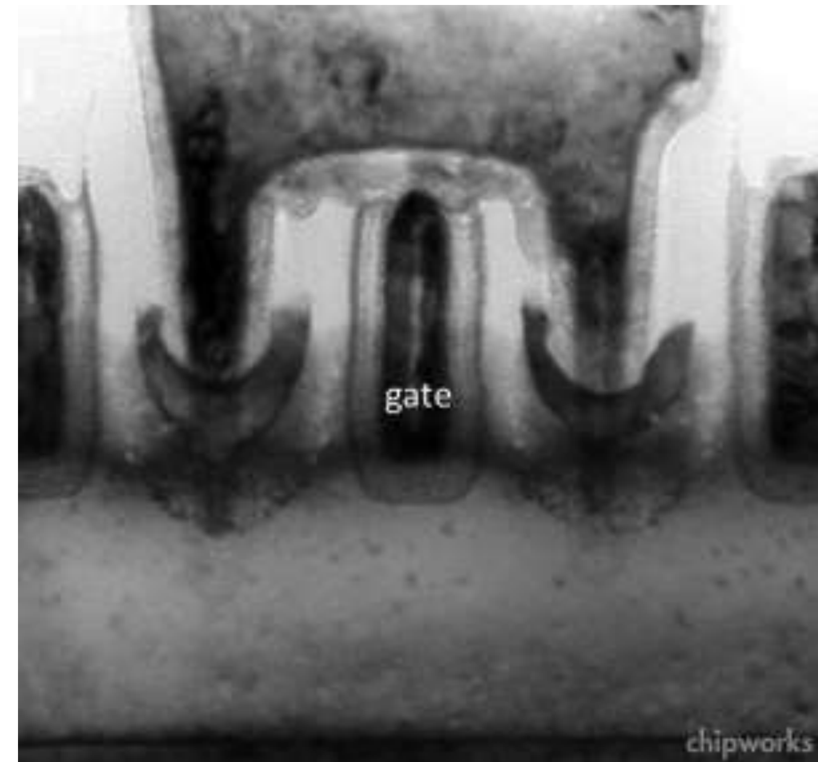
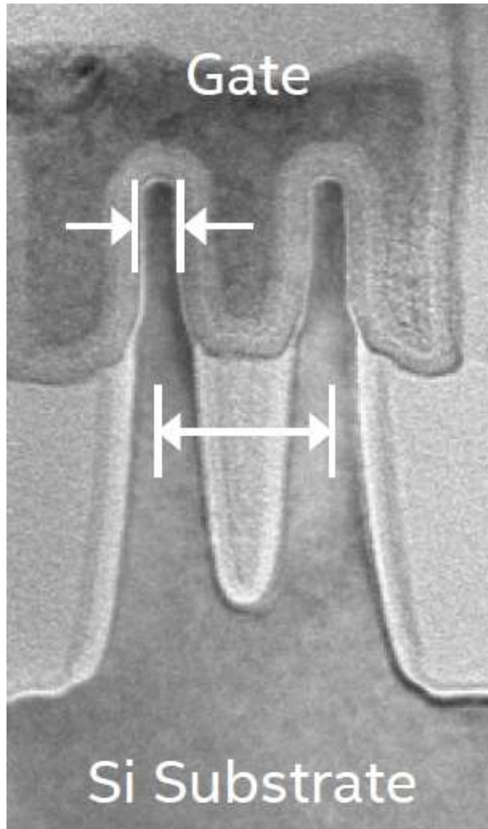




What's next?



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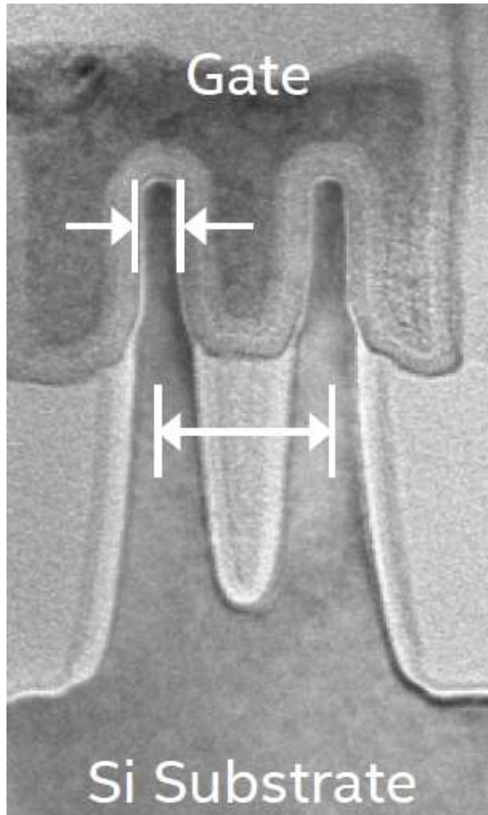
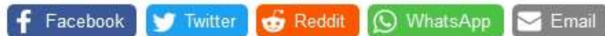


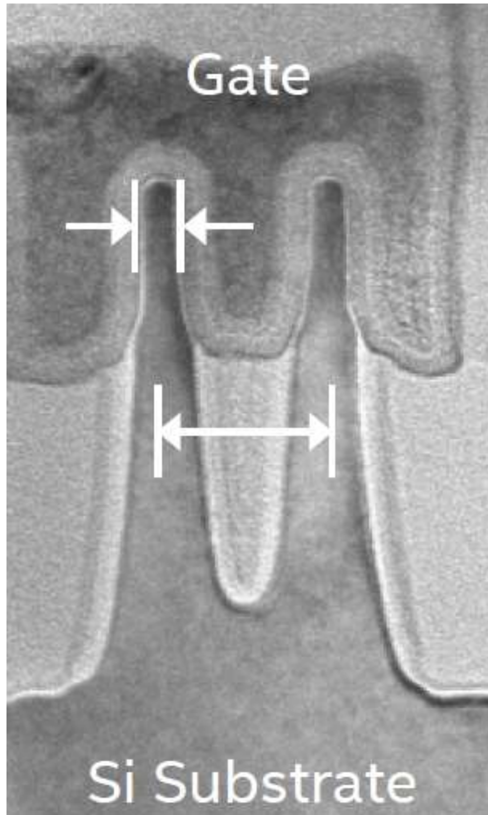
Samsung has created its first 3nm GAAFET prototypes - Transistors beyond FinFET

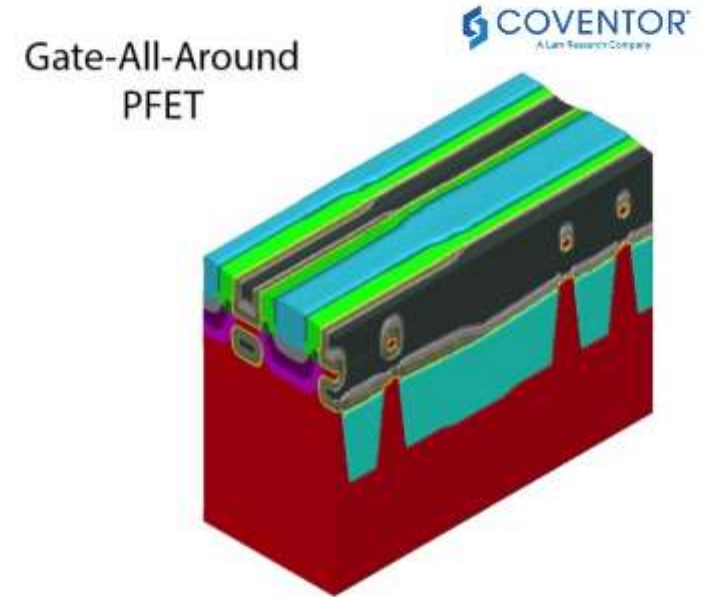
Should TSMC be worried?



Published: 4th January 2020 | **Source:** Maeil Economy - Via Tom's Hardware | **Author:** Mark Campbell

What's next?





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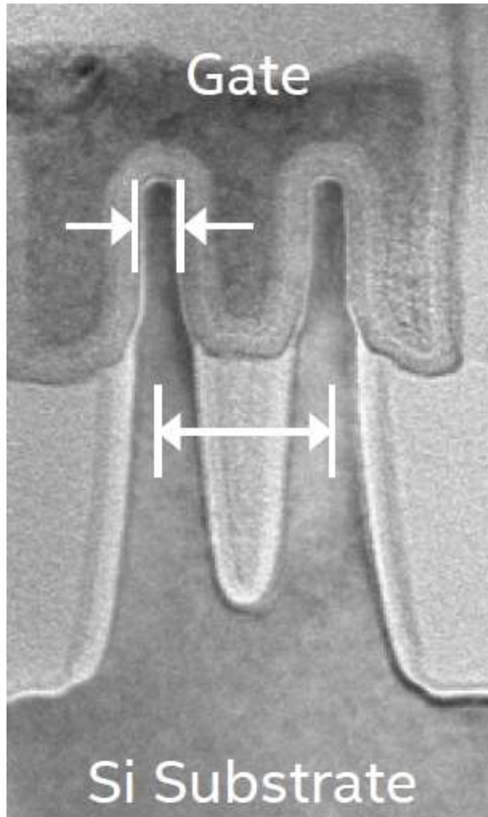
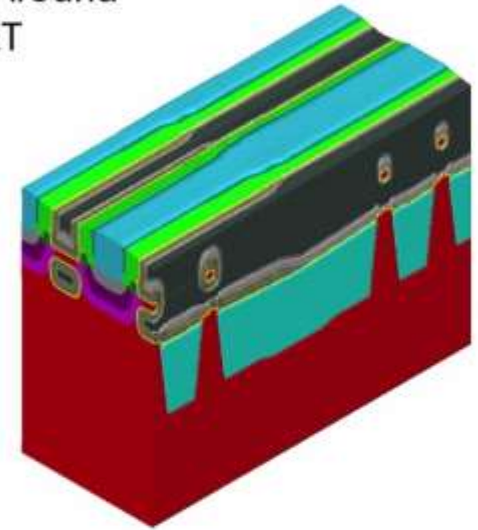


From Fin
via Gate all arround
to Nanowires resp.
Nanosheets



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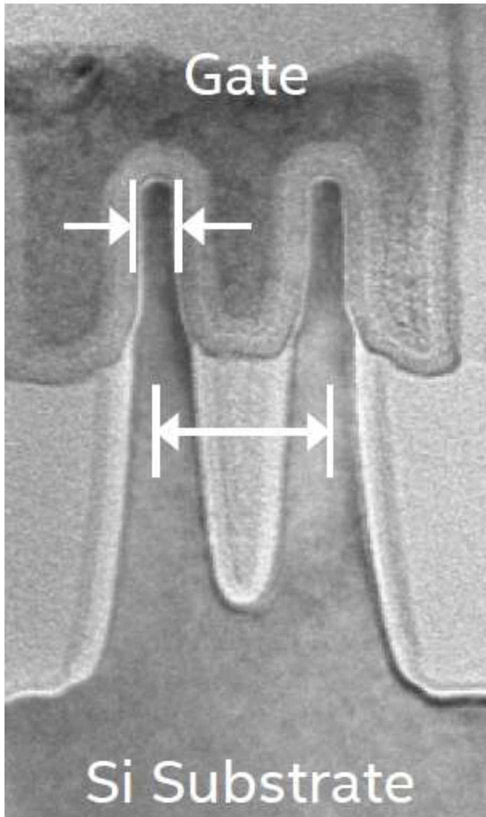

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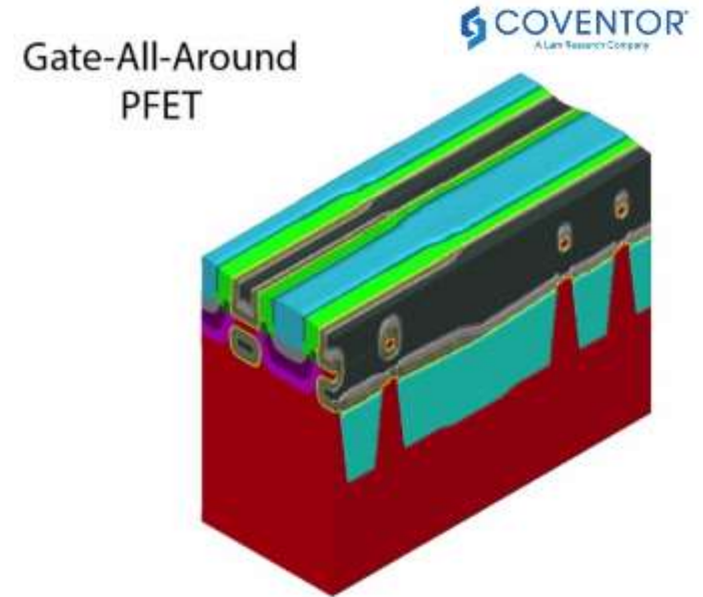

Samsung has created its first 3nm GAAFET prototypes - Tra

Should TSMC be worried?

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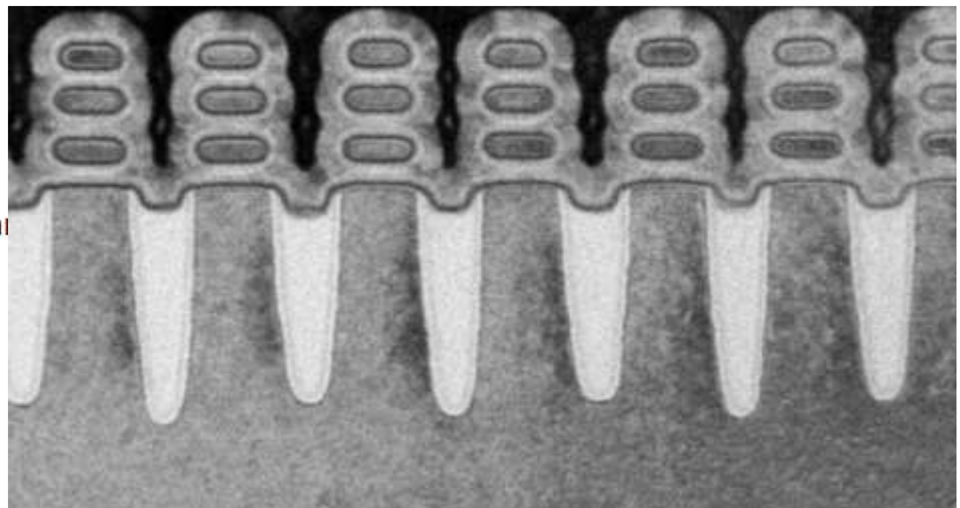


Alu
FOX
n+
P
Al-Gate Fieldox

SALICIDE LDD
n-
LOCOS
n+
p+
p

Alu
LOCOS
n+
p+
P
Al-Gate LOCOS

STI

GF
HKMG

Poly-Si Gate
Poly
LOCOS
n+
p+
P

RG
HKMG
Retrograde Well + Halo Impl.

Polycide LDD
n-
LOCOS
n+
p+
p

PDSOI
HKMG

Strain Layer
BOX
Back Gate
i-Si
Epi raised S/D
FDSOI – NMOS

Strain Layer
BOX
Back Gate
i-Si
SiGe Epi raised S/D
FDSOI – PMOS/SiGe

FDSOI 8:07

Al-Gate Fieldox

Alu, FOX, n+, P

Al-Gate LOCOS

Alu, LOCOS, n+, p+, P

Poly-Si Gate

Poly, LOCOS, n+, p+, P

Polycide LDD

n⁻, n+, LOCOS, p+, p

SALICIDE/LDD

n⁻, n+, LOCOS, p+, p

STI

GF HKMG

RG HKMG

Retrograde Well + Halo Impl.

PDSOI HKMG

HKMG, S/D, Field-ox

FINFET

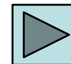
Strain Layer, BOX, Back Gate, i-Si, Epi raised S/D

FDSOI – NMOS

Strain Layer, BOX, Back Gate, i-Si, SiGe Epi raised S/D

FDSOI – PMOS/SiGe

FDSOI 8:07



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HK MG
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Field-ox
FINFET

Poly-Si Gate
Poly
n+
LOCOS
p+
P

RG
HK MG
Retrograde
Well + Halo Impl.

GAAFET

n-
Polycide LDD
n+
LOCOS
p+
p

PDSOI
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Strain Layer
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FDSOI – NMOS

Strain Layer
BOX
Back Gate
i-Si
SiGe
Epi raised S/D
FDSOI – PMOS/SiGe

FDSOI 8:07

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Chaper 5 - Summary: FEOL Scaling & Limits

- Sub threshold slope does not scale
    - Degrades I_{on} / I_{off}
- DIBL = Drain induced Barrier Lowering
    - Shallow Junctions
    - Retrograde Wells
    - Halo Implants
    - SOI = Silicon on Insulator -> FDSOI
    - or FinFET resp. GAA FET
- Gate Leakage
    - High k Dielectrics
    - Poly Depletion > Metal Gate
- Mobility Engineering
    - Stress Layers
    - SiGe FETS
- V_t Variability -> Intrinsic Si in FD FETs

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Continue

"SCT_SS21_14.03" 18:22

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TECHNISCHE UNIVERSITÄT DRESDEN

Outline

SC-Basics

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
   1. MOS Structure, MOS Capacitor
   2. Structure of a MOSFET
   3. I/V behavior
2. Circuits in Metal-Gate FET Technology
   1. Process sequence of N-MOSFET in Metal Gate
   2. From inverter to memory cell
   3. SRAM in NMOS Metal Gate
   4. The threshold voltage of the MOSFET
      1. Parasitic FET
      2. Enhancement/Depletion Transistor
      3. N-MOS Logic by E/D Transitors
      4. Process sequence of the N-MOS E/D Process
3. Self aligned Process
   1. Metal Gate -> Si Gate
   2. Channel-Stop & LOCOS Technology
      1. Example: Process flow of E/D SiGate LOCOS Inverter
      2. LOCOS Variation
      3. Shallow Trench Isolation
   3. Lightly doped drain
   4. SALICIDE
   5. Self Aligned Contacts (SAC)
   6. Resist trimming
4. Transition to CMOS Technology
   1. MOS Transistor Types
   2. CMOS Inverter
      1. Consideration NMOS E/D Inverter
      2. Comparison CMOS Inverter
   3. CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
   1. Scaling
      1. Challenges
      2. Material Equivalent Scaling
      3. Further Concepts

http://www.computerhistory.org/siliconengine/timeline/

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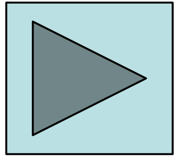
An outlook:



Future 14:29

3D Stacking
L4 Cache **1GB HBM** on-chip
L4 Cache **4GB HBM** on-chip
Mobile Frequency Wall ~4GHz
Photonics Laser

2021 **2022** **2023** **2024** **2025** **2026** **2028** **2029** **2030**

3nm TSMC / SAMSUNG 7nm Intel
3nm+ TSMC 7nm+ Intel
7nm++ Intel
2.5nm TSMC / SAMSUNG 5nm Intel
2nm TSMC / SAMSUNG 5nm+ Intel
1.5nm TSMC / SAMSUNG 3nm Intel
1nm TSMC / SAMSUNG 3nm Intel+

GAAFET aka Nanowire Transistor replaces FinFET
MBCFET Nanosheet Transistor replaces GAAFET
Stacked Carbon Nanotube Transistor
Stacked Carbon Nanotube + Photonics

FinFET GAAFET nanowire MBCFET nanosheet

Hybrid Scaling ERA

25:42 / 26:44

#Transistors #Moore #Quantum
The World After Silicon - From Vacuum Tubes to QUANTUM

Thank you very much for your attention!

All the very best for the upcomming exams!

Thank you very much for your attention!

All the very best for the upcomming exams!

Relaxing vaccation!

TECHNISCHE UNIVERSITÄT DRESDEN