

Module SCT

Wrap-Up for preparation of the exam Prof. Dr. Johann W. Bartha

Inst. f. Halbleiter und Mikrosystemtechnik
Technische Universität Dresden

Summer Semester 2021

Start lecture here



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Lecture Semiconductor Technology I,
Prof. Dr. J. W. Bartha

Content

- 1. Introduction**
- 2. Silicon as Substrate Material**
 - 2.1 The Silicon Crystal
 - 2.2 Crystal Defects
 - 2.3 Conductivity and Doping
 - 2.4 Si as the most important material of Microelectronics
 - 2.4.1. Fabrication of pure Silicon
 - 2.4.2. Si Wafer Fabrication
- 3. The Oxidation of Silicon**
 - 3.1. Growth model after Deal and Grove
 - 3.2. Dependency on Process parameters
 - 3.3. Oxidation technique
 - 3.4. Stress and Oxidation
- 4. Lithography**
 - 4.1. Process sequence
 - 4.1.1. Negative Resist
 - 4.1.2. Positive Resist
 - 4.2. Multi-Layer Resists
 - 4.3. Image Reversal
 - 4.4. Pattern Enhancement
- 5. Doping**
 - 5.1. Diffusion
 - 5.1.1. ...from an infinite Source
 - 5.1.2. ...from a finite Source
 - 5.1.3. Two step Diffusion
 - 5.1.4. Further Effects
 - 5.1.5. Practical Realization
 - 5.2. Implantation
 - 5.2.1. Projected Range
 - 5.2.2. Implantation - Masks
 - 5.2.3. Channeling
 - 5.2.4. Further Effects
 - 5.2.5. Healing and Activation
 - 5.2.6. Implantation Systems

- 6. Epitaxy**
 - 6.1. Gas Phase Epitaxy
 - 6.1.1. Uniformity
 - 6.1.2. Reaction Kinetics
 - 6.1.3. Monocrystalline vs. Polycrystalline
 - 6.1.4. Pattern Displacement
 - 6.1.5. Doping
 - 6.1.6. Epi-Reactor + Process
 - 6.1.7. Selective Epitaxy
 - 6.2. Molecular Beam Epitaxy
- 7. Chemical Vapor Deposition CVD**
 - 7.1. Poly-Silizium
 - 7.2. Siliconoxide SiO_2
 - 7.3. Silicon nitride Si_3N_4
 - 7.4. PECVD
 - 7.5. Tungsten W
- 8. Plasma based Deposition and Etch**
 - 8.1. Plasma technology
 - 8.1.1. Basic Processes in a Plasma
 - 8.1.2. Energy Absorption by the Electric Field
 - 8.1.3. Plasma Properties
 - 8.1.4. Plasma Generation
 - 8.2. Sputter Deposition
 - 8.2.1. Sputter Deposition of Alloys
 - 8.2.2. Reactive Sputtering
 - 8.2.3. Magnetron Sputtering
 - 8.2.4. Bias-Sputtering
 - 8.3. Plasma induced Etching
 - 8.3.1. Sputter-Etching
 - 8.3.2. Plasma Induced Chemical Etching
 - 8.3.3. Reactive Ion Etching
 - 8.3.4. Process Parameters
 - 8.3.5. Plasmatools

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7.6 ALD

0. Introduction/ Lab organization/DMA /SCT1/Motivation
1. Process integration
 - 1.MOS Structure, MOS Capacitor
 - 2.Structure of a MOSFET
 - 3.I/V behavior
2. Circuits in Metal-Gate FET Technology
 - 1.Process sequence of N-MOSFET in Metal Gate
 - 2.From inverter to memory cell
 - 3.SRAM in NMOS Metal Gate
 - 4.The threshold voltage of the MOSFET
 - 1.Parasitic FET
 - 2.Enhancement/Depletion Transistor
 - 3.N-MOS Logic by E/D Transistors
 - 4.Process sequence of the N-MOS E/D Process
3. Self aligned Process
 - 1.Metal Gate -> Si Gate
 2. Channel-Stop & LOCOS Technology
 - 1.Example: Process flow of E/D SiGate LOCOS Inverter
 - 2.LOCOS Variation
 - 3.Shallow Trench Isolation
 - 3.Lightly doped drain
 - 4.SALICIDE
 5. Self Aligned Contacts (SAC)
 6. Resist trimming
- 4.Transition to CMOS Technology
 - 1.MOS Transistor Types
 - 2.CMOS Inverter
 - 1.Consideration NMOS E/D Inverter
 - 2.Comparison CMOS Inverter
 - 3.CMOS Process flow (Example CMOS 180 nm process)
5. Further Considerations
 - 1.Scaling
 1. Challenges
 - 2.Material Equivalent Scaling
 - 3.Further Concepts

Thank you very much for your attention!

All the very best for the upcoming
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Relaxing vacation!





»Wissen schafft Brücken.«