TECHNISCHE UNIVERSITÄT DRESDEN

DRESDEN concept

Institute of Computer Engineering / Chair of Adaptive Dynamic Systems

DESIGN AND PROGRAMMING OF ADAPTIVE MULTICORE SYSTEMS AND THEIR APPLICATION IN AUTONOMOUS CARS, ROBOTS AND DRONES

Prof. Dr.-Ing. Diana Göhringer
Dresden, April 2018

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Outline

DRESDEN concept

- Research Topics
- Introduction and Motivation
  - Multicore Architectures
  - Requirements of Autonomous Systems
- Adaptive Multicore Systems / Multiprocessor Systems-on-Chip (MPSoCs)
  - Hardware Architecture
  - Design / Programming Tools
  - Software Architecture and Runtime/Operating Systems
- Application Examples: Automotive, Robotics and Drones
- Conclusion and Outlook

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Chair of Adaptive Dynamic Systems

DRESDEN concept

Founded: April 2017

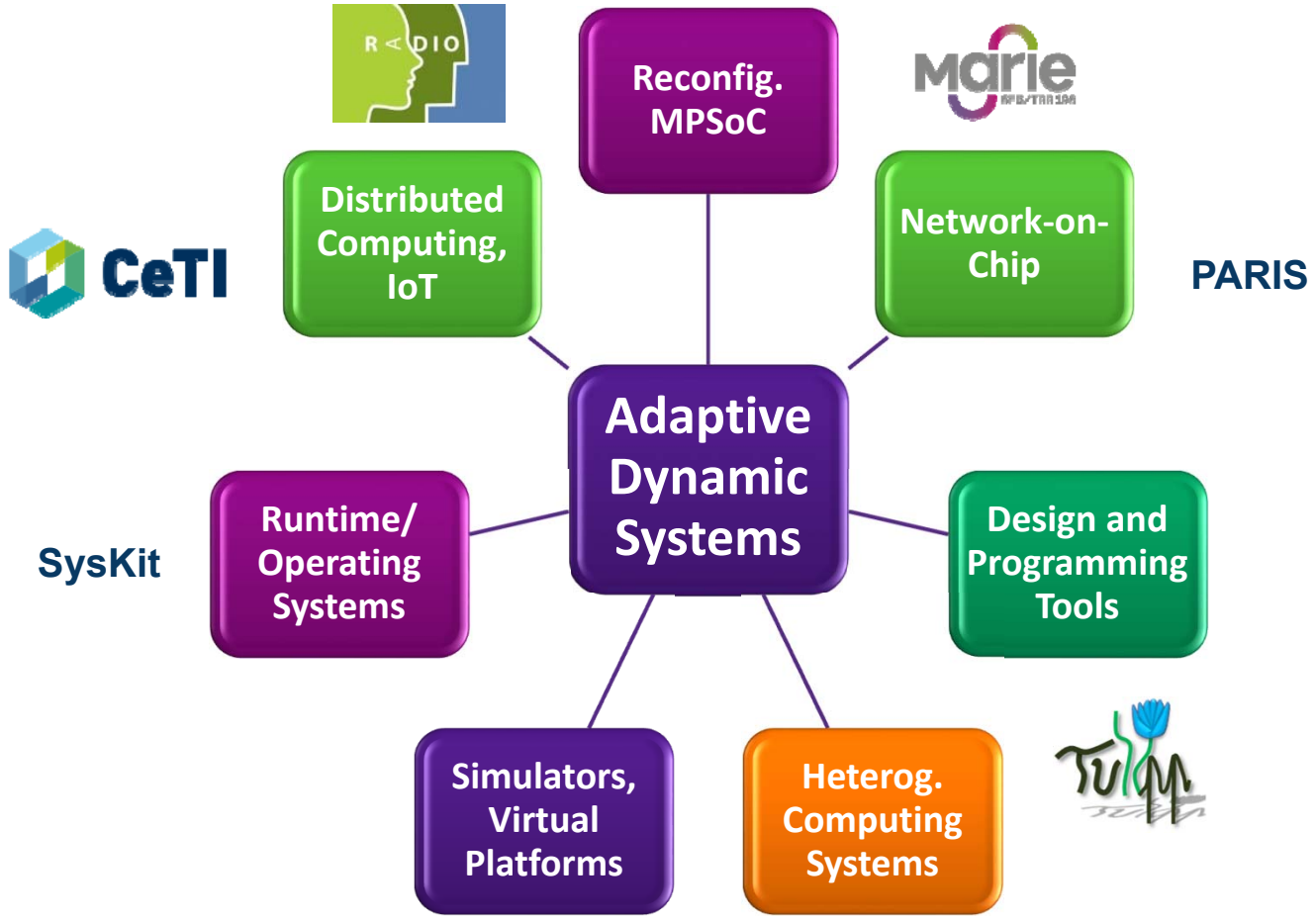
Head: Prof. Dr.-Ing. Diana Göhringer

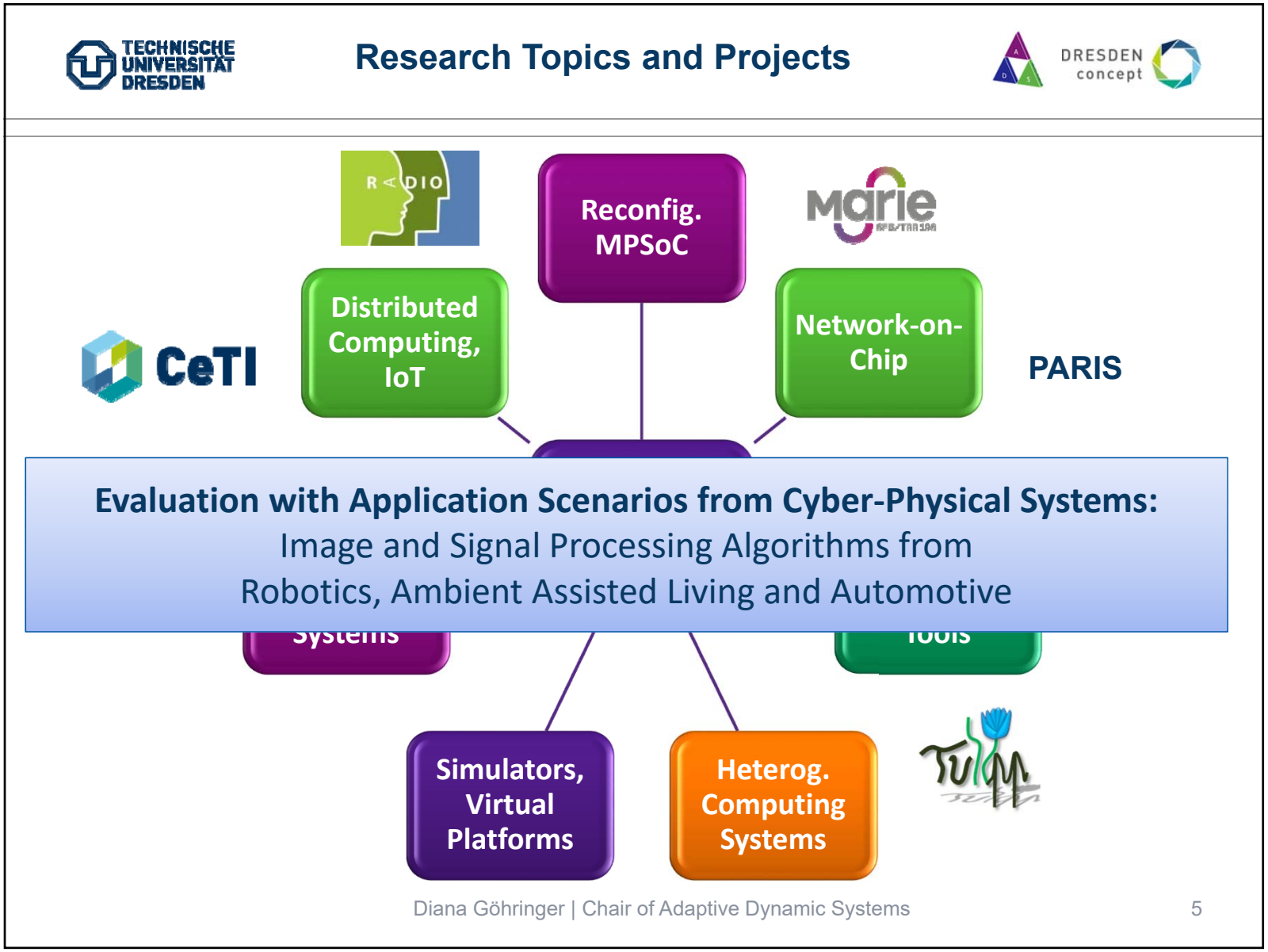
15 PhD students

My previous positions:

2013 – 2017	Juniorprofessor for Application-Specific Multi-Core Architectures at Ruhr-University Bochum
2012	Head of the Young Investigator Group CADEMA at KIT
2011	PhD at Karlsruhe Institute of Technology (KIT)
2007 – 2012	Researcher at Fraunhofer IOSB

Research Topics and Projects

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Research Topics and Projects
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RADIO
Reconfig. MPSoC
marie
Distributed Computing, IoT
Network-on-Chip
CeTI
PARIS
Evaluation with Application Scenarios from Cyber-Physical Systems:
Image and Signal Processing Algorithms from
Robotics, Ambient Assisted Living and Automotive
Simulators, Virtual Platforms
Heterog. Computing Systems
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5

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Motivation

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"I think there is a world market for maybe five computers."

Thomas Watson, chairman of IBM, 1943.

"640K [of memory] ought to be enough for anybody."

Bill Gates, chairman of Microsoft,1981.

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Moore‘s Law

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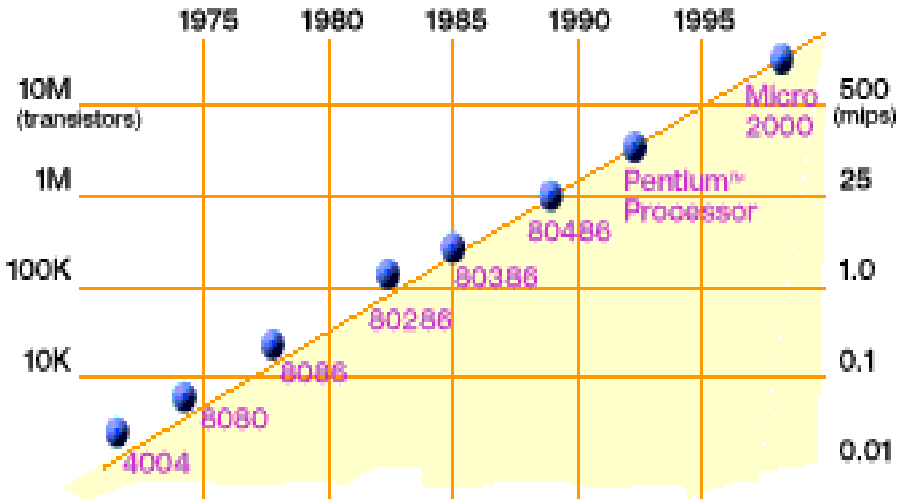
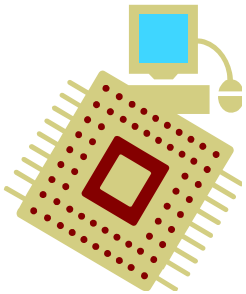
Number of Transistors per Chip is doubled every 18 months



Source: Jack Dongarra



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Problem 1: ILP Wall (II)

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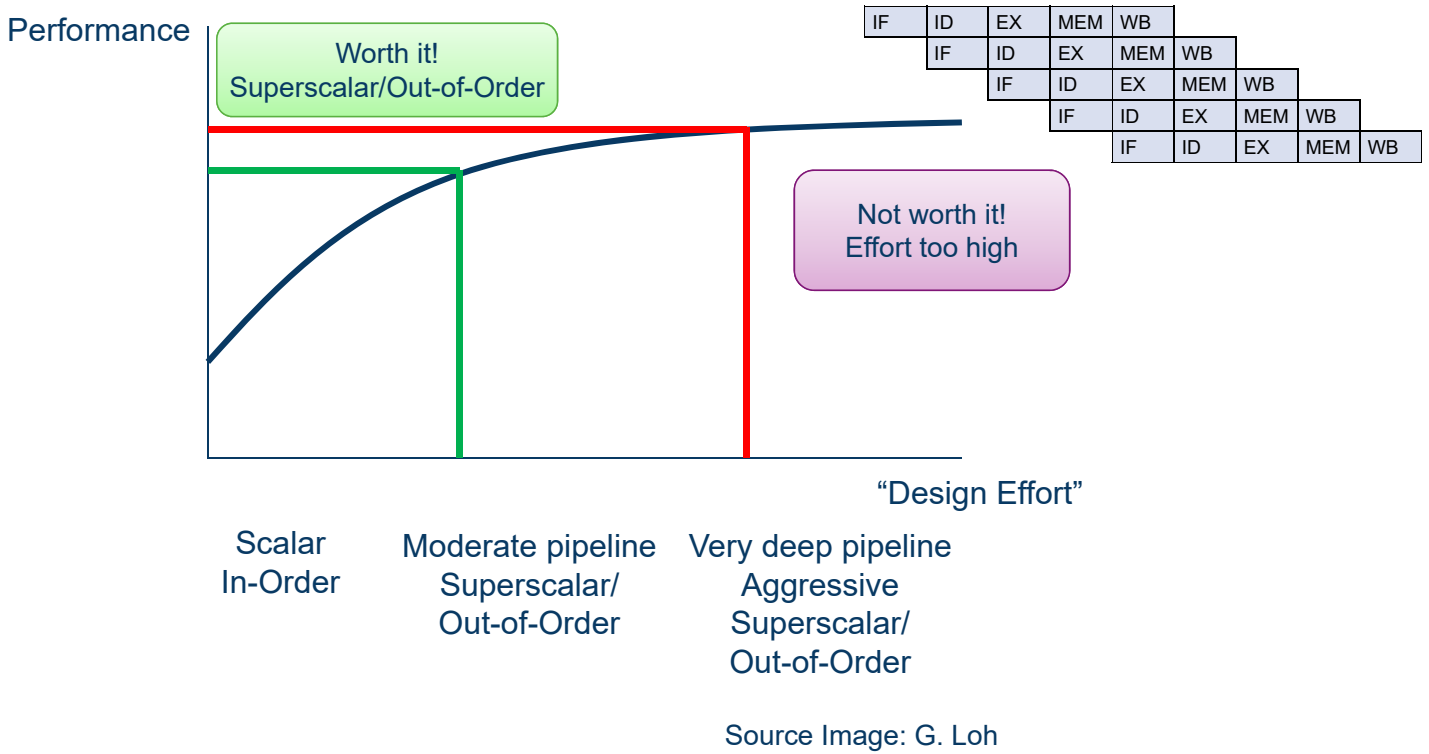

IF	ID	EX	MEM	WB			
	IF	ID	EX	MEM	WB		
		IF	ID	EX	MEM	WB	
			IF	ID	EX	MEM	WB
				IF	ID	EX	MEM	WB

Source Image: G. Loh

→ Solution: Increase the number of processors

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Problem 2: Memory Wall

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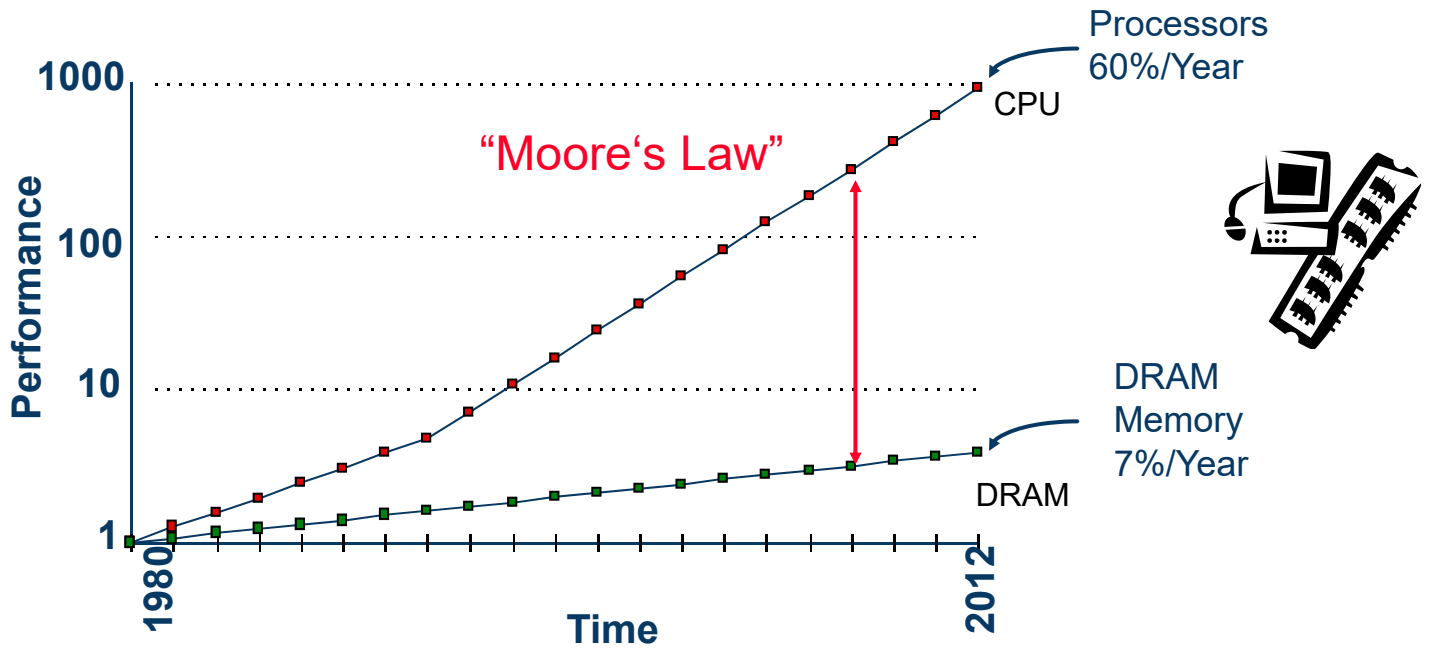
The performance gap between processors and memories grows 50%/year



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Solution: Hierarchical Memory and Multicore Architectures

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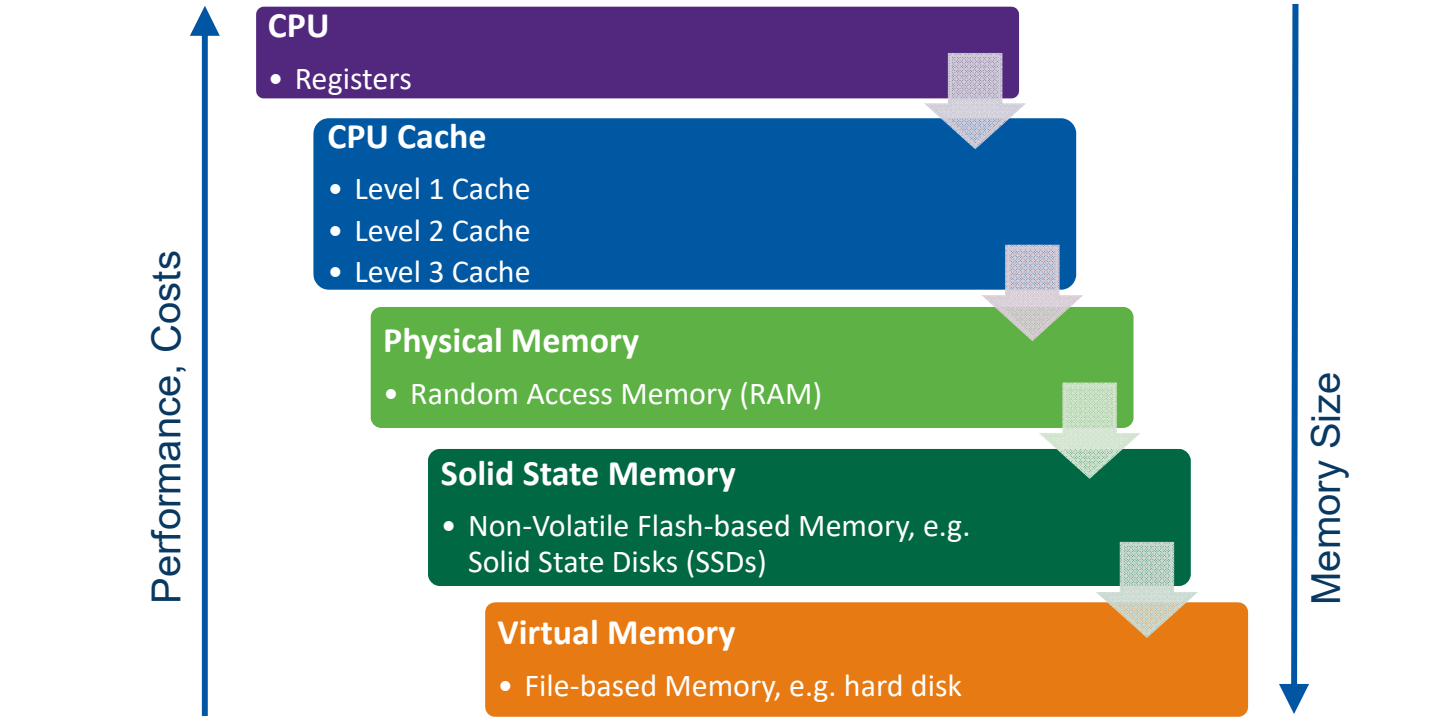

→ To hide memory access times

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Problem 3: Power Wall

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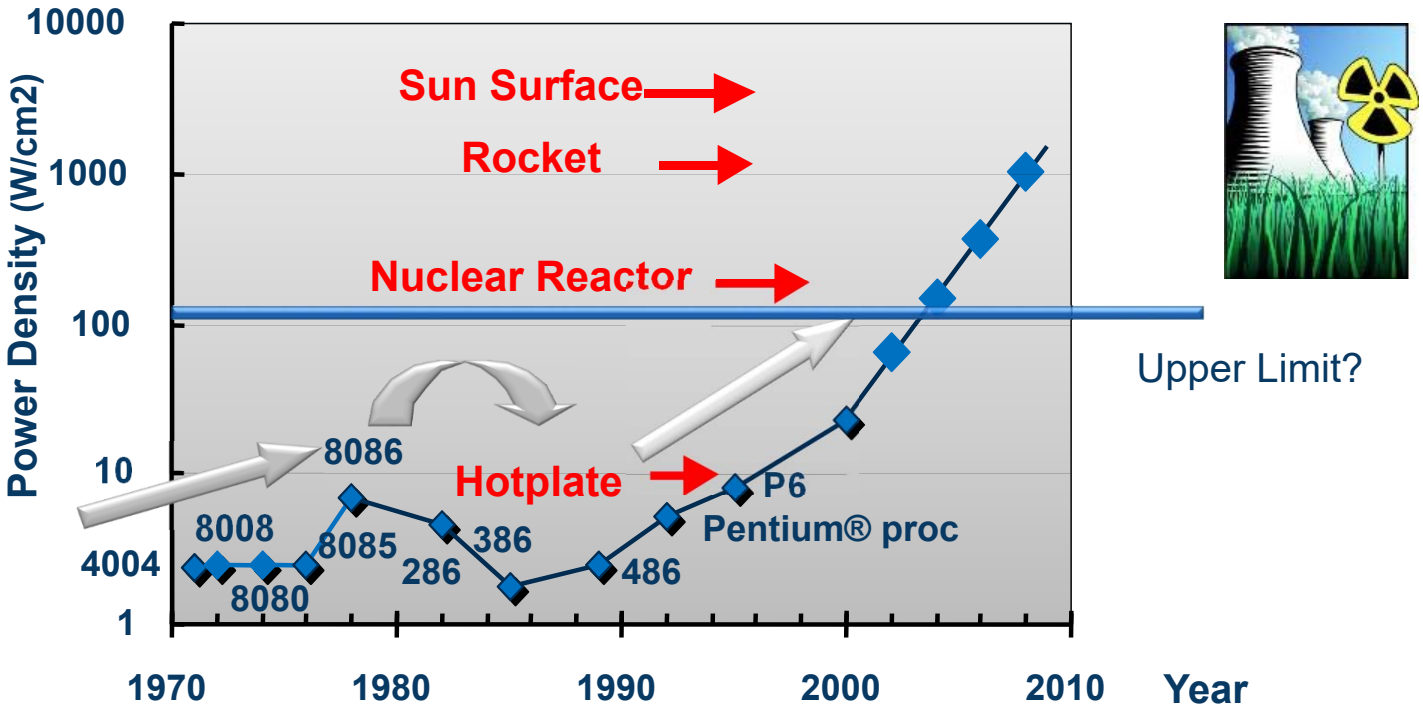
Unbearable in the future! Too high costs for cooling!



Source: J. B. Rabaey, S. Borkar, Intel

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Solution: Parallelism

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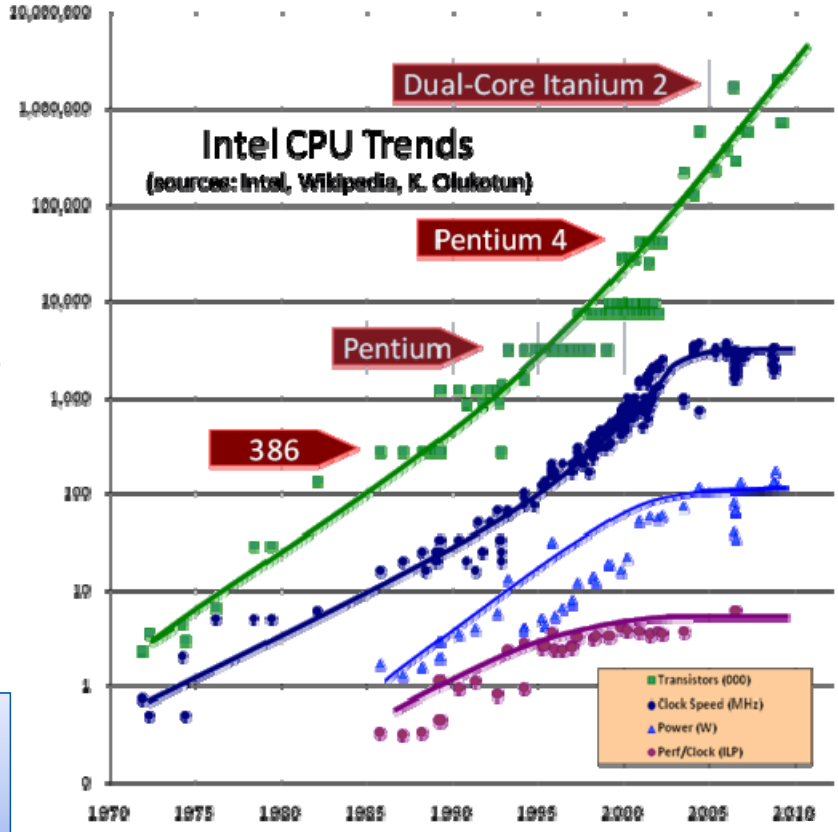
- Number of transistors per chip continues to grow
- **But:** Frequency cannot be increased any further due to the power density
- **Question:** How to efficiently use the increasing number of transistors so that performance continues to grow?

→ Increase the number of processors every 18 months

→ Parallel Programming necessary to efficiently use the processors



Source: Sutter

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Where are Multicore Architectures used?

DRESDEN concept

Multicore

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Where are Multicore Architectures used?

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Embedded Systems → Often powered by batteries, low power consumption
IPADs, Laptops, PCs → Execute a variety of applications in parallel
Supercomputer → Reduce costs for Power and Cooling

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Hardware Components of Multicore Systems

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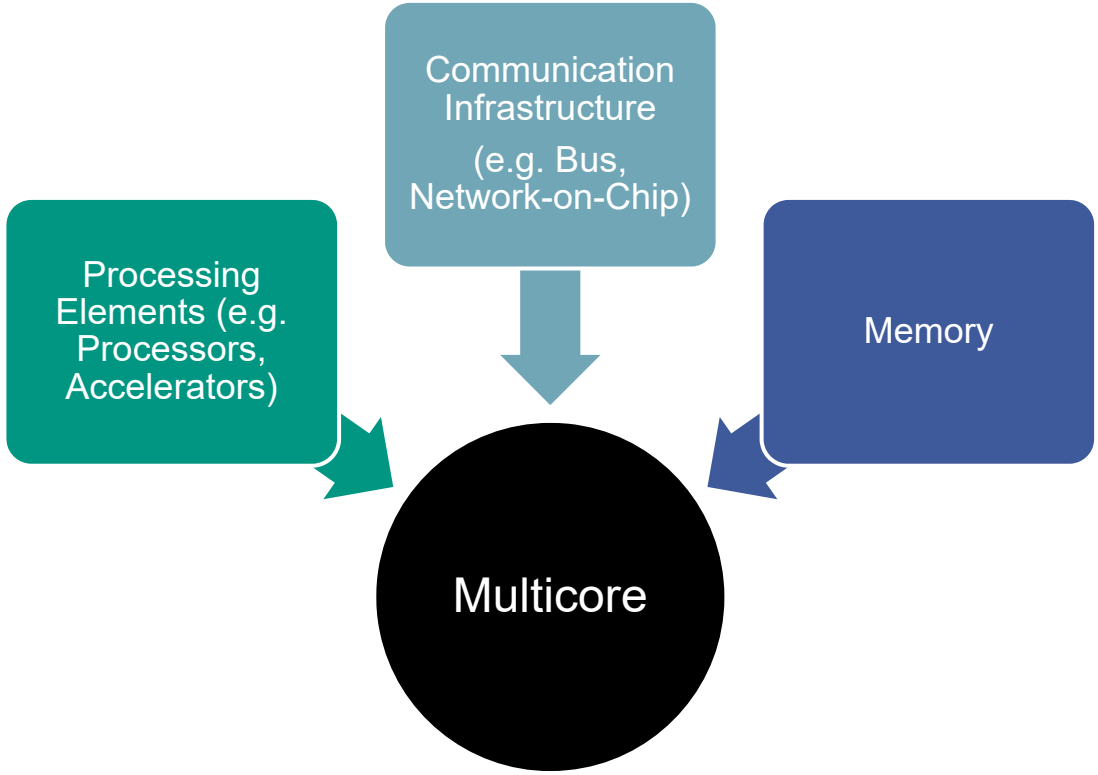

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Classification of Multicore Systems

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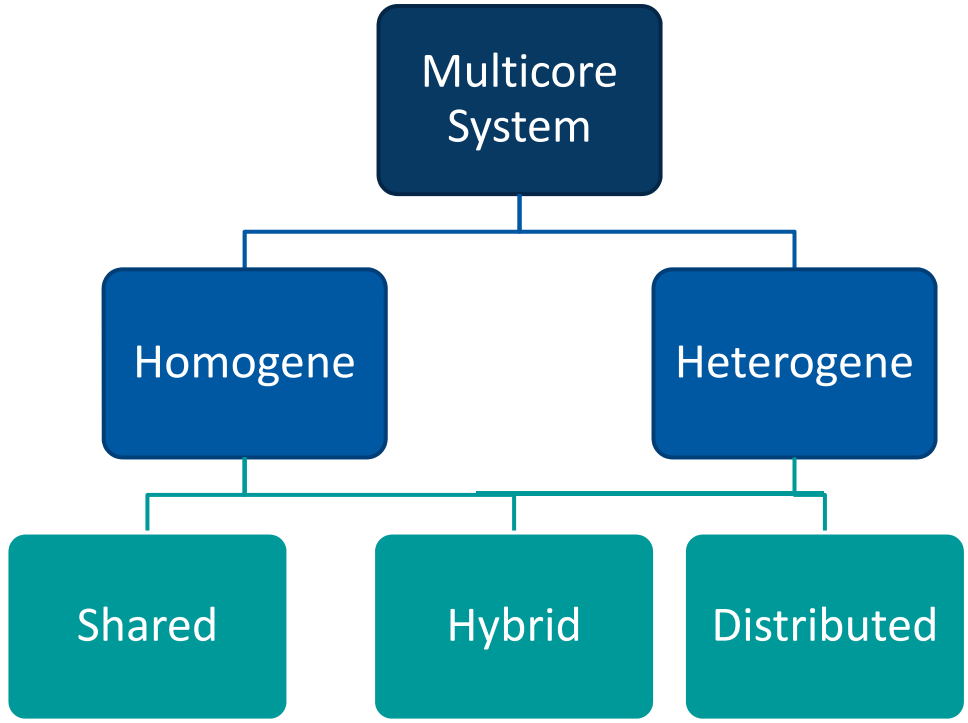
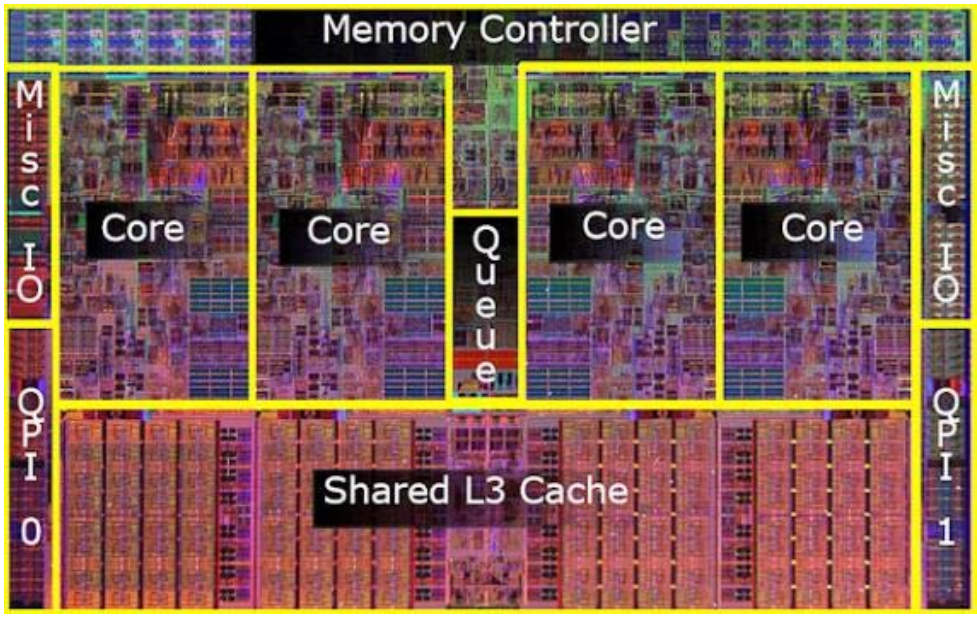
Processing Elements

Memory



Example: Intel i7 Core

- Homogeneous processing elements:
  - 4 Cores
- Shared memory with cache hierarchy to hide latencies:
  - Per core: 32 KB L1 Cache (Instructions and Data) and 256 KB L2 Cache
  - Shared: 8 MB L3 Cache



Source: Intel

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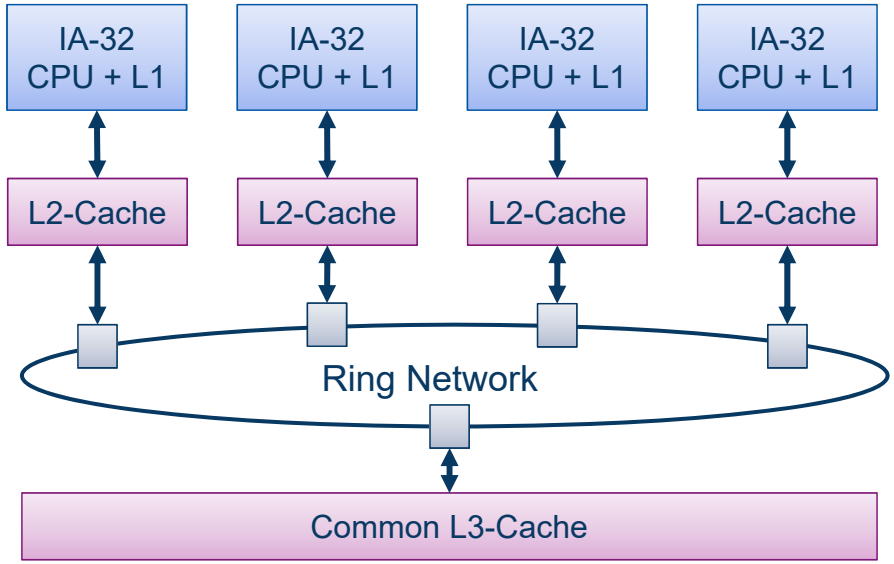
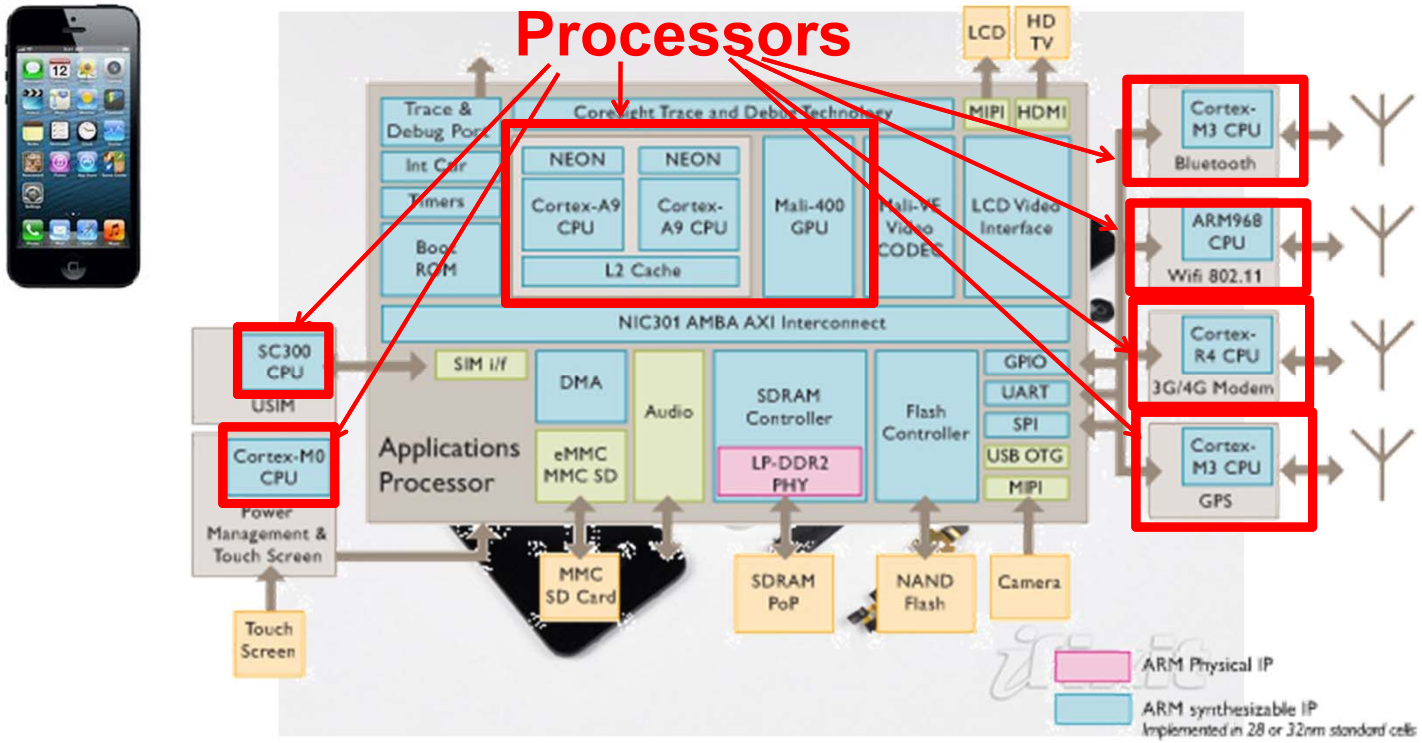


Modified source from: A. S. Tanenbaum, T. Austin: „*Rechnerarchitektur*“. Pearson Verlag, 2014, pp.588.

Example: Heterogeneous Multiprocessor Architecture of the iPhone

Source: K. Asanovic, E. H. Katz

Example: Heterogeneous Multiprocessor Architecture of the iPhone



Source: K. Asanovic, E. H. Katz

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Autonomous Systems

DRESDEN concept

Problem:

- Increasing complexity
- Mixed criticality requirements
- Real-time requirements
- Low power/energy consumption (batteries, cooling)
- Small overall size
- Dynamic adaptation to changing environments

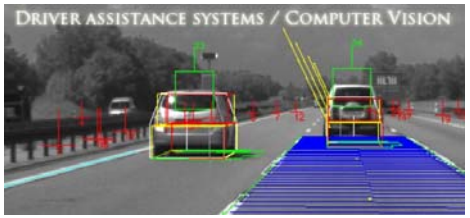
→ Cannot be solved anymore by embedded single core solutions

Possible solution: Heterogeneous multicore systems

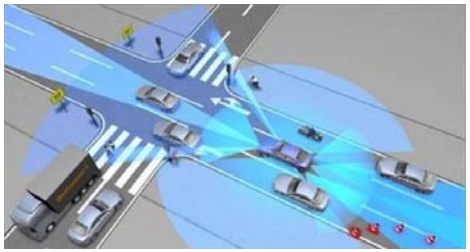
- How to support the dynamic adaptive behavior? Is migration of software tasks sufficient?

Better solution: Reconfigurable MPSoCs

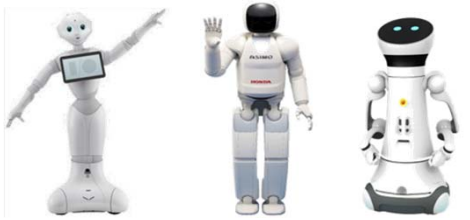
- Runtime adaptation of hardware and software
- Energy-efficient solution for each application phase



http://www.rcs.ei.tum.de/forschung/driver-assistance/

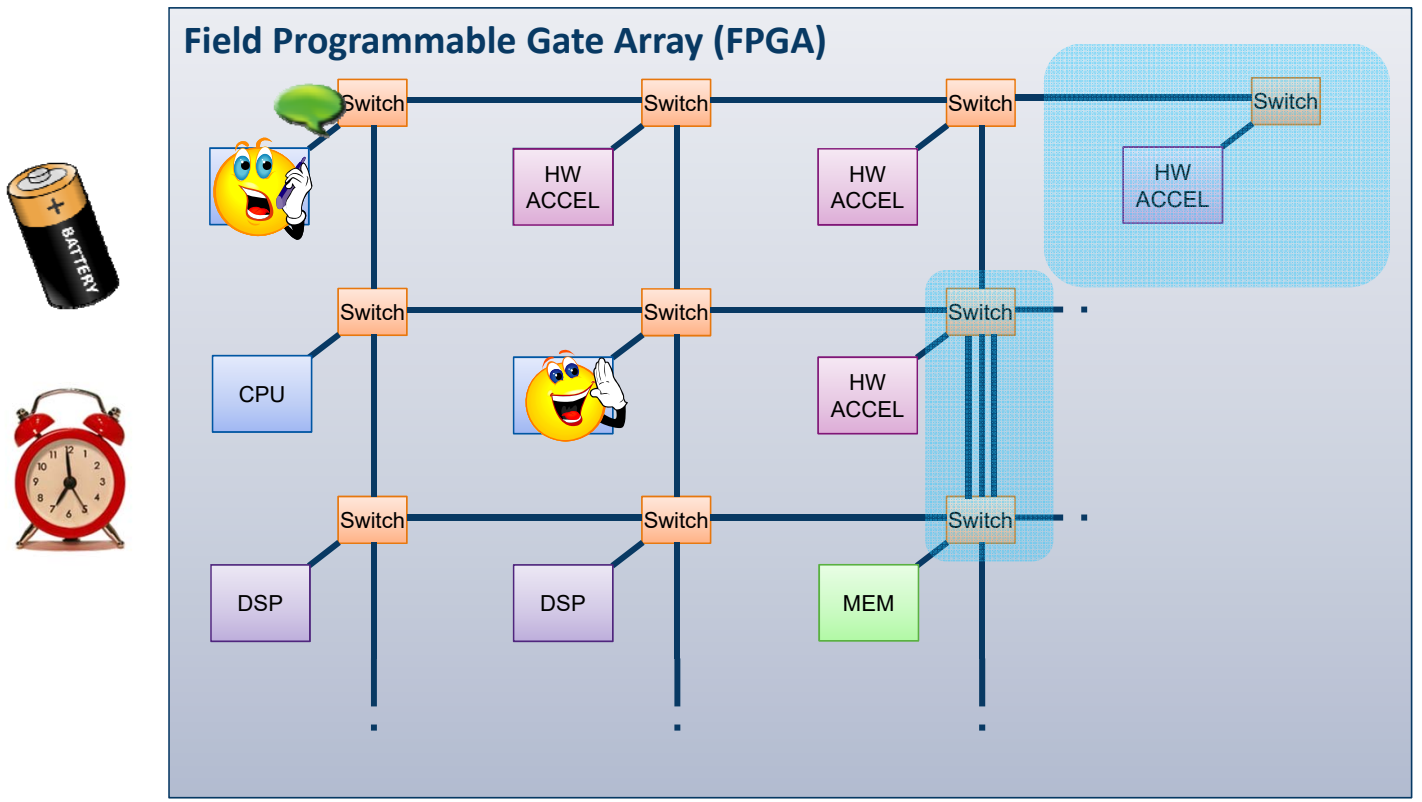


http:// www.asdreports.com/news-10595/key-players-advanced-driver-assistance-systems-adas-market-north-america-20152019

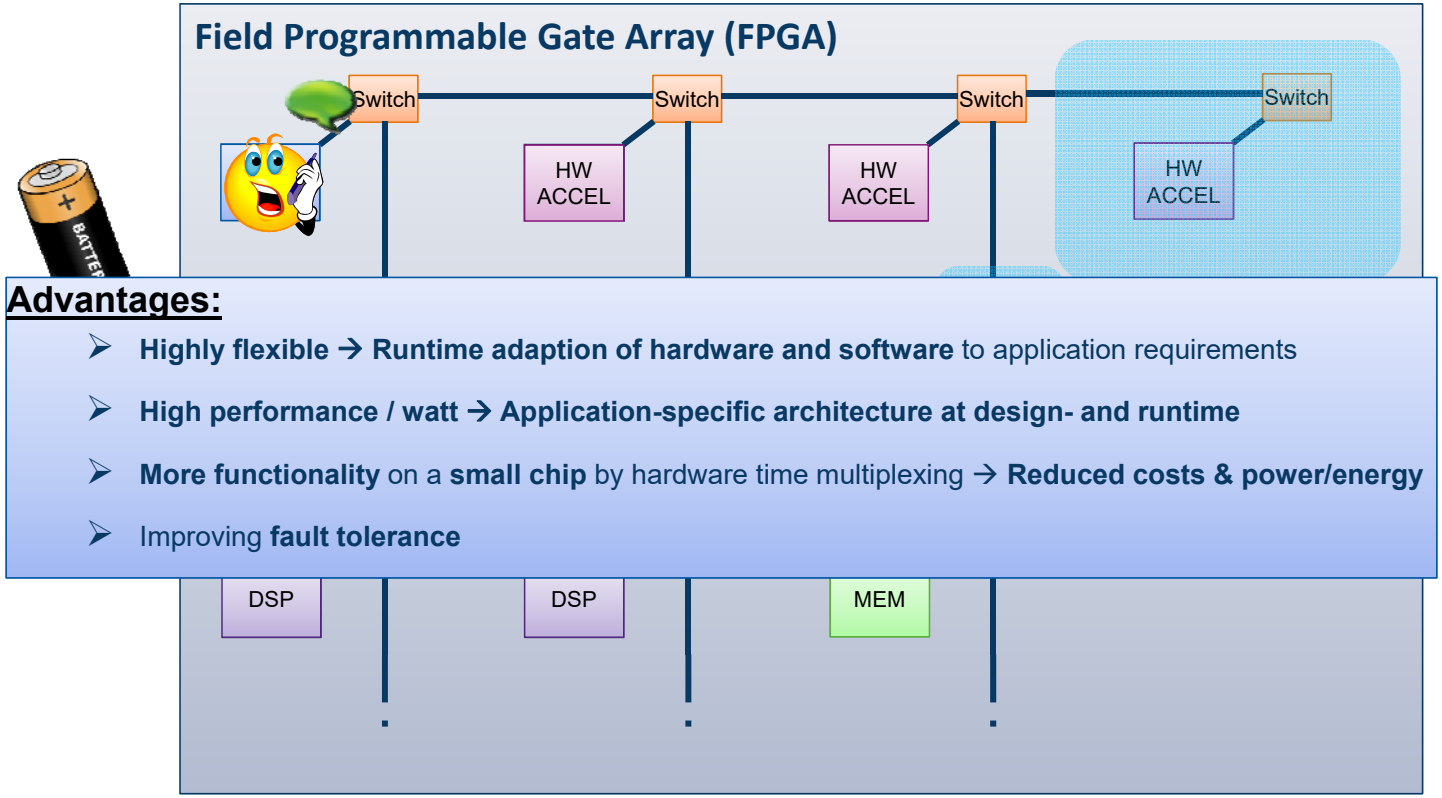


www.ald.softbankrobotics.com asimo.honda.com www.care-o-bot-4.de

Reconfigurable Multiprocessor System-on-Chip (MPSoC)



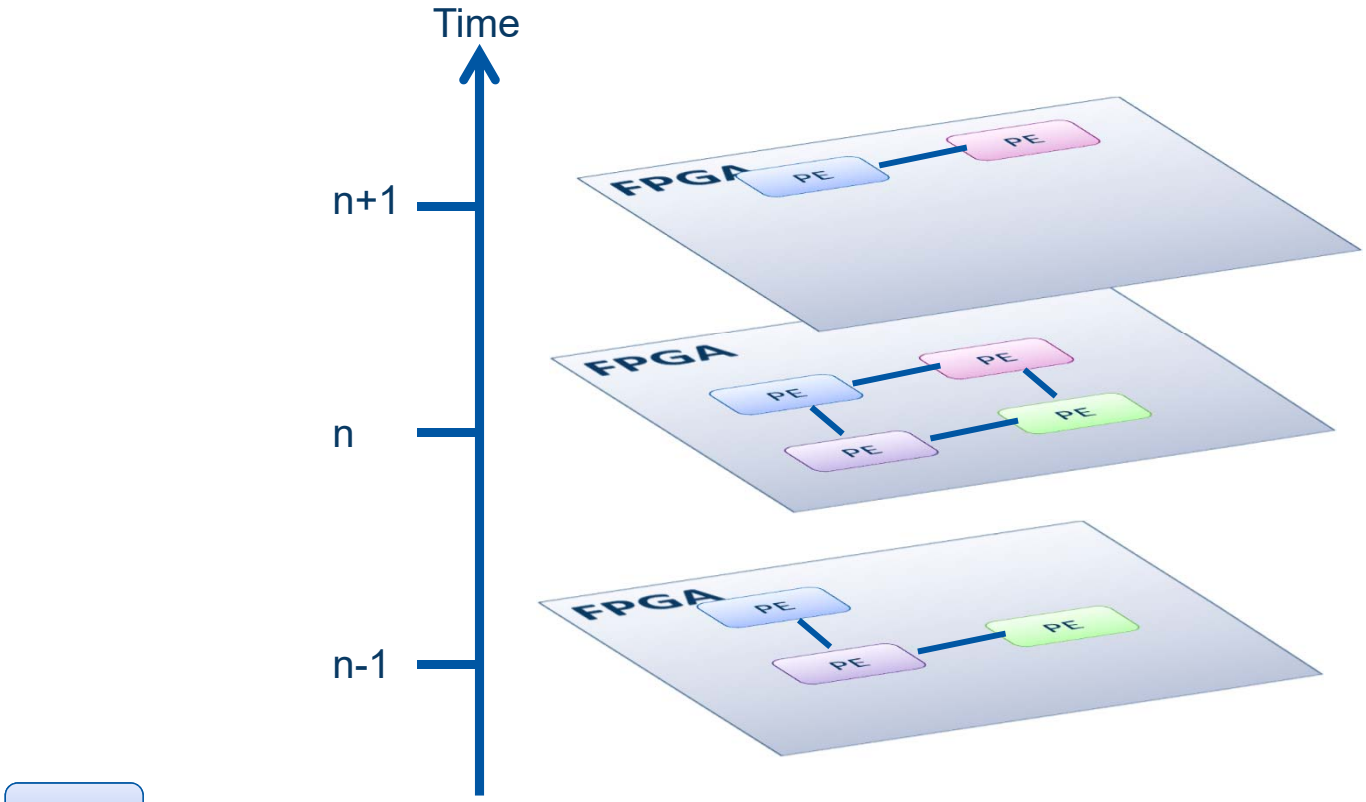
Reconfigurable Multiprocessor System-on-Chip (MPSoC)



Advantages:

- **Highly flexible → Runtime adaption of hardware and software** to application requirements
- **High performance / watt → Application-specific architecture at design- and runtime**
- **More functionality** on a **small chip** by hardware time multiplexing → **Reduced costs & power/energy**
- Improving **fault tolerance**

Time Domain of Reconfigurable MPSoCs

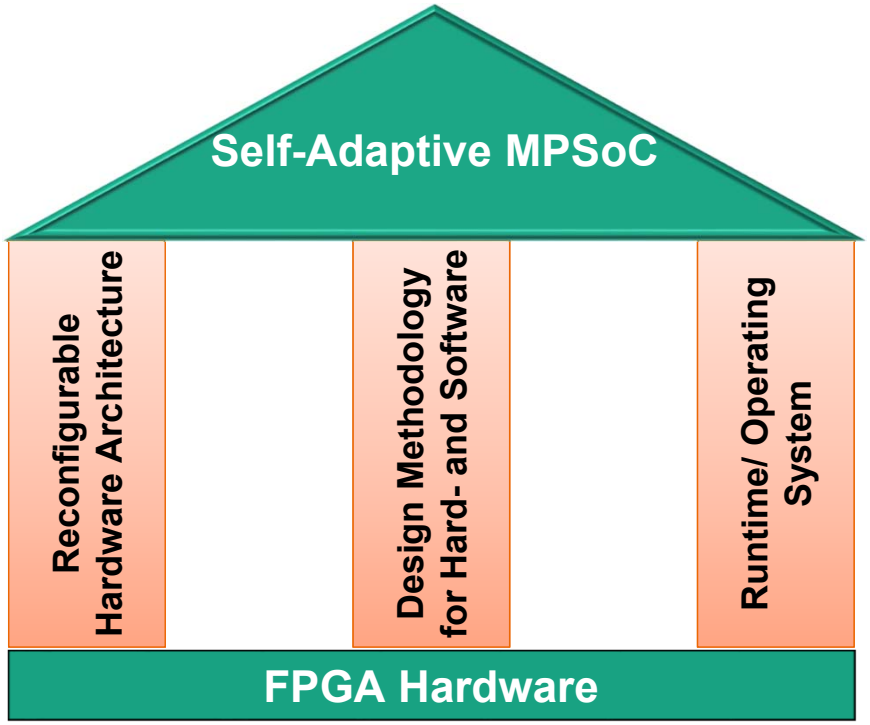


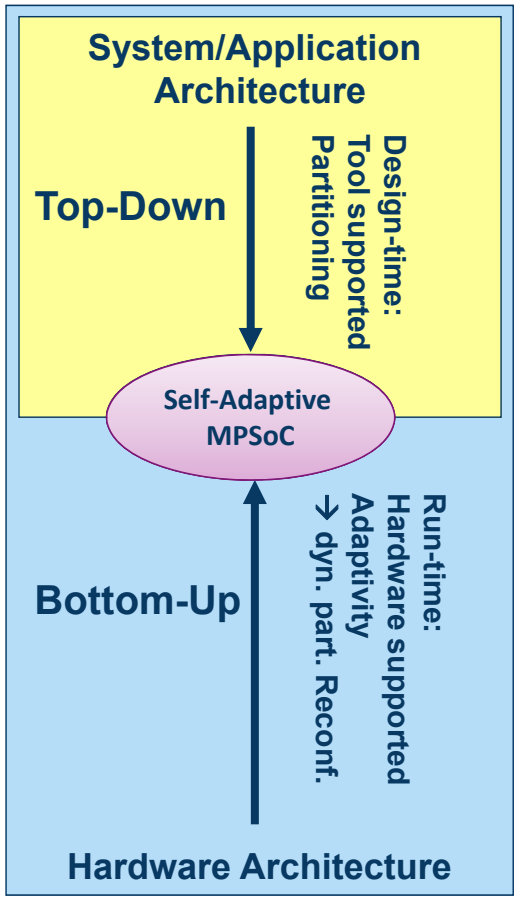
Towards Self-Adaptive MPSoCs

- Challenges are e.g.:
  - Number and type of processing elements (PEs)
  - Type of communication infrastructure (Bus, Network-on-Chip (NoC), etc.)
  - Application description
  - Application partitioning and mapping
  - Which components need to be runtime adaptive?
  - How to decide at runtime, if and how the systems needs to be adapted? Who makes this decision?

→ Huge Design Space: Hardware and application mapping have to be managed over time

Novel „Meet-in-the-Middle“ Solution





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RAR-MPSoC

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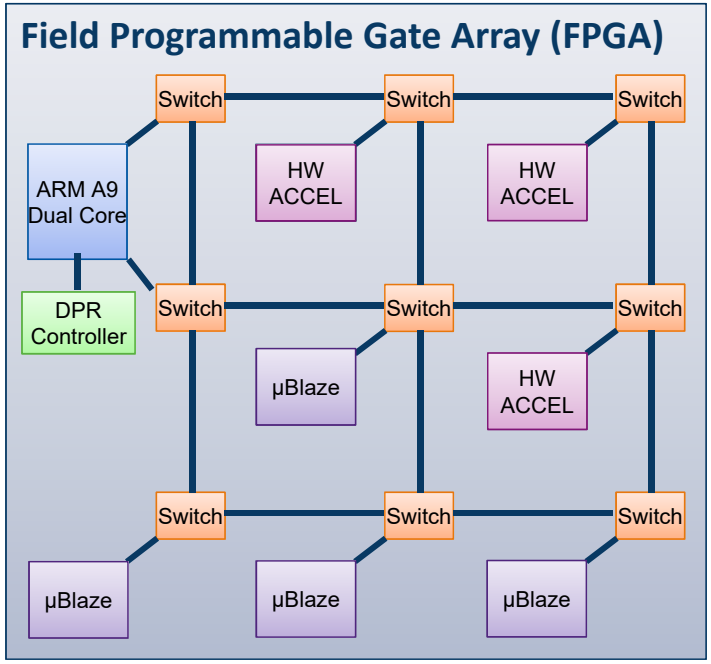
Reconfigurable and Adaptive Routable MPSoC

Motivation:

- Improving throughput and energy efficiency
  - Decrease energy consumption: dynamic partial reconfiguration
  - Increase throughput: choose the best path (avoiding hotspots) in NoCs
- RAR-MPSoC provides:
  - Reconfigurable processing elements
  - RAR-NoC with
    - 2D-Mesh with wormhole switching → Highly scalable and low latency
    - Runtime adaptive routing algorithms
    - Reconfigurable routers



DPR: Dynamic and Partial Reconfiguration

Rettkowski J, Goehringer D (2014) RAR-NoC: A Reconfigurable and Adaptive Routable Network-on-Chip for FPGA-based Multiprocessor Systems. In Proc. of the International Conference on Reconfigurable Computing and FPGAs (ReConFig), Cancun, Mexico.

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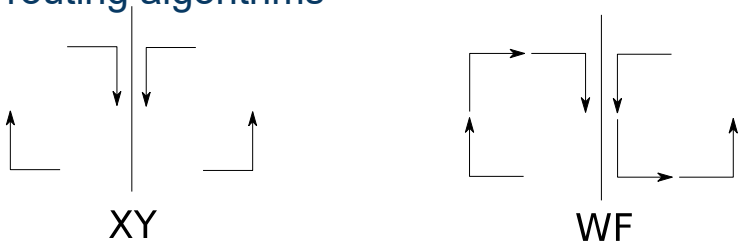
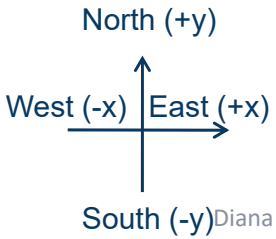
RAR-MPSoC

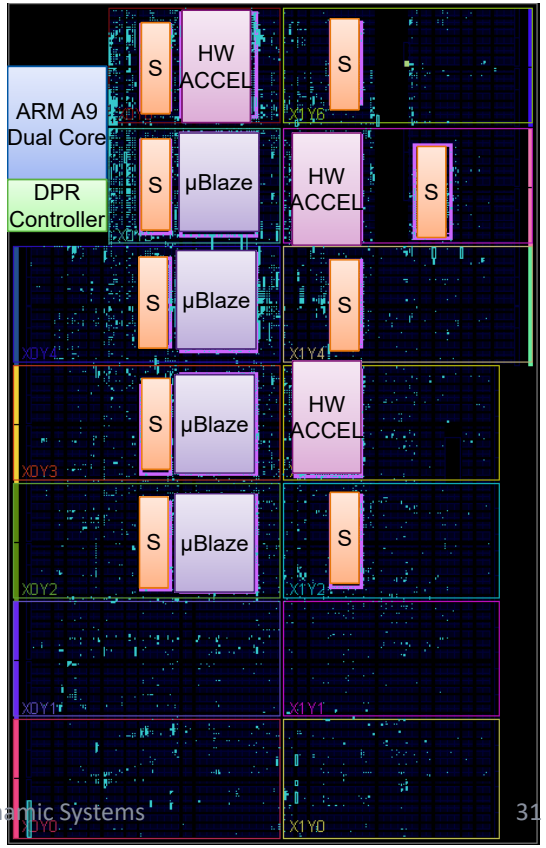
DRESDEN concept

Reconfigurable and Adaptive Routable MPSoC

- Implemented on Xilinx Zynq
- ARM processor controls the self-adaptation
- Two high performance interfaces between ARM processor and RAR-NoC
- RAR-NoC supports XY and West First routing algorithms







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RAR-MPSoC

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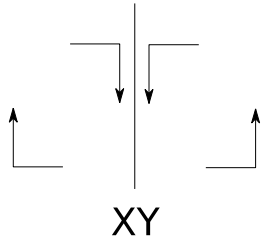
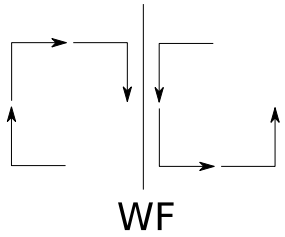
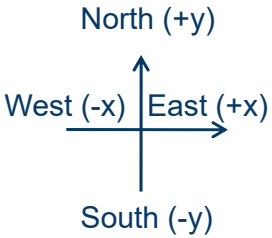
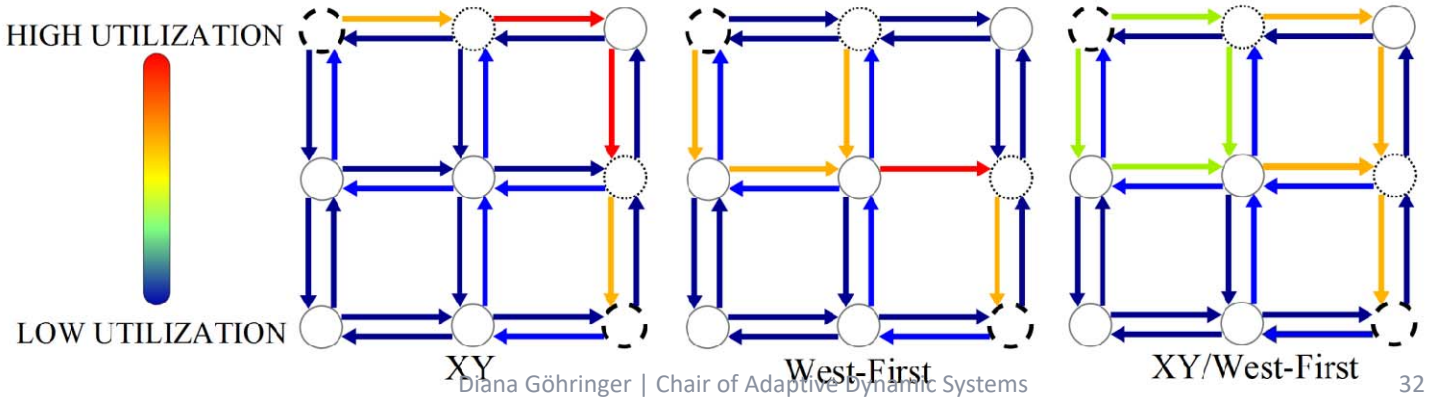
Load Balancing using two Routing Algorithms

- Using both routing algorithm reduces congestions









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Area Results on Zynq 706

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Module	LUT	BRAM
Direct Memory Access	2091	3
Reset	147	0
Monitor	1370	0
Timer	321	0
Network Interface	2	0
Microblaze	4327	5
Accelerator	28	0
System	42855 (17%)	44 (3%)

RAR-NoC Router (xc7z045-2)	XY	WF	XY & WF
Number of LUTs	781	808	869

Area Results on Zynq 706

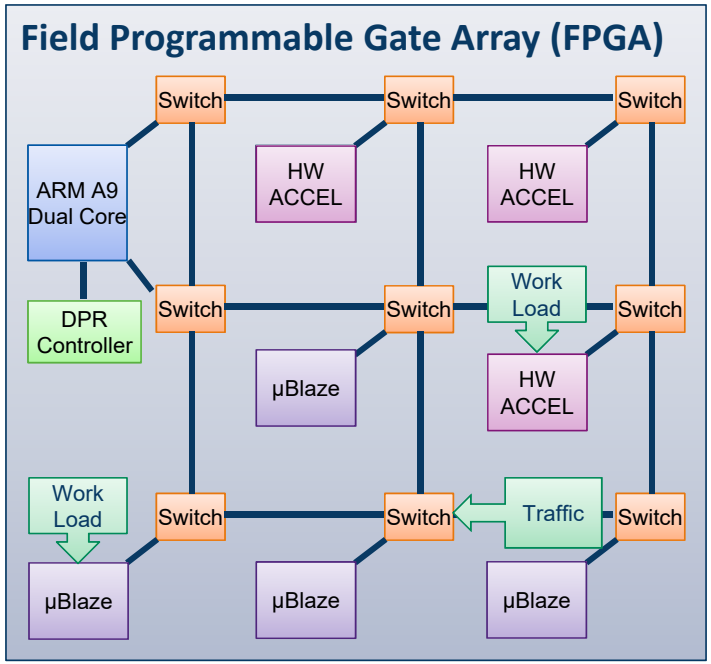
Module	LUT	BRAM
Direct Memory Access	2091	3
Reset	147	0
Microblaze	4327	3
Accelerator	28	0
System	42855 (17%)	44 (3%)

Still plenty of resources available
→ Can easily realize systems with > 30 processors on this midsize FPGA

RAR-NoC Router (xc7z045-2)	XY	WF	XY & WF
Number of LUTs	781	808	869

Hardware/Software Monitors

- To overserve the current state of the MPSoC, such as
  - Performance (e.g. execution times, communication times)
  - Work load of the processors and accelerators
  - Communication bottlenecks
  - Faults



DPR: Dynamic and Partial Reconfiguration

→ **Important to detect situations for self-adaptation of hardware and software**

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Hardware/Software Monitors: Example

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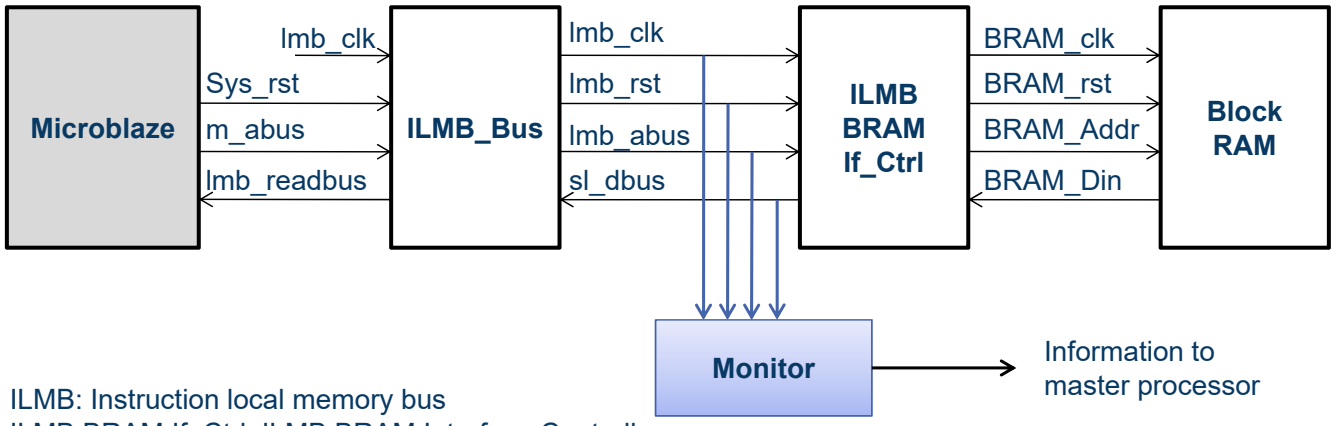
Hardware Monitor for Workload Detection for Xilinx MicroBlaze Processor

- Collects information about the computational load:
  - Loops
  - Wait states
  - End of executable files



ILMB: Instruction local memory bus
ILMB BRAM If_Ctrl: ILMB BRAM Interface Controller

Goehringer D, Chemaou M, Huebner M (2012) On-chip monitoring for adaptive heterogeneous multicore systems. In Proc. of the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), York, UK.

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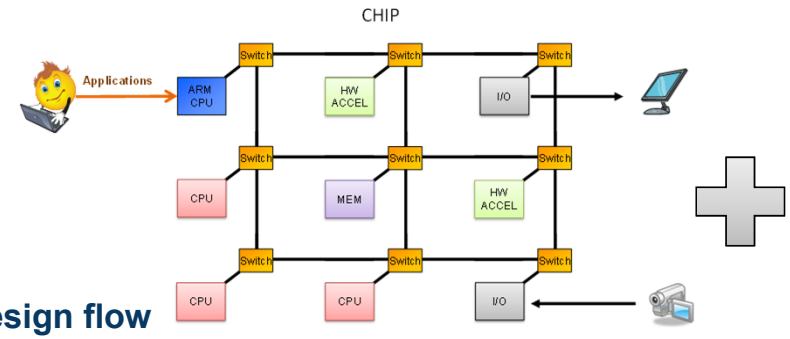
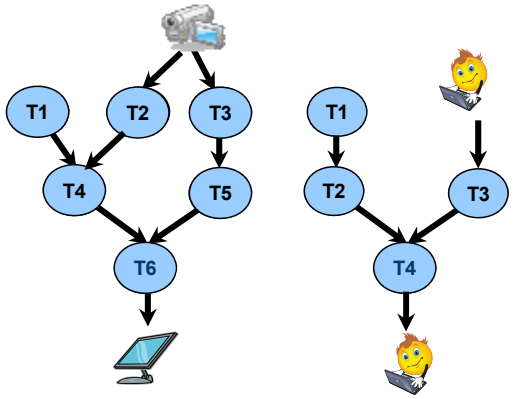
Abstraction of the Complexity

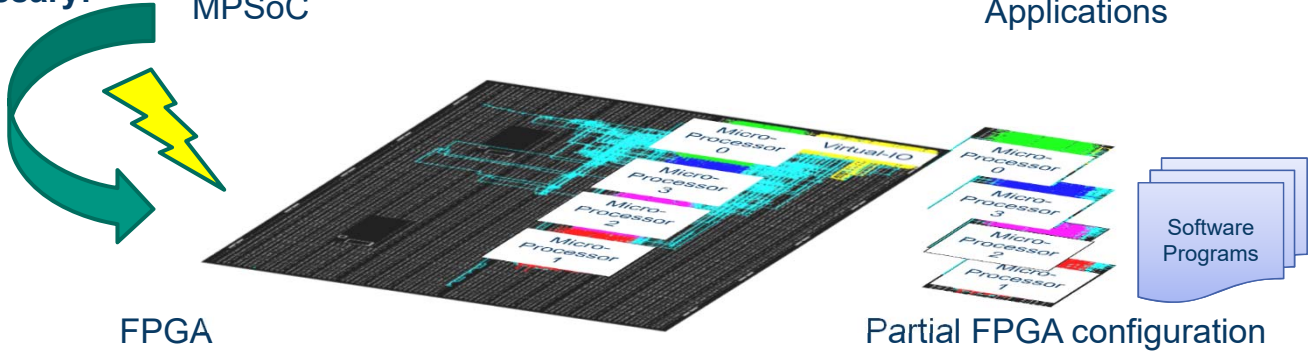




Design flow and runtime management necessary!

Self-adaptive MPSoC

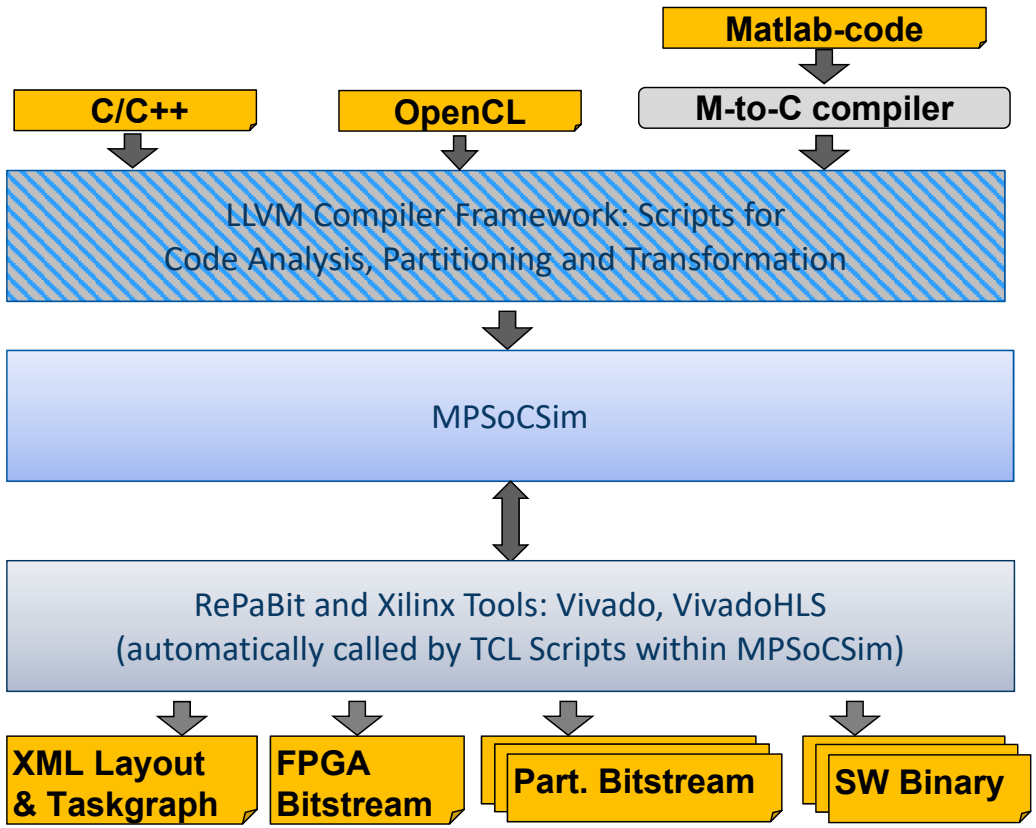
Multiple Applications



FPGA configuration data

Partial FPGA configuration streams and software programs

Design / Programming Methodology



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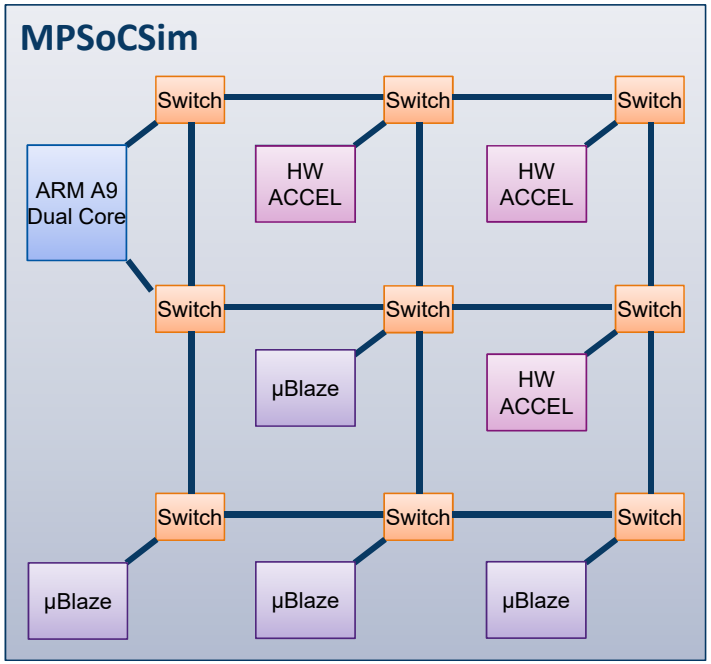
MPSoCSim

DRESDEN concept

Key Features

First Simulator for self-adaptive NoC-based heterogeneous MPSoCs:

- Based on Open Virtual Platform (OVP) from Imperas
- Supports several processor models (e.g. ARM, µBlaze) and operating systems (e.g. Linux)
- Supports simulating partial reconfiguration of the processing elements
- Fast estimation of system and network-on-chip performance, resource requirements and power consumption
- Automatic generation of the target FPGA design



Wehner P, Rettkowski J, Kalb T, Göhringer D (2016) Simulating Reconfigurable Multiprocessor Systems-on-Chip with MPSoCSim. ACM Transactions on Embedded Computing Systems (TECS), pp. 1-24.

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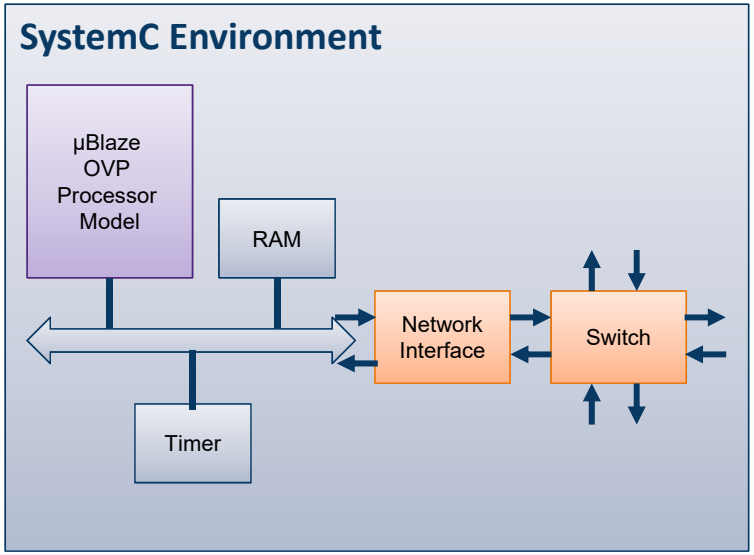
MPSoCSim

DRESDEN concept

Network Interface

Network Interface:

- Used to connect OVP Processor Models to the SystemC-based Network-on-Chip
- Acts equivalent to ordinary peripheral components
- Addressed via a local bus



Problem with simulating dynamic and partial reconfiguration (DPR)

- No open SystemC ports and sockets are allowed
- Once SystemC simulation runs, no connections to ports/sockets may be changed

→ New interface needed!

Wehner P, Rettkowski J, Kalb T, Göhringer D (2016) Simulating Reconfigurable Multiprocessor Systems-on-Chip with MPSoCSim. ACM Transactions on Embedded Computing Systems (TECS), pp. 1-24.

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MPSoCSim

DRESDEN concept

DPR Interface

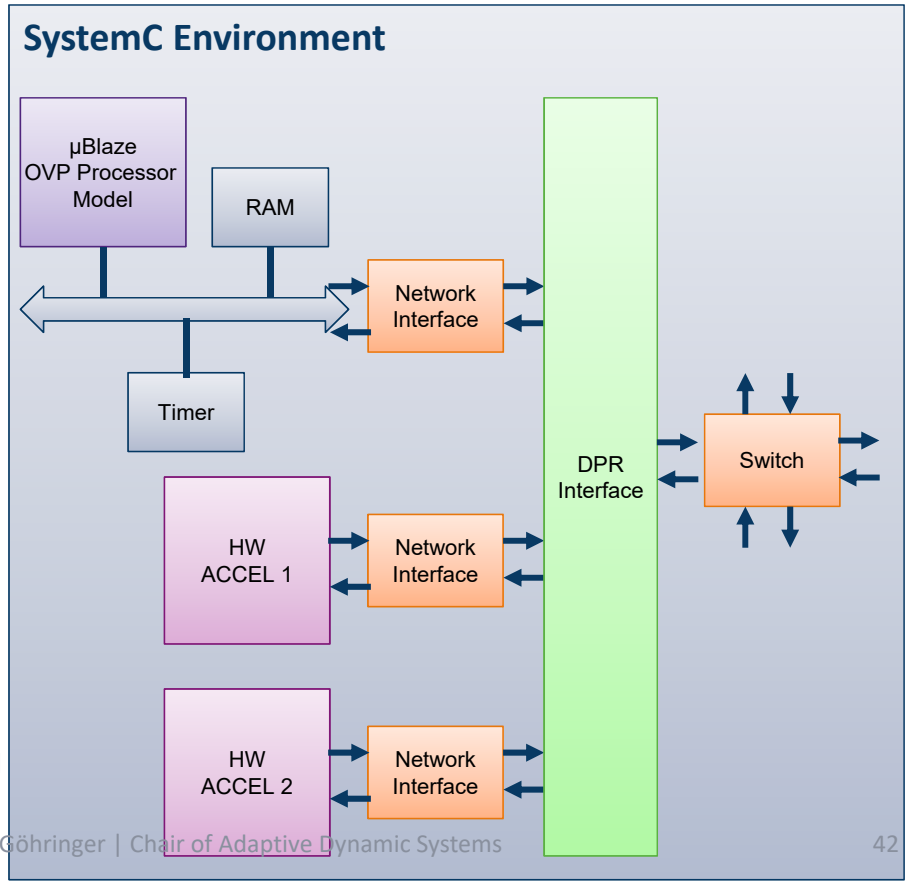
DPR Interface – SystemC

Module

- Flexible amount of initiator and target sockets for binding processing elements
- Extends simulator with additional Z-dimension

Function

- Contains information of currently active processing element
- Can switch at runtime between active processing elements
- Connects the active processing element with the network-on-chip



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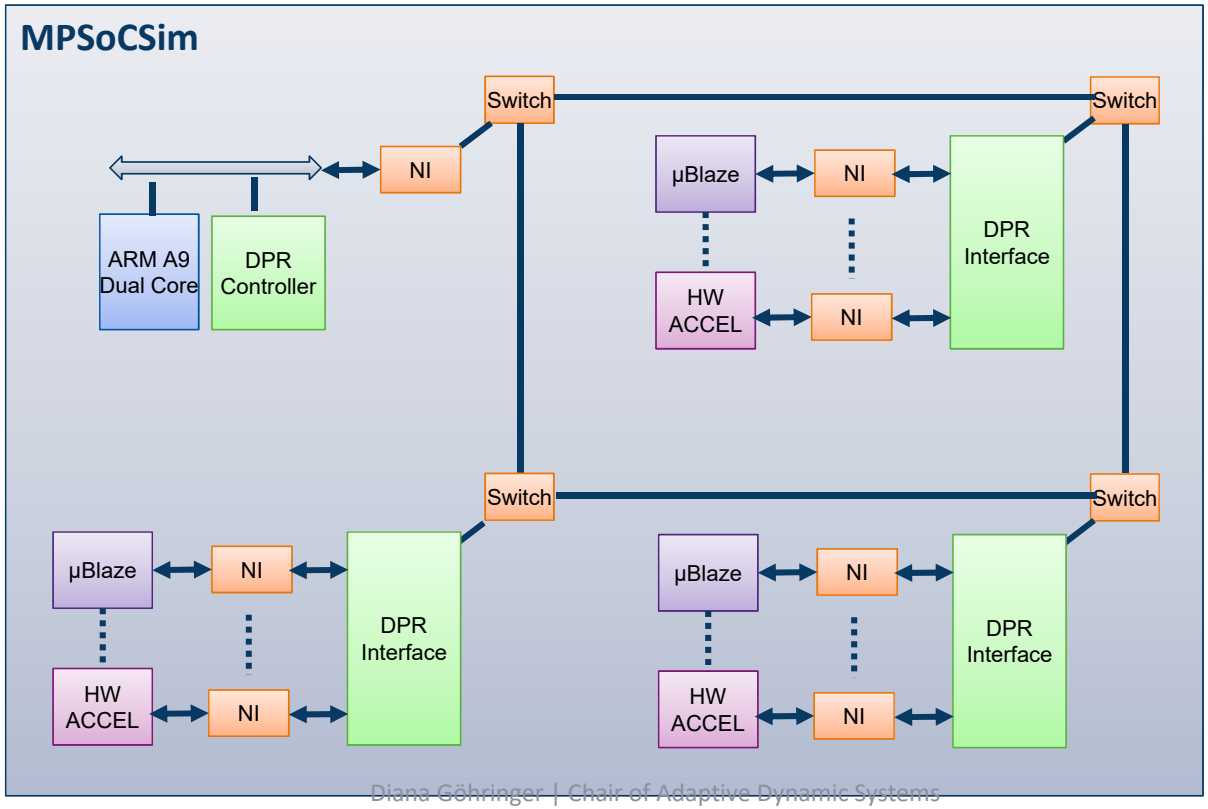
MPSoCSim

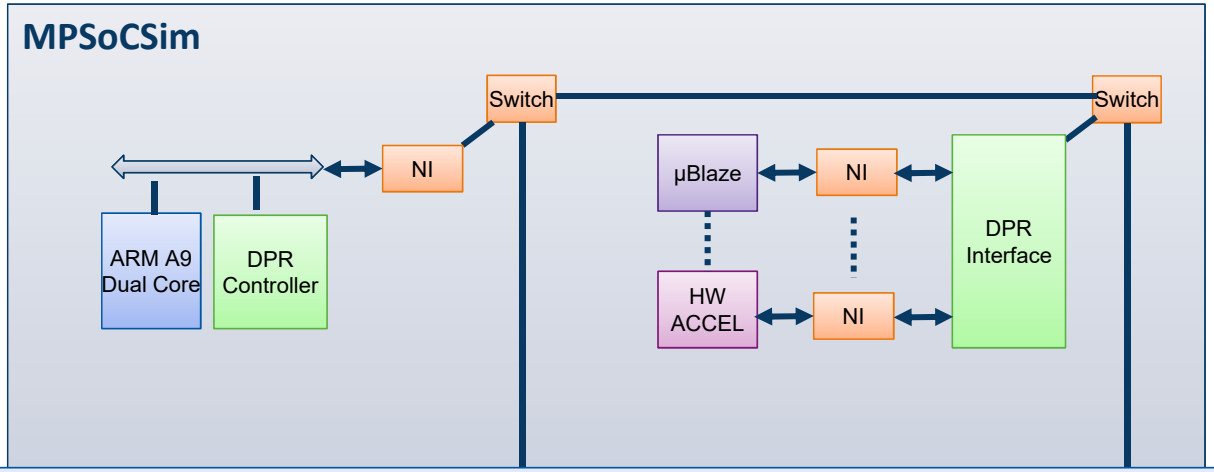
DRESDEN concept

System View and DPR controller



MPSoCSim

System View and DPR controller



DPR Controller – SystemC Module

- Holds information about present DPR Interfaces and their active processing elements
- Receives data necessary for dynamic partial reconfiguration (*ID and socket nr.*)
- Executes DPR according to PCAP interface

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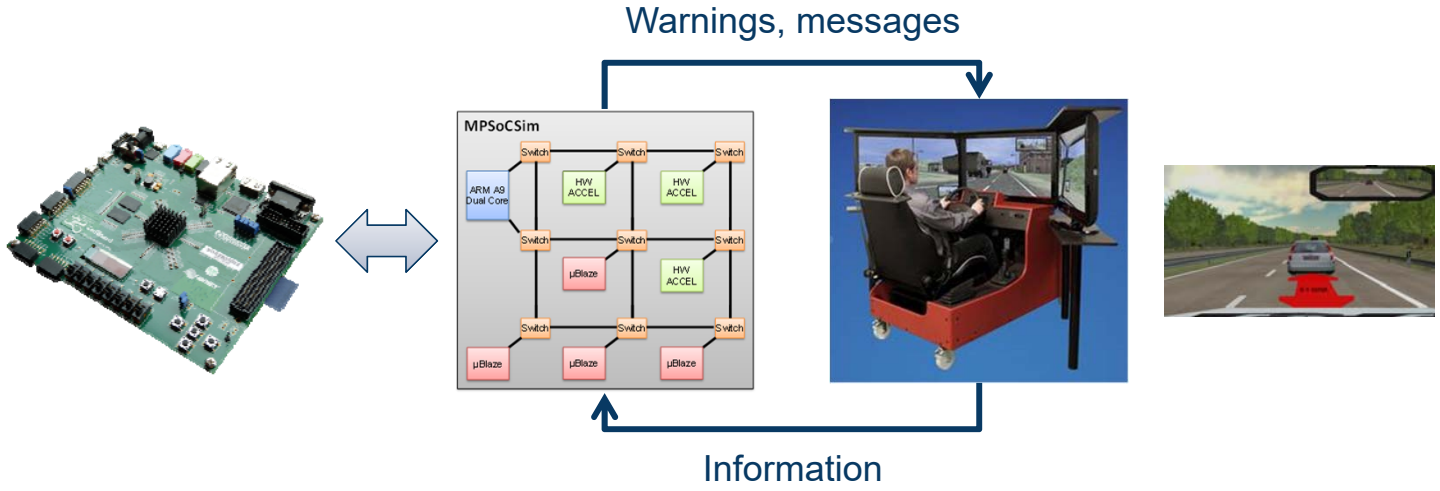
MPSoCSim

DRESDEN concept

Additional Features

- Can easily be connected to real sensor/actors and other simulators, e.g. a car simulator
- Proof of concept with two ECUs: cruise control and adaptive cruise control (ACC)



P. Wehner, D Goehringer (2013) Evaluation of Driver Assistance Systems with a Car Simulator using a Virtual and a Real FPGA Platform , In Proc. of the Conference on Design and Architectures for Signal and Image Processing (DASIP), Cagliari, Italy.

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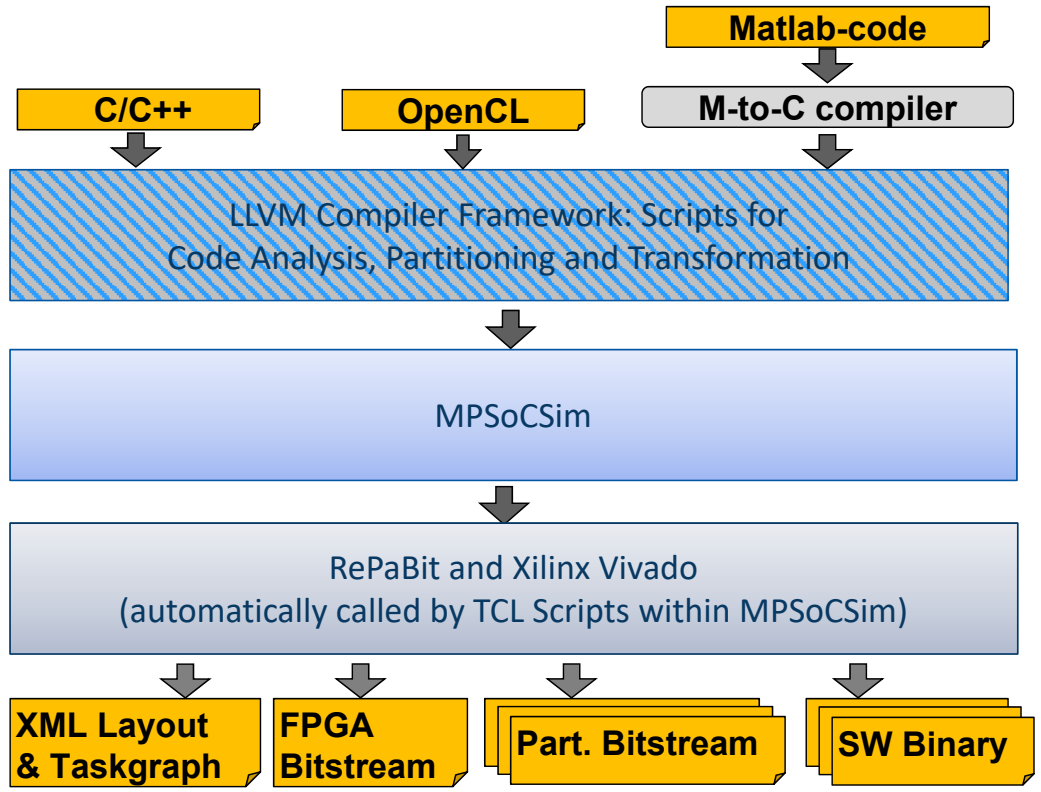
Design / Programming Methodology

DRESDEN concept



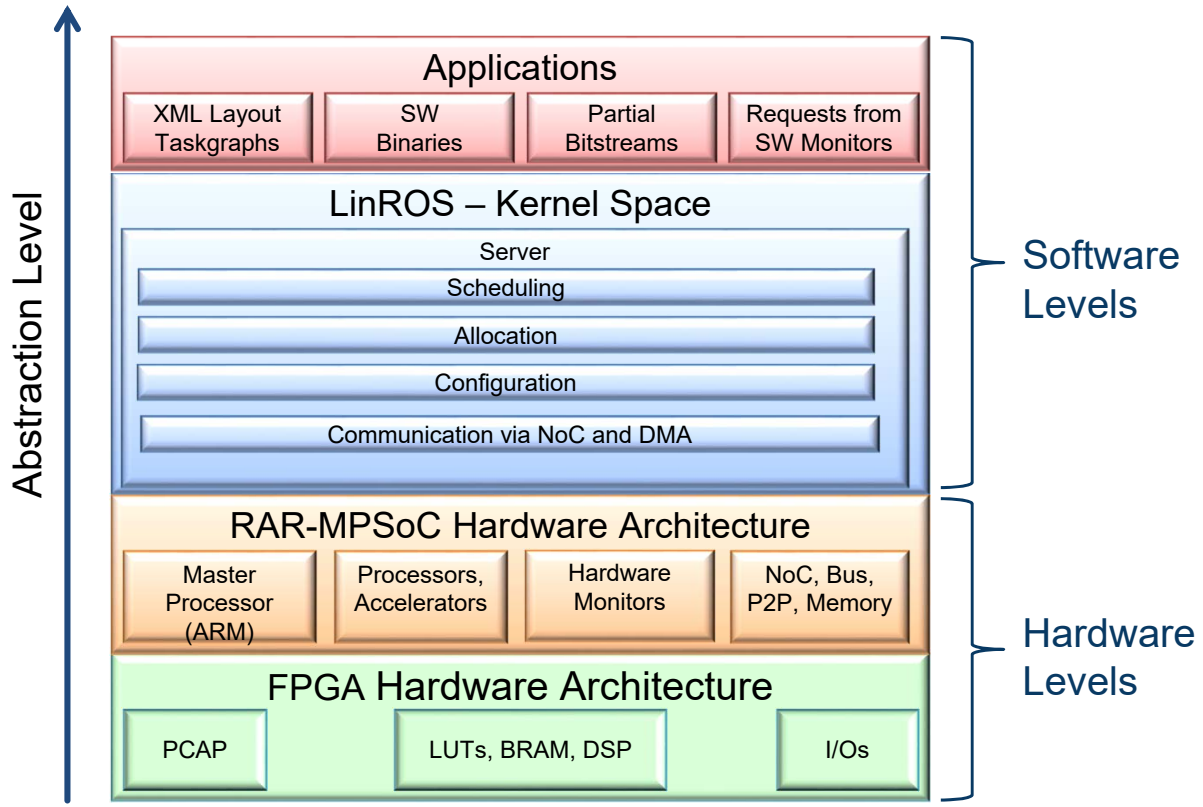
TECHNISCHE UNIVERSITÄT DRESDEN

Outline

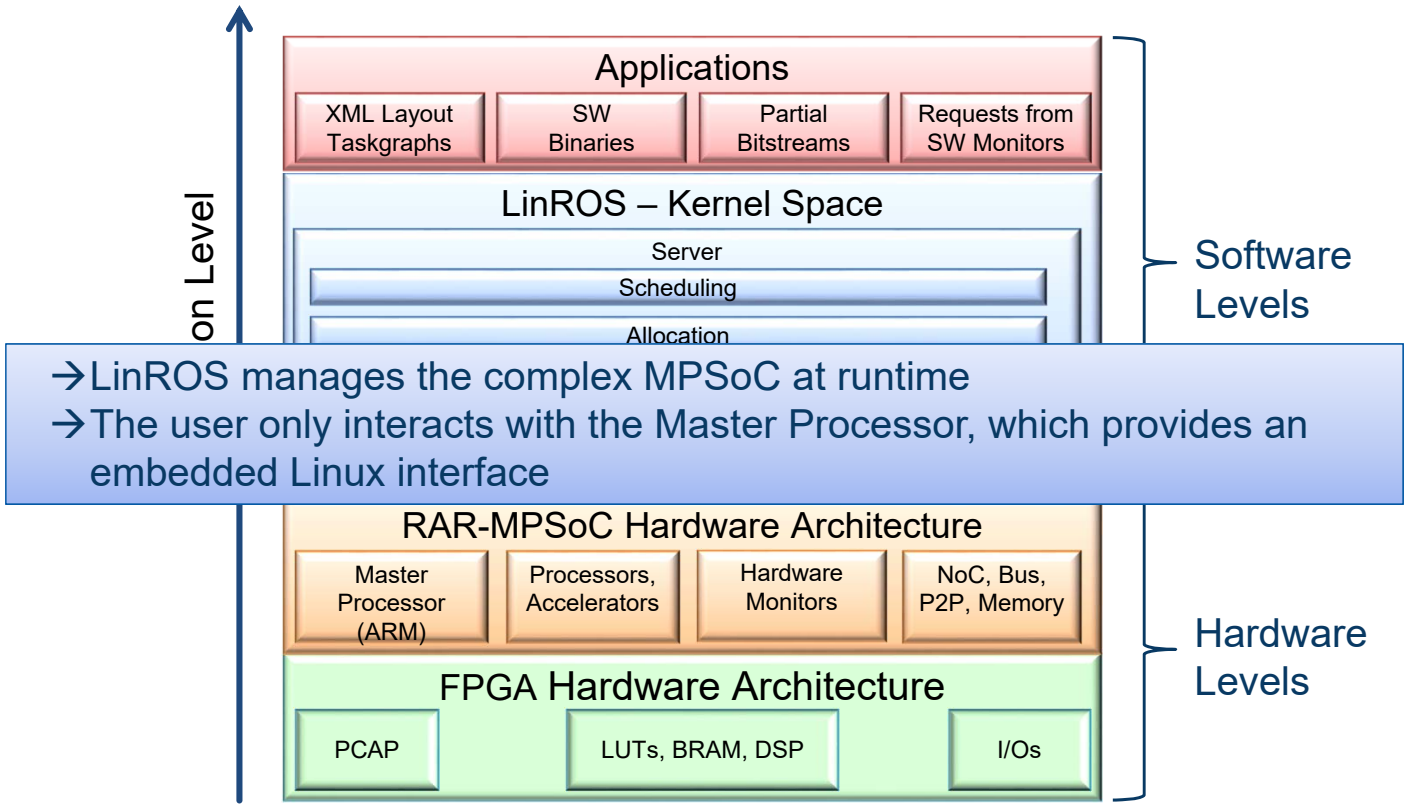
DRESDEN concept

- Research Topics
- Introduction and Motivation
  - Multicore Architectures
  - Requirements of Autonomous Systems
- Adaptive Multicore Systems / Multiprocessor Systems-on-Chip (MPSoCs)
  - Hardware Architecture
  - Design / Programming Tools
  - Software Architecture and Runtime/Operating Systems
- Application Examples: Automotive, Robotics and Drones
- Conclusion and Outlook

Linux-based Runtime System: LinROS



Linux-based Runtime System: LinROS



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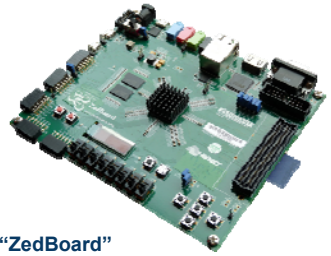
Advanced Driver Assistance System

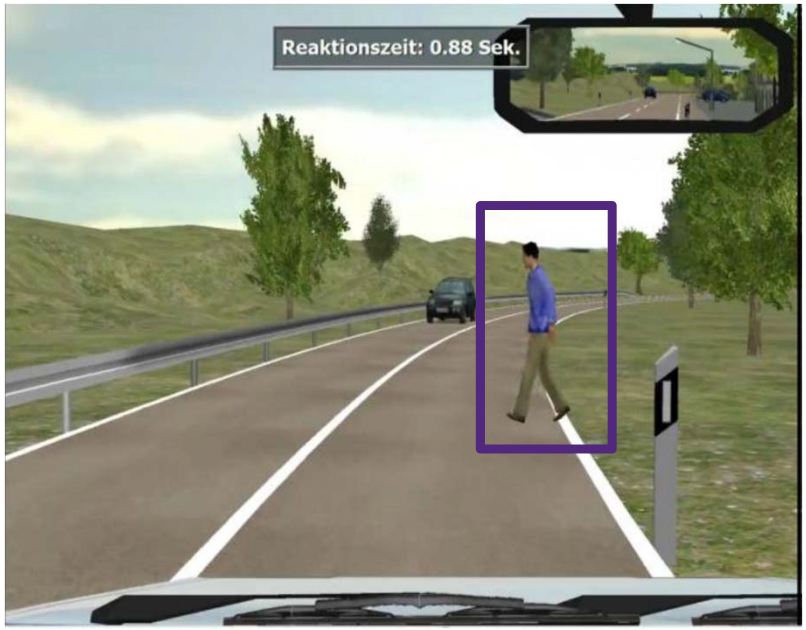
DRESDEN concept

Pedestrian Detection: Introduction

- Histogram of Oriented Gradients (HoG Algorithm)
- Optimized SW version on ARM Multi-Core Processor
- Optimized HW accelerator on FPGA



"ZedBoard"



Pedestrian Detection using the HoG Algorithm

J. Rettkowski, A. Boutros, D. Göhringer (2015) Real-Time Pedestrian Detection on a Xilinx Zynq FPGA using the HOG Algorithm. In Proc. of the International Conference on Reconfigurable Computing and FPGAs (ReConFig), Cancun, Mexico, Dec. 2015. (**Best Application Paper Award**)

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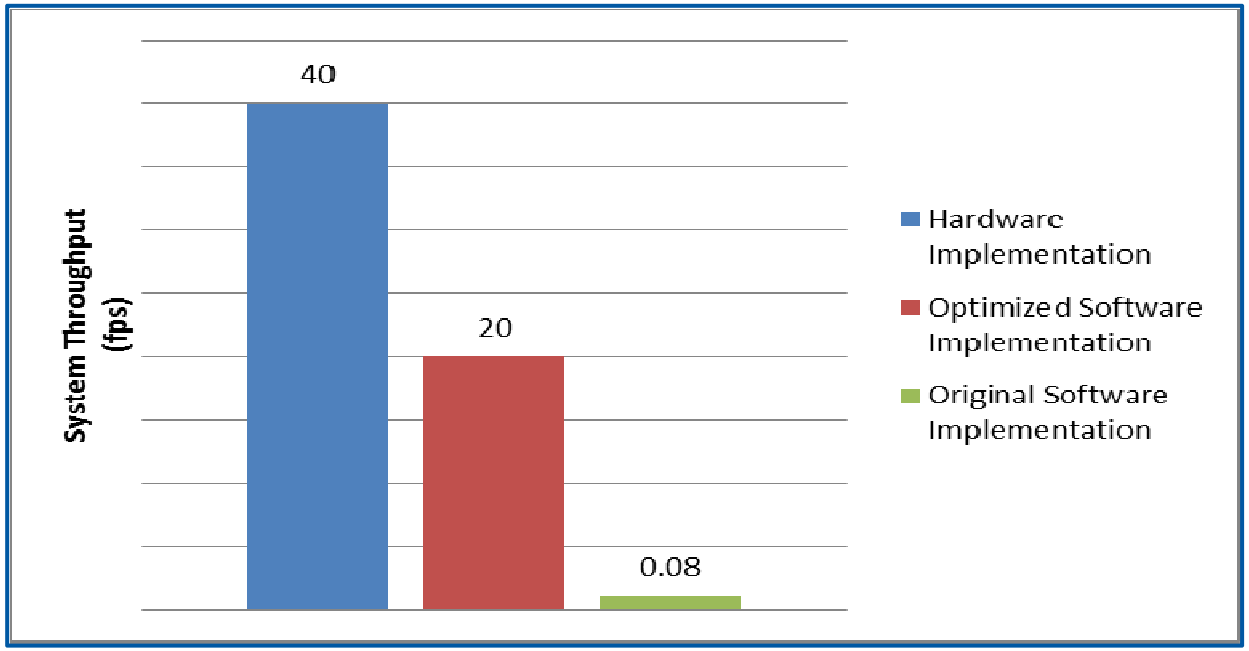
Advanced Driver Assistance System

DRESDEN concept

Pedestrian Detection: Performance



FPGA-based approach is clocked by **82.3 MHz → 40 fps**
Processor-based approach uses an ARM dual processor with **666 MHz → 20 fps**

J. Rettkowski, A. Boutros, D. Göhringer (2015) Real-Time Pedestrian Detection on a Xilinx Zynq FPGA using the HOG Algorithm. In Proc. of the International Conference on Reconfigurable Computing and FPGAs (ReConFig), Cancun, Mexico, Dec. 2015. (**Best Application Paper Award**)

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Advanced Driver Assistance System

DRESDEN concept

Pedestrian Detection: Hardware-Resources

Module	LUTs	Slices	DSPs
Luminance Calculation	59	17	0
Gradient Computation	2985	797	0
Gradient Magnitude and Direction	8432	2397	4
Formation of Cell Histogram	6140	1676	0
Block Normalization	1278	421	0
Binarization	93	26	0
AdaBoost Classifier	2310	608	0
Total	21297 (40%)	5942 (45%)	4 (2%)

J. Rettkowski, A. Boutros, D. Göhringer (2015) Real-Time Pedestrian Detection on a Xilinx Zynq FPGA using the HOG Algorithm. In Proc. of the International Conference on Reconfigurable Computing and FPGAs (ReConFig), Cancun, Mexico, Dec. 2015. (**Best Application Paper Award**)

H2020-Project: TULIPP (2016 – 2019)

Towards Ubiquitous Low-power Image Processing Platforms

Reference Platform Concept for Image Processing Applications: Bringing energy efficiency from chip level to system level through:

- Heterogeneous Hardware
- Toolchain
- Operating System

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H2020-Project: TULIPP (2016 – 2019)

Towards Ubiquitous Low-power Image Processing Platforms

Use Cases

- **Unmanned Aerial Vehicles** (Fraunhofer IOSB):

  More intelligence through an energy- efficient and small on-board controller

- **Medical Imaging** (Thales):

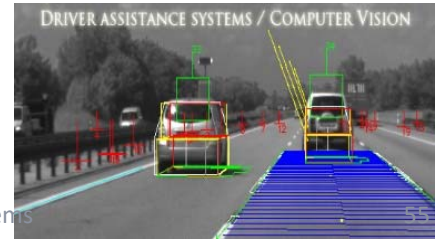
  Radiation dose reduction in surgical X-ray systems through real-time image processing

- **Automotive** (Synective Labs):

  Reliable, affordable and low latency image processing with hard real-time constrains

Surveillance and Rescue UAVs

Medical X-Ray Imaging



Advanced Driver Assistance

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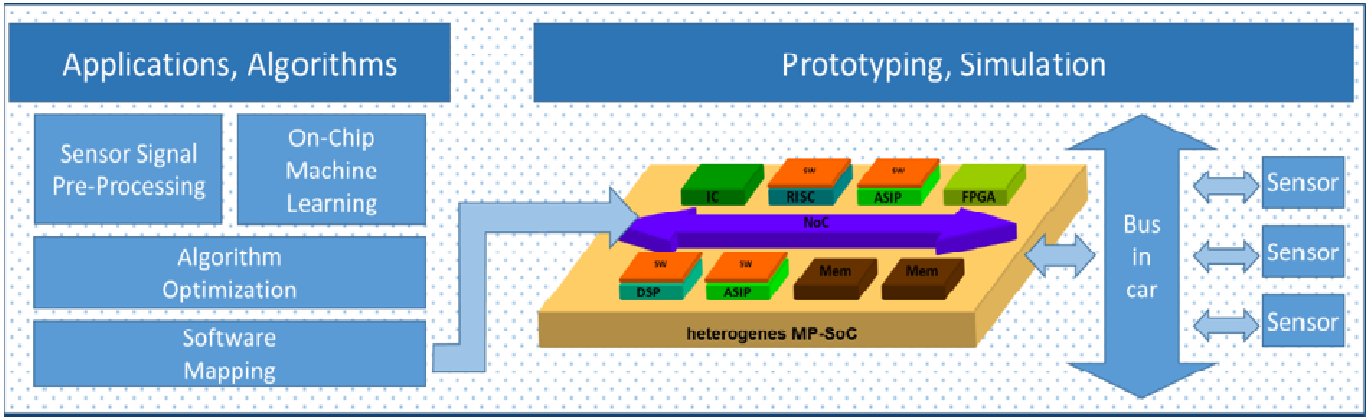
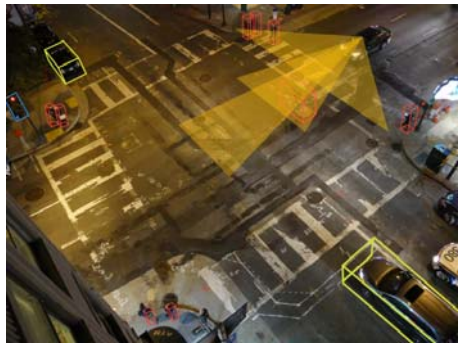
DRESDEN concept

BMBF-Project: PARIS (2017 – 2020)

Parallel Implementation-Strategies for Highly Automized Driving



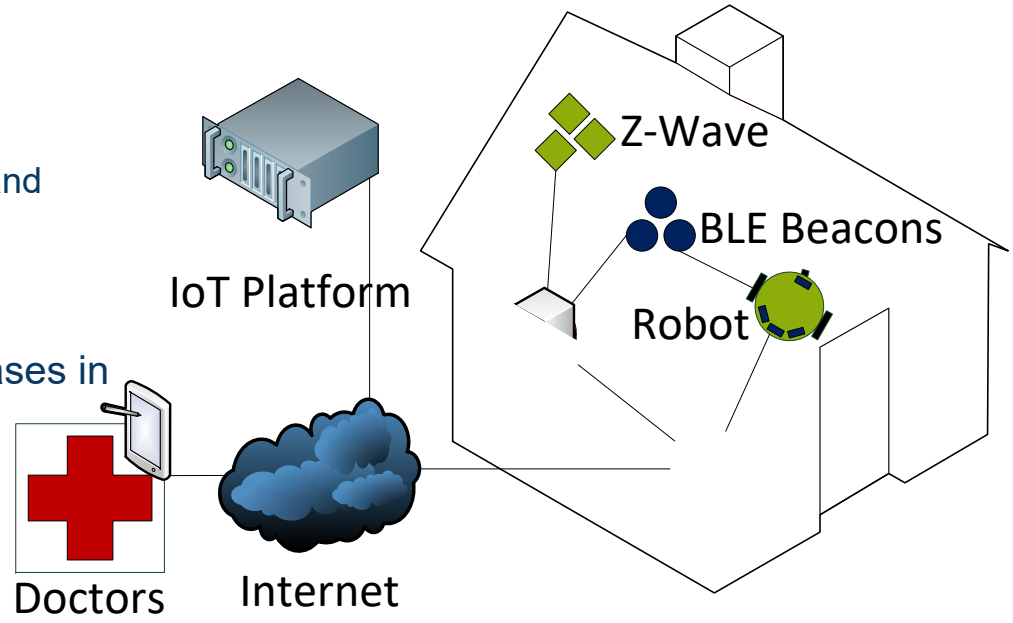


H2020-Project: RADIO (2015 – 2018)
Robots in Assisted Living Environments

A Cyber-Physical System [*] that combines

- Robots
- Smart home technology
- Wireless sensor networks and
- Decision making

For supporting elders and persons with chronic diseases in their daily home activities

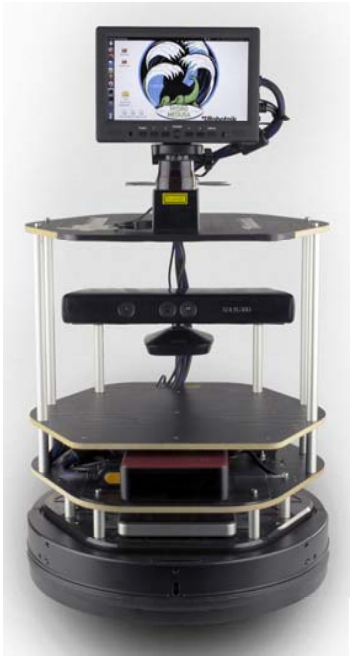


H2020-Project: RADIO (2015 – 2018)

Robots in Assisted Living Environments

Detection of

- Activities of the Daily Life (ADL)
- Mood conditions
- Early symptoms of cognitive impairment and
- Social exclusion



Including a mobile robot platform

- Central focus of interaction
- Offers assistance
- Combined with smart home automation
- Based on COTS
- Embeds recognition methods

→Reconfigurable MPSoC for energy efficient execution of recognition methods

→Distributed system based on ROS (Robot OS)

DFG SFB/Transregio: MARIE (2017 -2020)

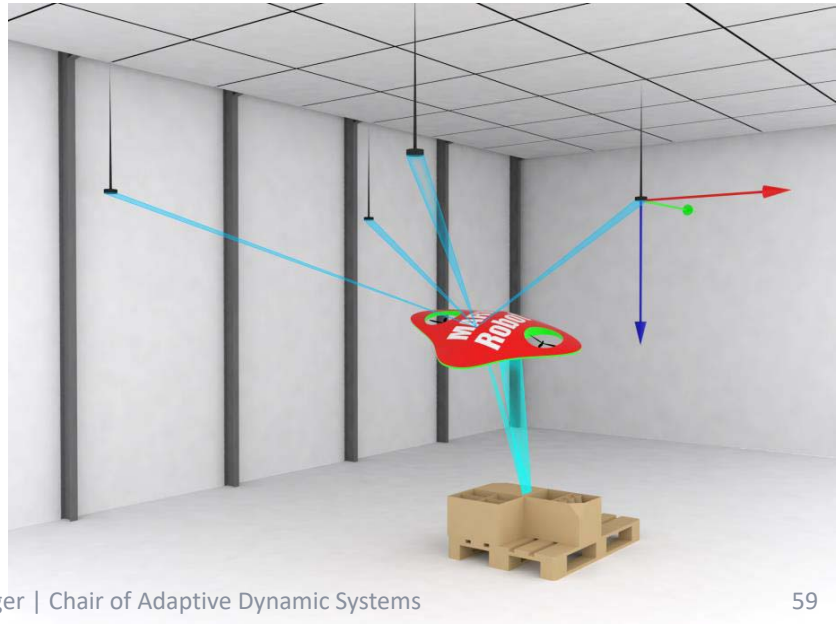
Mobile Material Characterization and Localization by Electromagnetic Sensing

Challenges:

1) THz wave propagation measurement, analyzation and modelling
2) Small sub-mm-wave transceivers
3) Material characterization
4) Material localization

Our Contributions:

- ➢ Real-time computing architecture
- ➢ Design and programming method
- → For enabling mobile material characterization and localization



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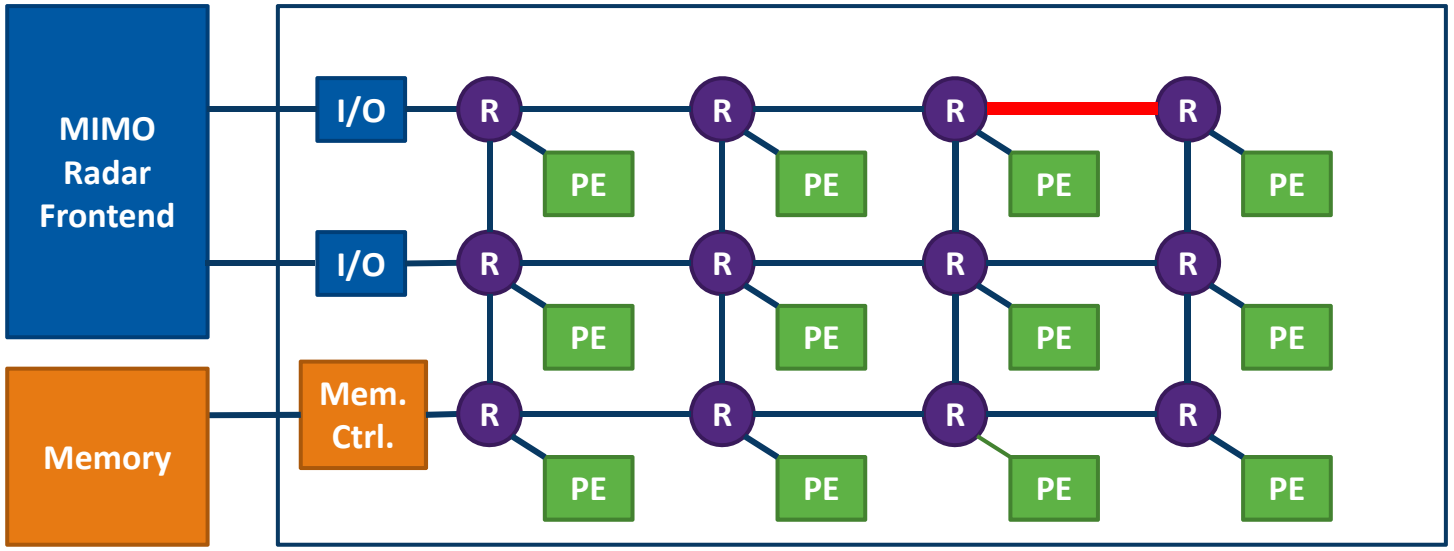
DRESDEN concept

DFG SFB/Transregio 196: MARIE (2017-2020)

Mobile Material Characterization and Localization by Electromagnetic Sensing

Real-Time Massive MIMO THz Computing Architecture



I/O: Input/Output R: Router Mem. Ctrl.: Memory Controller PE: Processing Element

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DRESDEN concept

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Conclusions

DRESDEN concept

- Reconfigurable Multiprocessor Systems-on-Chip
  - **High flexibility** → Hardware and software can be adapted at design- and at runtime to the application requirements, such as data throughput, real-time, safety
  - **High performance** → Application-specific architecture
  - **High energy efficiency** → On demand functionality, better area utilization by hardware task multiplexing
  - **Problem oriented tool flow** → Can be easily adapted to new applications / standards

TECHNISCHE UNIVERSITÄT DRESDEN

Outlook

DRESDEN concept

- Development and support of other/new:
  - Architecture components
  - Design methods and tools
  - Runtime management systems
- Evaluation with further application domains
- Further research projects/collaborations are planned/under review

Ausblick: Weiterführende Lehrveranstaltungen

- **Vorlesungen:**
  - Einführung in die Technische Informatik Teil 1: HW/SW Codesign (WiSe, 4/2/2)
  - Hardware Modellierung und Simulation (WiSe, 2/0/2 SWS)
  - Entwurf und Programmierung Eingebetteter Multicore Architekturen (SoSe, 2/2/0 SWS)
- **Hauptseminar:** Adaptive Computing Systems
- **Komplexpraktikum:** Programmierung und Hardwareentwurf für Rekonfigurierbare Rechensysteme

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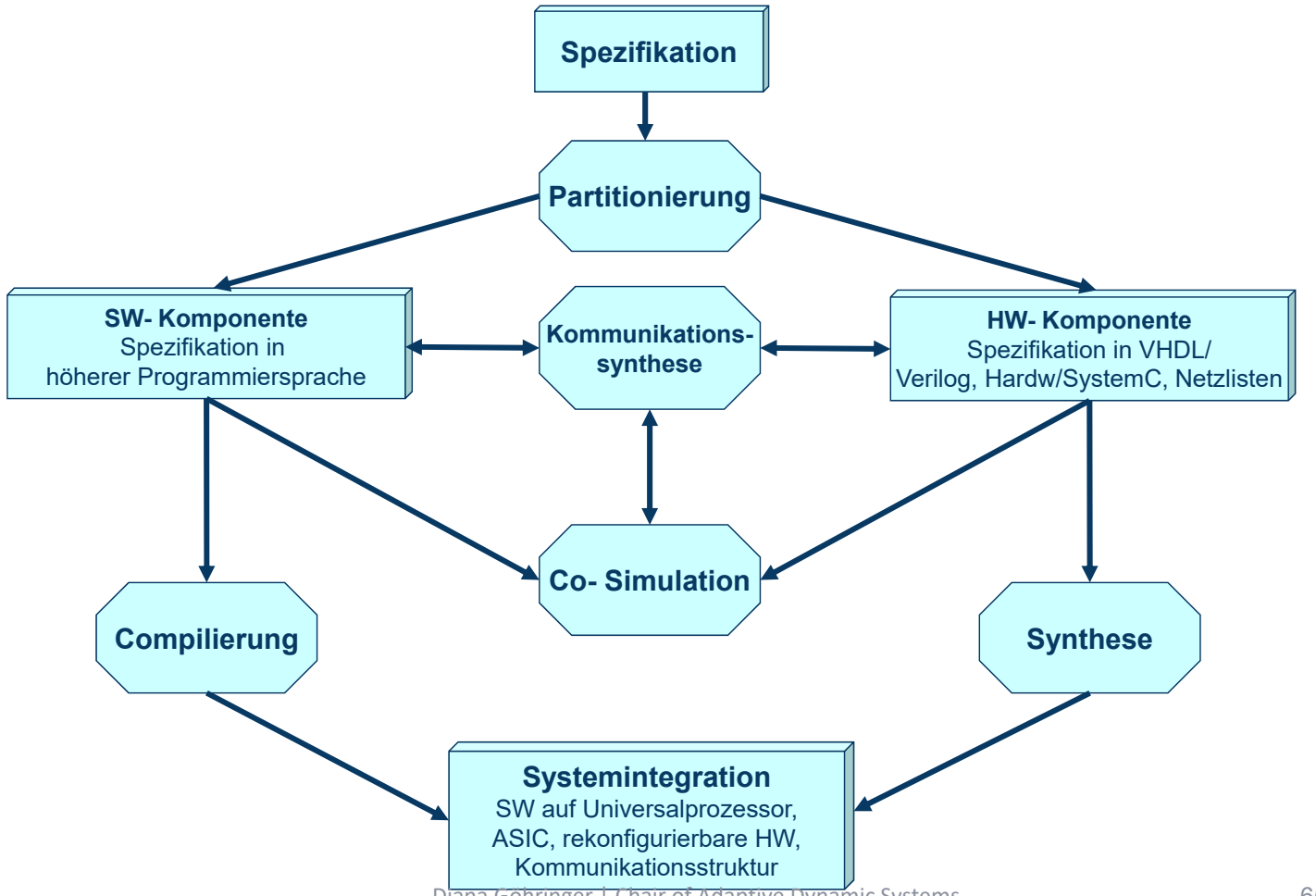
Einführung in die Technische Informatik
Vorlesung Teil 1: HW/SW Codesign

DRESDEN concept



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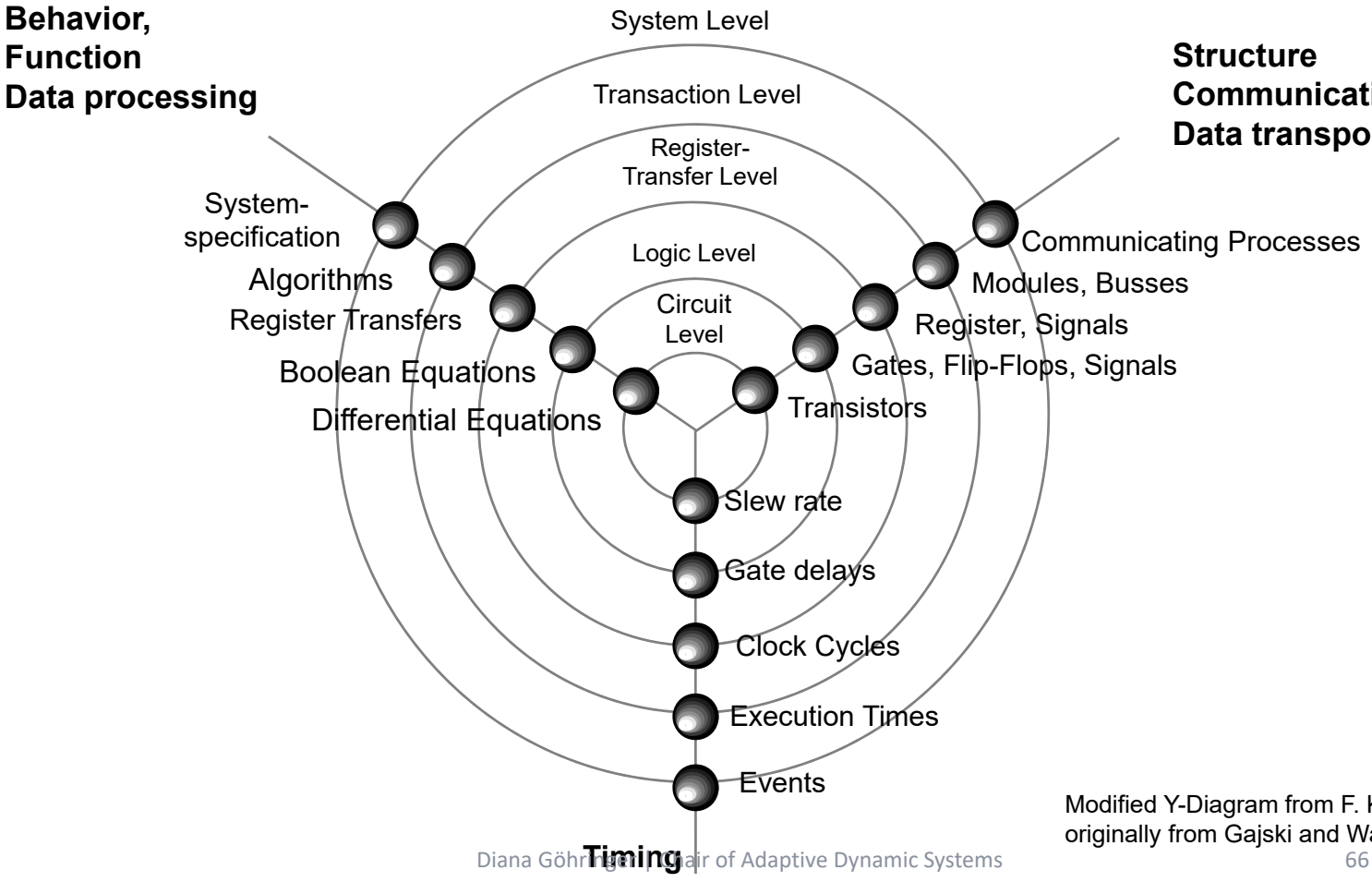
Vorlesung Hardware Modellierung und Simulation (WiSe)

DRESDEN concept



Modified Y-Diagram from F. Kesel, originally from Gajski and Walker

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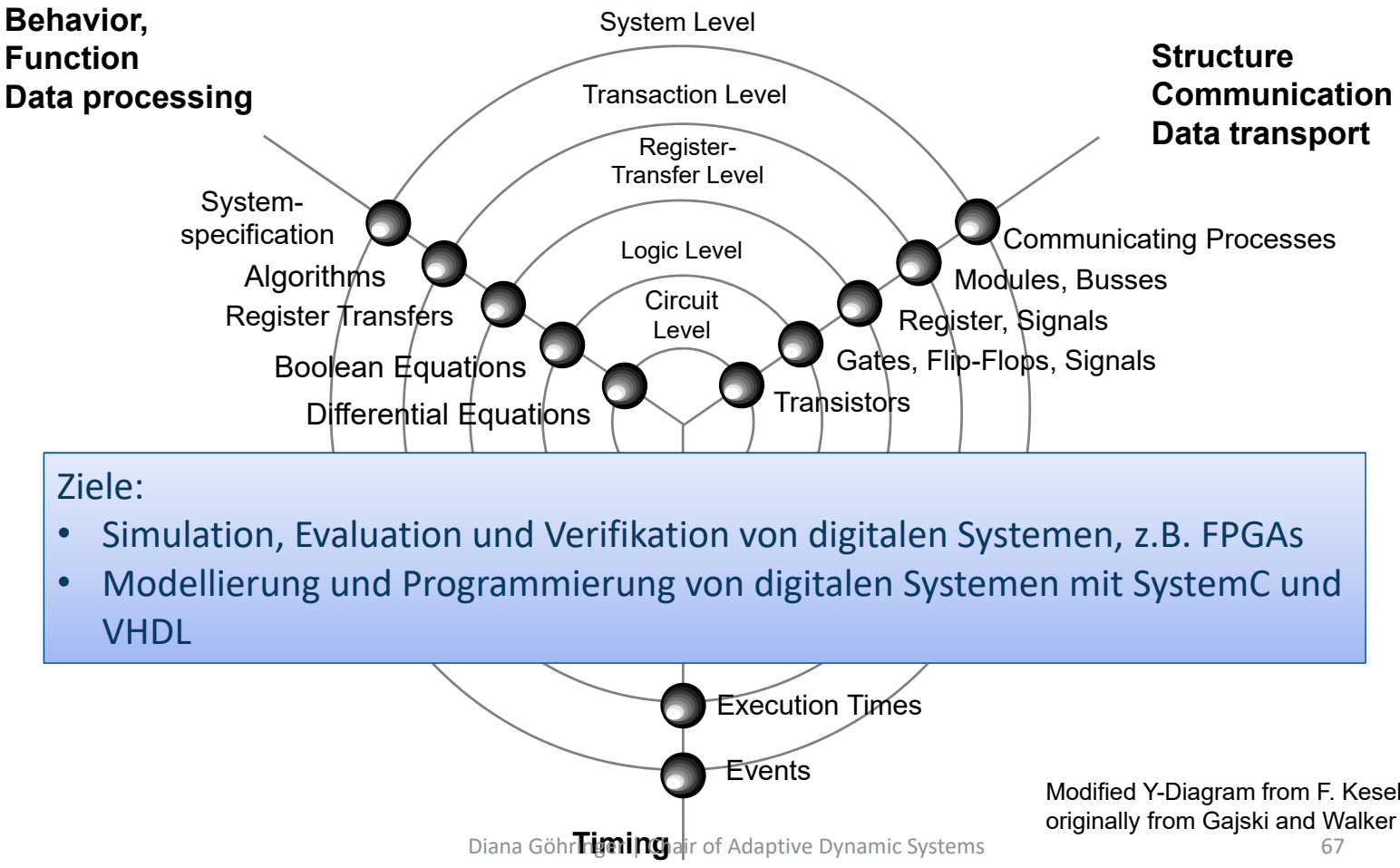
Vorlesung Hardware Modellierung und Simulation (WiSe)

DRESDEN concept



Ziele:

- Simulation, Evaluation und Verifikation von digitalen Systemen, z.B. FPGAs
- Modellierung und Programmierung von digitalen Systemen mit SystemC und VHDL

Modified Y-Diagram from F. Kesel, originally from Gajski and Walker

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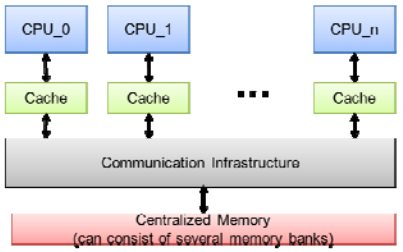
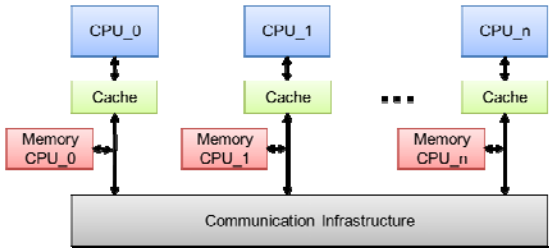
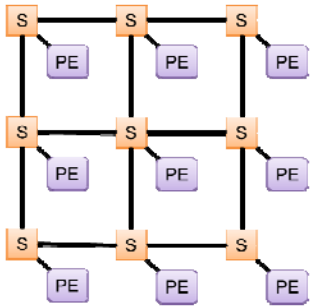
Vorlesung: Entwurf und Programmierung Eingebetteter Multicore Architekturen (SoSe)

DRESDEN concept

- Eingebettete Systeme / Cyber-Physikalische Systeme
- Eingebettete Multicore Architekturen
  - Speicherstrukturen
  - Kommunikationsinfrastrukturen (Bus, Network-on-Chip)
- Simulatoren/Virtuelle Plattformen für Mehrkernarchitekturen
- Programmierung (z.B. Pthreads, OpenMP)
- Eingebettete Betriebssysteme (z.B. Embedded Linux, FreeRTOS)







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Thank you! Questions?

DRESDEN concept

Contact:

Prof. Dr.-Ing. Diana Göhringer

Chair of Adaptive Dynamic Systems
TU Dresden, Germany

Email: diana.goehringer@tu-dresden.de
www: http://www.tu-dresden.de/inf/ads