Acceleration of Signal Processing Kernels on FPGA

Tasks:

- Understanding the required signal processing algorithms and profiling them
- Implementing the accelerator using HLS or HDL, like [1]
- Testing the accelerated algorithm on the board and evaluating the results

Required skills:

HDL (Verilog or VHDL), HLS, C/C++

Being Familiar with Machine Learning

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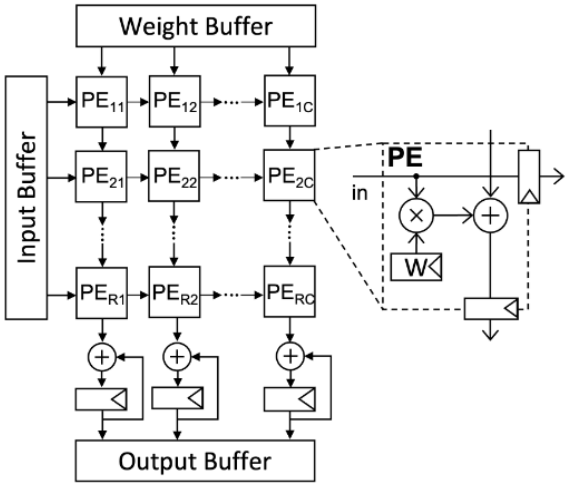

[1] Systolic array-based accelerator

[1] C. Peltekis et al., "ArrayFlex: A Systolic Array Architecture with Configurable Transparent Pipelining," *DATE*, 2023