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From Hardware Trace to System Knowledge

Data-intensive Hardware Trace Analysis

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TU Dresden, 25.04.2012

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Outline

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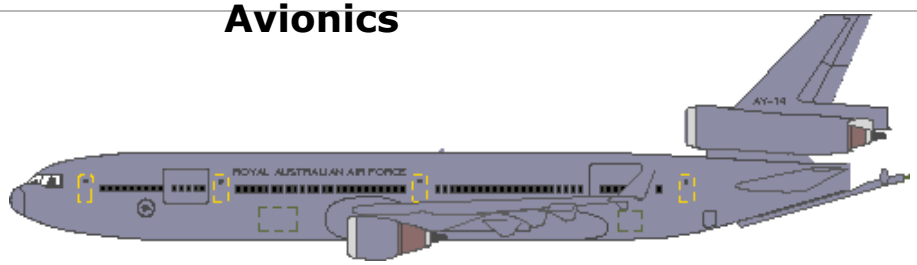
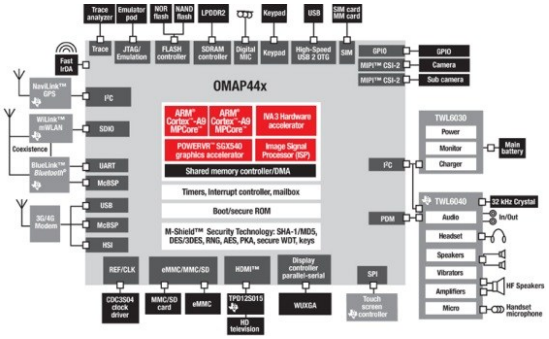
Industrial technologies

Avionics



Green IT

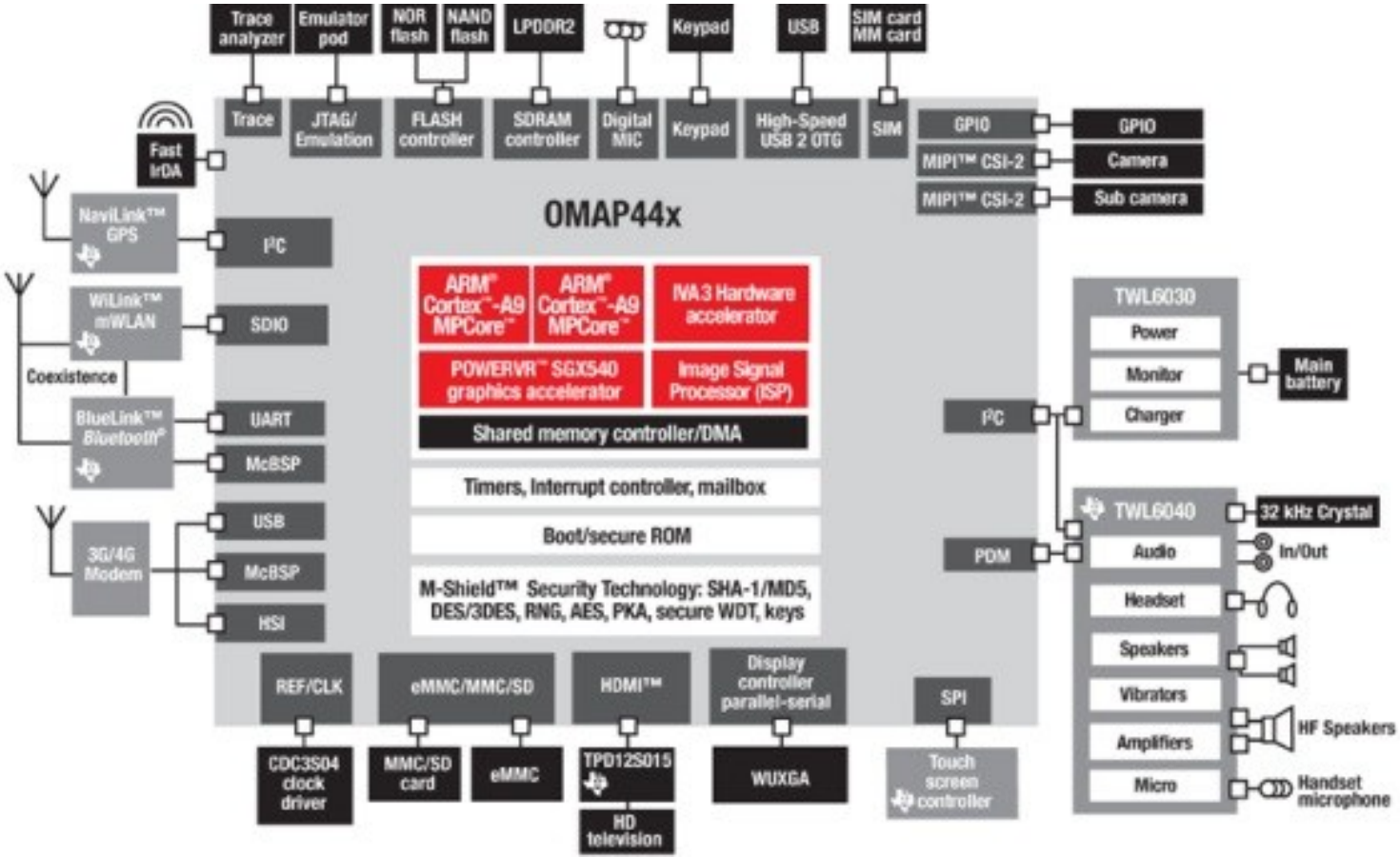


Medical technologies

Mobile Devices

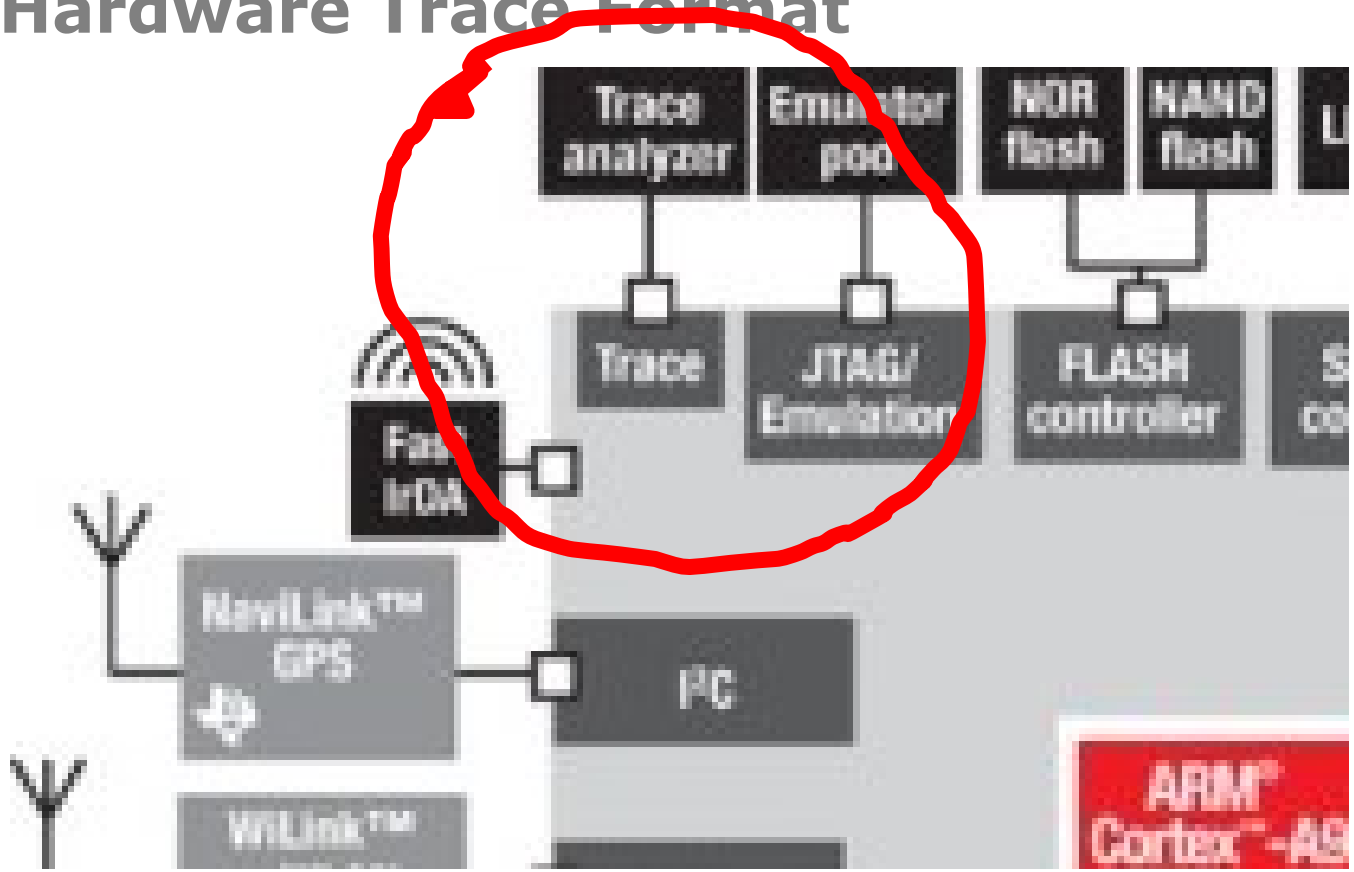
Automotive

Hardware Trace Format



Img 1: OMAP 44x ARM® Ltd. [1]

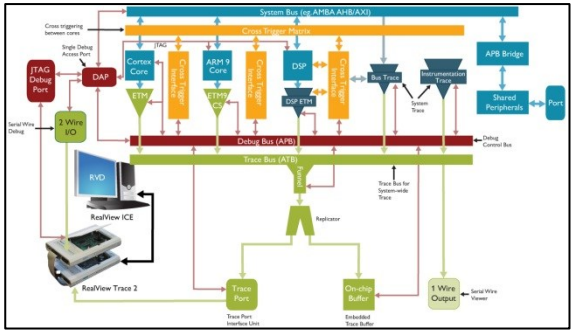
Hardware Trace Format



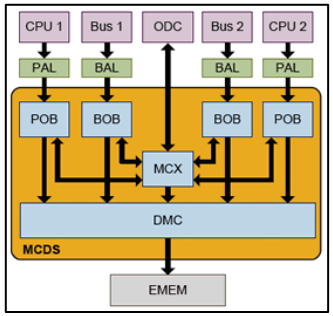
Img 1: OMAP 44x ARM® Ltd. [1]

Multiple Vendor Solutions

- ARM® CoreSight™ / ETM ™
- Infineon Multi-Core-Debug-Solution (MCDS)
  e.g. TriCore TC1797ED
- Nexus IEEE-ISTO 5001
  e.g. PowerPC Aurora Nexus Trace



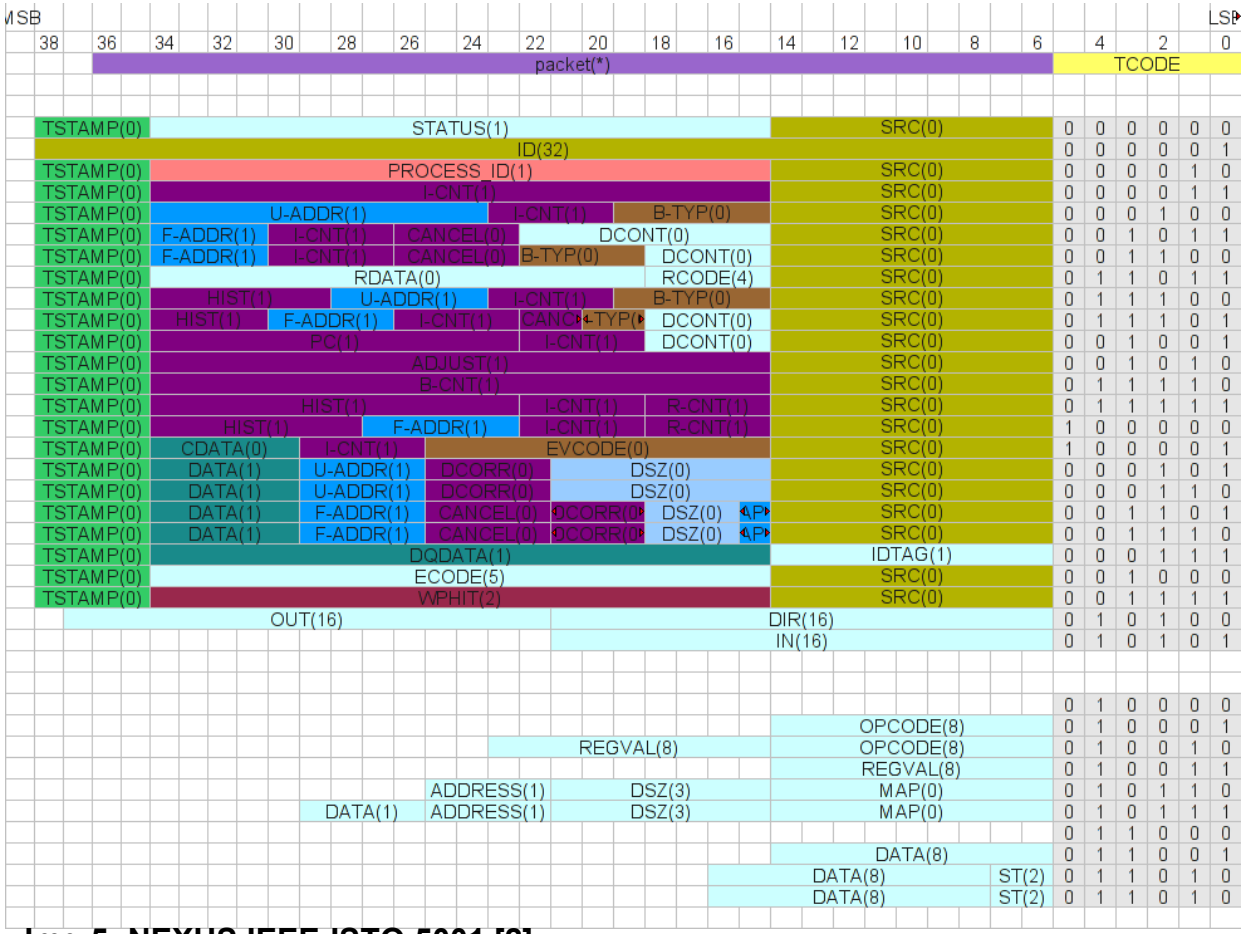
Img 2: CoreSight™ ARM® Ltd. [1]



Img 3: MCDS [3]

Img 4: NEXUS IEEE-ISTO 5001 [2]

Packet based



Img 5: NEXUS IEEE-ISTO 5001 [2]

Hardware Trace Content

Analysis POV	IEEE-ISTO-5001 (NEXUS) Features: Program Trace	Data Trace	Device ID	Ownership Trace	Watch-points	Run/Trace Control
Control Flow Trace	X		X	X		
Data Flow Trace	(X)	X	X	X		
Performance Counter	(X)		X	X	X	
Run/Trace Control						X

Breakpoints and other Features are summarized in Run/Trace Control.

Hardware Trace Amount

- EEMBC Benchmarks [6]
  - Cycle accurate Program and Data Trace
  - 20M Ticks covered; 100ms Program Execution
  - 28MiB Trace Data
  - ➢ **315 MiB/s on 100MHz Embedded PowerPC Processor**

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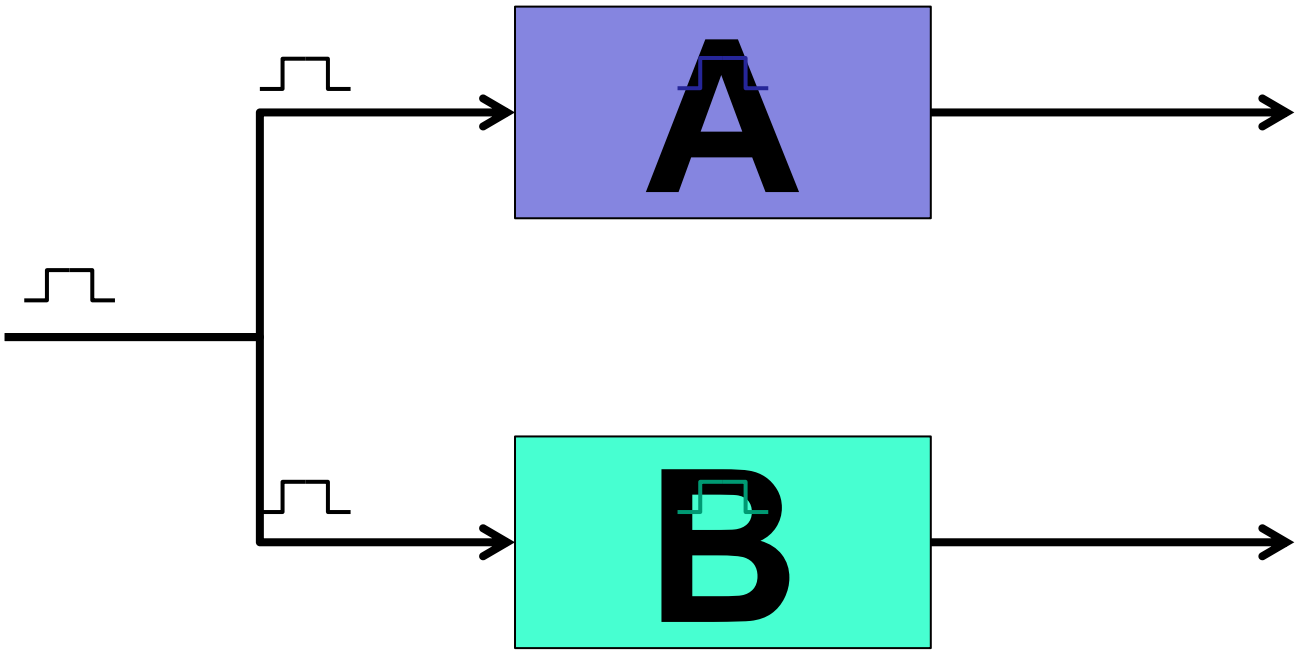
Current Hardware Trace Analysis

- Single-Core Call Graph / Timeline
- Code Coverage
- Counter Timeline
- Basic Statistics (Minimum, Maximum, Average)

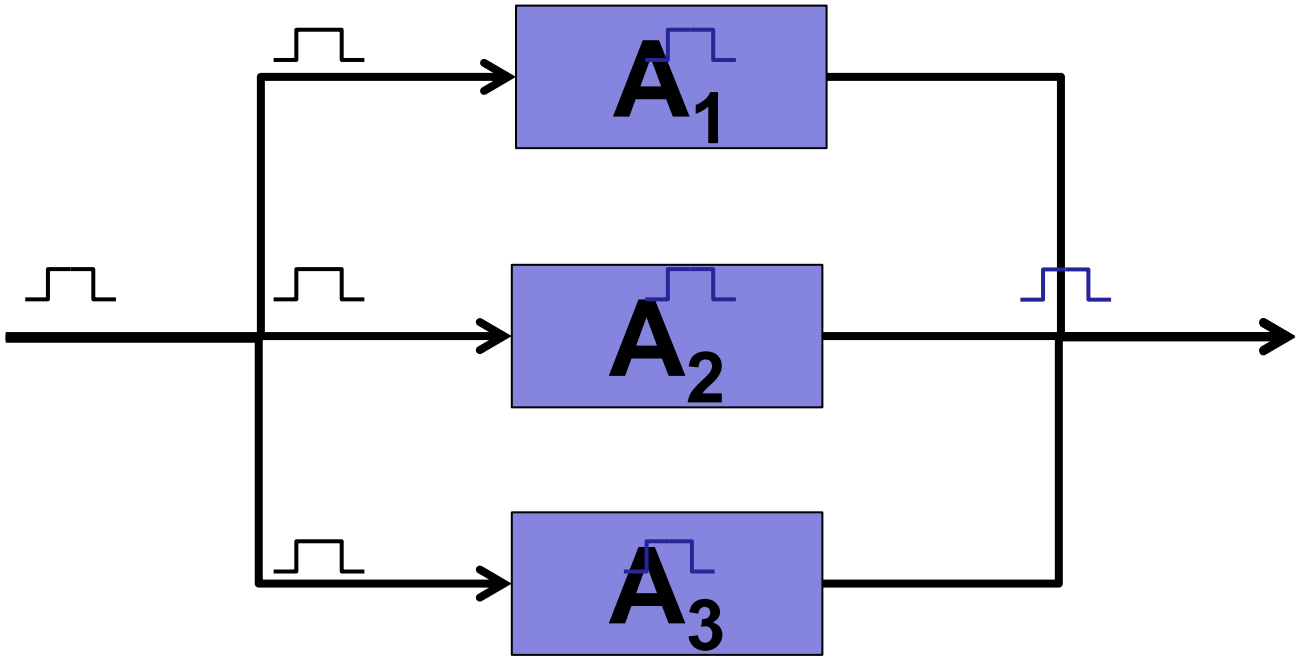
Learning from Software Trace Analysis [5]

- Multi-Core Call Graph / Timeline
- Extended Statistics (Distribution, Coherence etc.)
- Counter-Arithmetic
- Multi-dimensional Counter Timelines / Surface Plots
- Machine Learning Algorithms
- Graph based Analysis (WCET etc.)
- Pattern Matching
- Model Verification
- Communication analysis
- Data for external Tools
- …

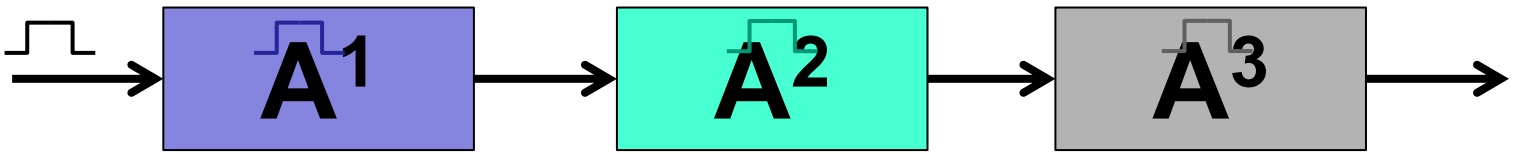
Function-Parallel Trace-Analysis



Data-Parallel Trace-Analysis



Function Pipeline Trace-Analysis

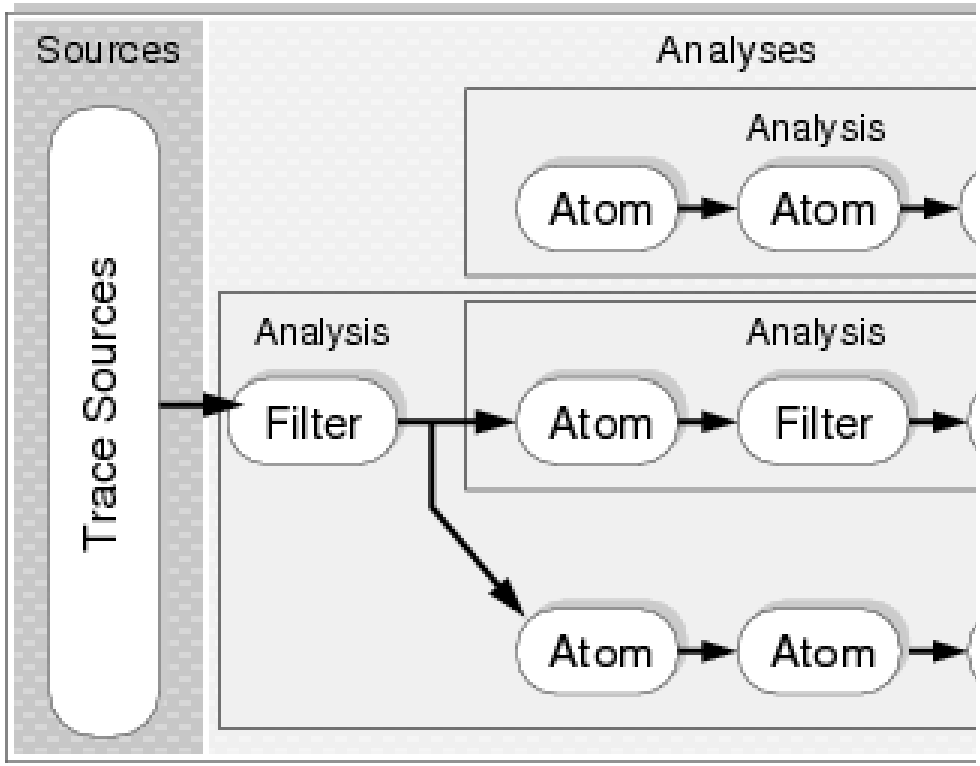


Outline

Objectives

- High Performance Analysis
  - Near Real-Time
  - Parallel and Scalable
- Vendor Independent Trace Format
- Caching or Storage of Intermediate and Final Results
- Interoperability and Independence of Analyses and Atoms
- Interoperability with external Tools

Framework Structure



Img 6: Trace Analysis Framework Structure

- Analysis split into Atoms
  - Combine Atoms
  - Independence of Execution
- Universal Trace Format
  - HW / SW Trace
  - Analysis-Oriented
  - Simple Compression
  - Conversion into SW-Trace Format
- Intermediate and Final Results can be stored

Outline

Conclusion

- Demands on Hardware Trace Analysis are rising.
  - Need for high performance and scalable Trace Analysis
  - Decomposition and Arrangement of Analyses
  - Potential for automated Analysis
- Hardware Platform independent Trace Analysis
  - Single Trace Format
  - Defined Interfaces
  - Analysis independent from Framework implementation
- Flexible Data-Management
  - Store of Final and Intermediate Results in Trace Format
  - Input / Output from Trace-Database
  - Conversion of Trace-Data into other Trace-Formats

Future Work

- Finish Framework
  - Implement Basic Analysis
  - Implement Visualization Components
- Implement simple Analysis in programmable Hardware (FPGA)

Outline

References

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(2) (Mar 2012) NEXUS 5001 Forum, http://www.nexus5001.org , [online], http://www.nexus5001.org/sites/default/files/waffles_logo.gif

(3) (Mar 2012) IPextreme, http://www.ip-extreme.com/IP/mcds.shtml, [online], http://www.ip-extreme.com/images/products/MCDS_Diagram3.gif

(4) (Sep 2008) ARM Ltd., William Orme, „*Debug and Trace for Multicore SOCs*“, Whitepaper, http://www.arm.com/files/pdf/CoresightWhitepaper.pdf

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