The Hardware Design Toolchain

Approaches and State of the Art

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We will hate the tools (FCCM 1996 prediction for 2001)

We will still hate the tools (FCCM 1998 prediction for 2003)

We will merely dislike the tools (FCCM 2000 prediction for 2005)

We [will] hate the tools more (FCCM 2007 prediction for 2012)

Outline

Why bother?

- Complexity of . . .
  - . . . designs
  - . . . the design process
- Tools are . . .
  - . . . rarely known to developers
  - . . . of unknown usefulness
  - . . . (not?) adequate?

HDLs: General

Everything below RTL is often specific to the HW-vendor
$\rightarrow$ HDLs also serve as interfaces

- VHDL
- Verilog
- SystemC, ABEL, JHDL...

HDLs: VHDL and Verilog

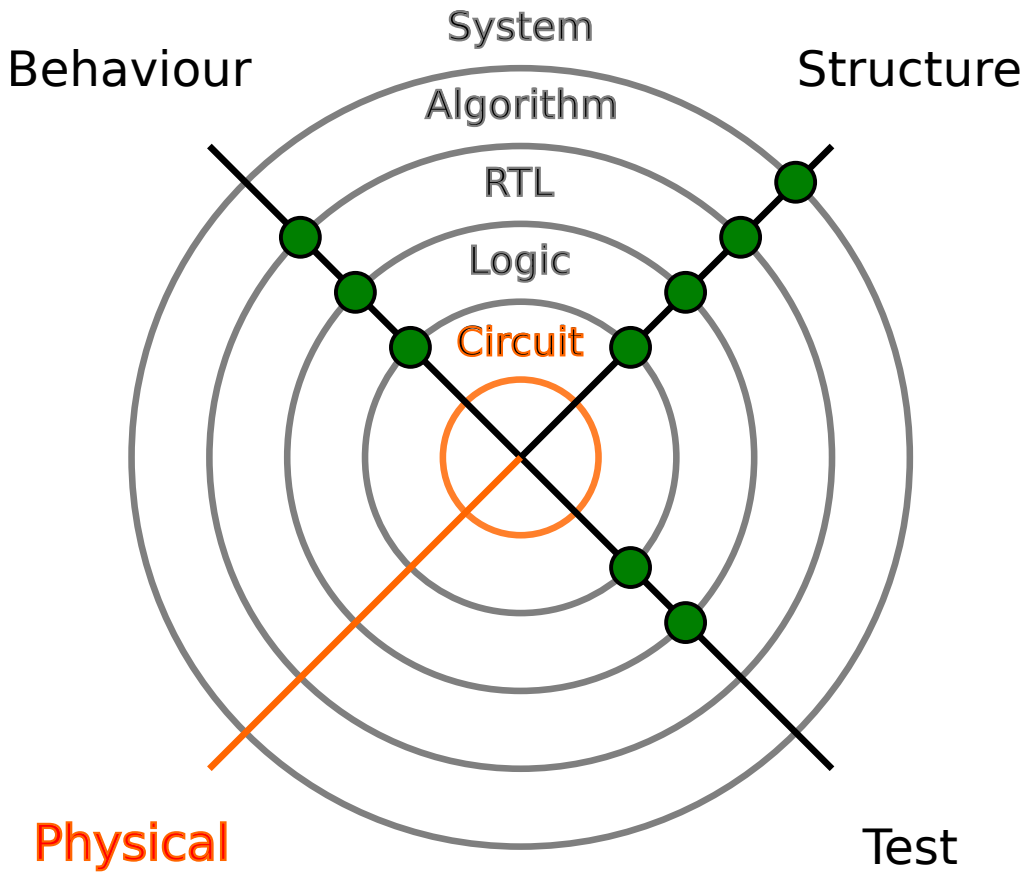
Most commonly used HDLs.
VHDL...

- ...originated from *Ada*
- ...can cover structure, behavior and some testing
- ...is consequently very complex

Verilog...

- ...is extended to *SystemVerilog*
- ...resembles *C*

The extended Gajski-Kuhn Chart



Criteria for Tool Evaluation

- The field of application [5].
- The design of human interaction
- Availability and openness
- Tool-chain integration capabilities

Specification: Why dedicated tools?

Specification is tightly linked to verification.
Verification should be done by automated tools.
→ Specification should be formalized and machine-readable.

Specification: Where are we now?

- State of the art
  - Text, tables, graphics
  - not formalized at all
- Approaches
  - try UML [1]
  - embed spec. in *VHDL* [11]
- . . . purely academic

HLS from High-level Languages

Idea

Write in an HLL, like you do with software.
Let the tools do the rest...

- *C/C++* [13]
- *Haskell* [3][12]
- *Java* $\rightarrow$ JHDL
- *Matlab* [2]

Approach: Evolutionary Algorithms

Idea

Only describe the environment conditions.
Let the algorithm figure out the best solution.

- Might work for optimization
- Not useful for new designs
- Purely academic for now. [8]

HLS by Dedicated Tools

Idea

Have a tool for each specific part of the design.
Control it by providing some parameters.

FloPoCo[4]

. . . is a generator for arithmetic cores for FPGAs

HLS from Visual Representations

Idea

Design by placing and connecting components using a GUI.
Translate the resulting layout into an HDL.

Show-off

Qucs

Editing Tool Requirements

Editing tools should help to tame the complexity of HDLs.

- Different views on design
- *Code* navigation
- *Code* completions
- Shortcuts for repeated tasks
- *Code* refactoring
- Enforcement of conventions

Show-off

SigasiPro

Also: documentation

High design complexity
→ extensive user and developer documentation required
Documentation quality impacts productivity!

Available tools
VHDLDoc, *doxygen-VHDL*, *VHDocl*

Considerations on T+V

- No tools focused on HW-design T+V
- Tool-assisted verification requires formalized spec
- Testing very much limited to
  - runtime assertions
  - waveform inspection
  - (JTAG)

State of the Art

Testing

Whatever your HDL offers you. . .

Verification

SPIN [10], HDL features

Chaining: Why bother?

One tool can not cover the whole design process.
But. . .

Behold!

One-vendor-to-rule-them-all-policies

Figure: Source: wikipedia

Difficulties when creating Toolchains

- Communication between tools in the chain → exchange formats
- Specialized tools rarely support many formats
- Chain needs to be set up manually

The true chore

Which tool is the right one?
Does my tool fit in the chain?

Exchange formats

- EDIF
  - Attempt to create industry standard (1985)
  - State: abandoned
- BLIF
  - Attempt to create academic standard (1992)
  - State: rarely used at best
- some HDL
  - limited to capabilities of the HDL

Open Source: Why bother?

- Tools can get widespread
- Closer interaction Developer $\leftrightarrow$ User
- Less effort for customization
- High number of potential developers

Disclaimer

Complex tools need high initial effort

What is out there?

Design	Qucs, fritzing
HLS	JHDL + JHDL-CAD [7]
Simulation	GHDL, FreeHDL
Below RTL	ABC [6], open HW-Platforms [14]

Suggested Improvements (by others)

- Formulation (Specification)
- Resource and Performance prediction
- Modeling techniques
- Bridge between formulation and design phase
- Reduced translation and routing times
- also see [9]

Suggested Improvements (by me)

- user interaction, usability
- content awareness
- chaining capabilities
- openness...

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