TECHNISCHE UNIVERSITÄT DRESDEN

INTERMEDIATE REPORT: BELEG

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Section 1

Introduction to the Problem

What am I working on?

01 Problem Statement

Topic

Graphical Support for the Design and Evaluation of Configurable Logic Blocks

Aim: Have a tool(-chain) that allows to

- Create Schematics of CLBs
- Find the mappings of given boolean functions onto these CLBs
- Visualize the found mappings

(Restricted to combinatoric circuits for now.)

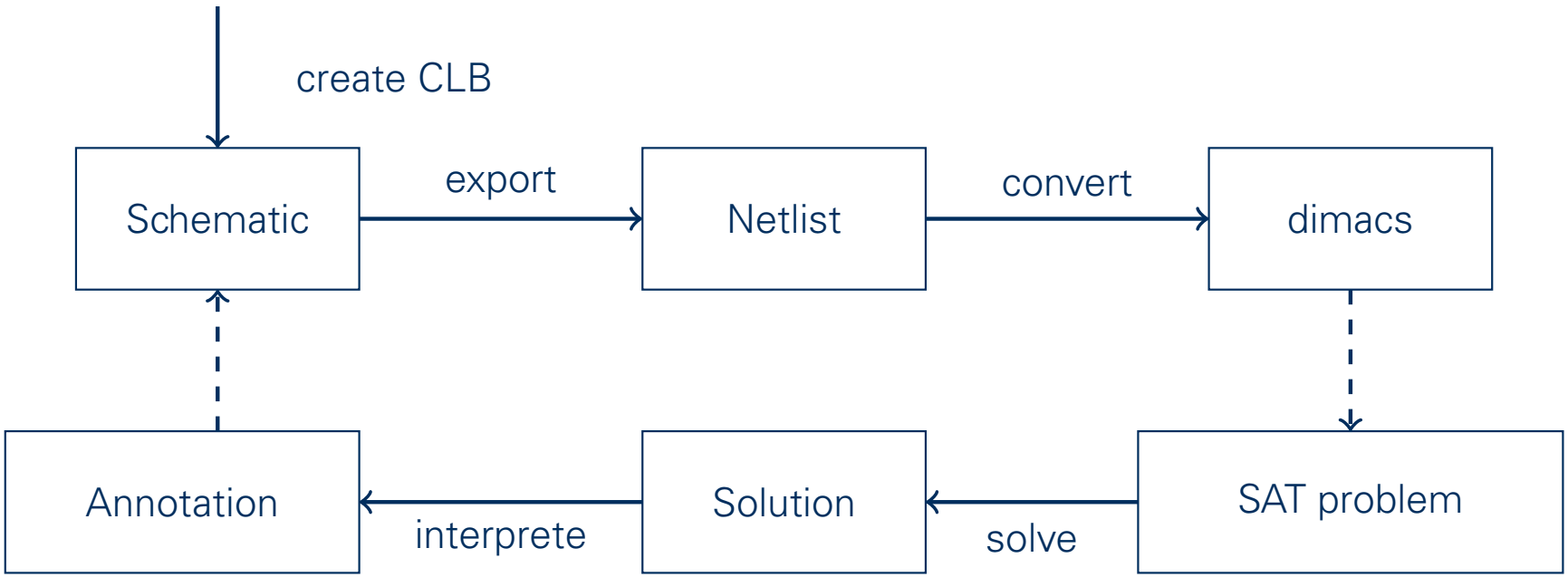
01 The Plan

1. Get accustomed to boolean mapping[5][4]
2. Find a tool chain
3. Research ways of integrating the work flow into existing tools
4. Implement a GUI-based tool chain/ Expand an existing tool chain

Section 2

State of my Research

02 The Work Flow



02 Concerning Feasibility

- Hand-crafted netlist
- Convert netlist into `dimacs` using `BM`
- Use `minisat`[2] as SAT-solver
- Find an interpretation of the output

Verdict

It can be done by hand. Therefore, it should be possible to do it in an application as well.

02 Introducing QUCS

Quite **U**niversal **C**ircuit **S**imulator[3][1]

- Allows schematic design of analog and digital circuits
- Several kinds of applicable simulations
- Wide range of already implemented components

Why not extend this tool?

02 A look inside QUCS

- Serious design flaws
  - Complete abundance of structure and patterns
- Inferior code quality
  - 50 shades of C(++)

Verdict

Great to use, terrible to maintain and develop.

02 So?

Qucs' code gets better. . . [6]
. . . but not fast enough.
Search for useful alternatives yielded nothing.

02 So. . .

I will (have to) build my own GUI-tool

With feature restrictions and documentation

Section 3

Implementation Progress

03 Design Decisions

- Usage of `C++11` with
  - convenient, well documented tooling
  - abstracting system specifics while keeping the power of C++
- Separate visual representation from internal model
  - class dependency reduction → maintainability
- Component information not hard-coded
  - Allow user-created component libraries
- Use `minisat` as SAT-solver
  - integration capabilities, open source

03 Deciding on a Netlist Format

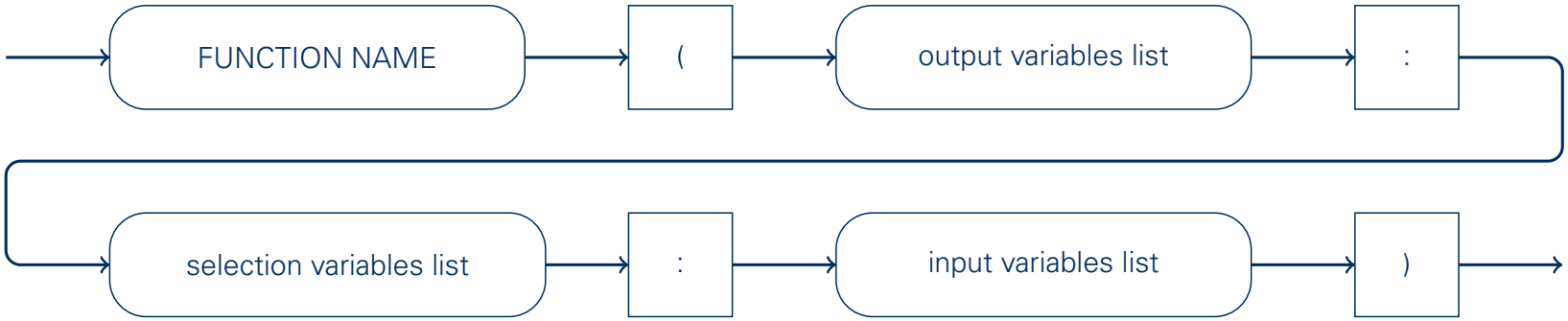


Figure : Syntax graph for a line in the intermediate netlist format

03 Example Netlist

```
# this is an example netlist comment

AND(and0_out0::and_in1, and0_out0)
MUX(mux0_out0:mux0_sel0:mux0_in1, mux0_in0)
CONNECT(and0_out0::mux0_sel0)
```

Section 4

Roadmap

A look into the crystal ball

04 Required Features

- Loading/Saving of projects
- Netlist generation
- `minisat` integration
- Backward annotation

04 Further Ideas

- Allow schematics to be used as components in other schematics
- Skip netlists and directly export dimacs
- Support components with generic parameters
- Convenience functions and usability

04 The (nearly) last slide

Git Repository: `https://github.com/fer-rum/q2d`

Bender is ©Matt Groening and David X. Cohen

04 Related Works I

M.E. Brinson and S. Jahn.

Qucs: A GPL software package for circuit simulation, compact device modeling and circuit macromodeling from DC to RF and beyond.
`http://www.mos-ak.org/eindhoven/papers/06_Qucs_MOS-AK_Eindhoven.pdf`, April 2008.

Niklas Eén and Niklas Sörensson.

An Extensible SAT-solver.
In Enrico Giunchiglia and Armando Tacchella, editors, *SAT*, volume 2919 of *Lecture Notes in Computer Science*, pages 502–518. Springer, 2003.

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The Hardware Design Toolchain - Approaches and State of the Art .
Technical report, TU Dresden, 2014.

Andrew C. Ling, Deshanand P. Singh, and Stephen Dean Brown.

FPGA PLB Architecture Evaluation and Area Optimization Techniques Using Boolean Satisfiability.
IEEE Trans. on CAD of Integrated Circuits and Systems, 26(7):1196–1210, 2007.

04 Related Works II

Sean Safarpour, Andreas Veneris, Gregg Baeckler, and Richard Yuan.

Efficient SAT-based Boolean Matching for FPGA Technology Mapping.
In *Proceedings of the 43rd Annual Design Automation Conference*, DAC '06, pages 466–471, New York, NY, USA, 2006. ACM.

Guilherme Torri, M.E. Brinson, F. Schreuder, B. Roucaries, C. Novak, and R. Crozier.

Building a second generation Qucs GPL circuit simulator: package structure, simulation features and compact device modelling capabilities.
`http://www.mos-ak.org/london_2014/presentations/09_Mike_Brinson_MOS-AK_London_2014.pdf`, March 2014.