WE LOOK AFTER THE EARTH BEAT

Diplomverteidigung

Reliable high-speed data transfers on satellites across Wizard-Link

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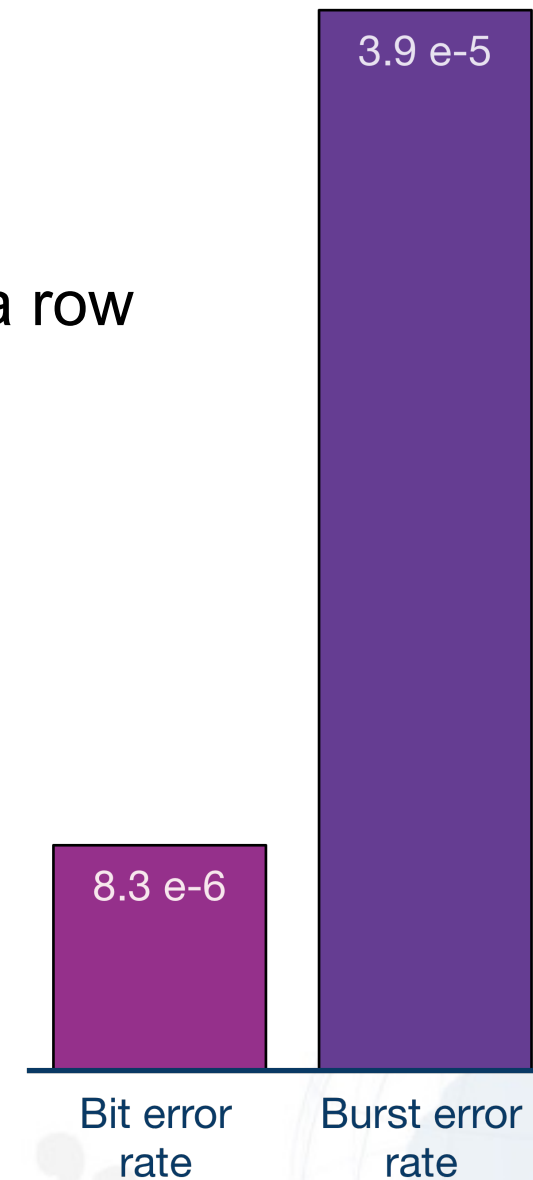
ThalesAlenia
Space
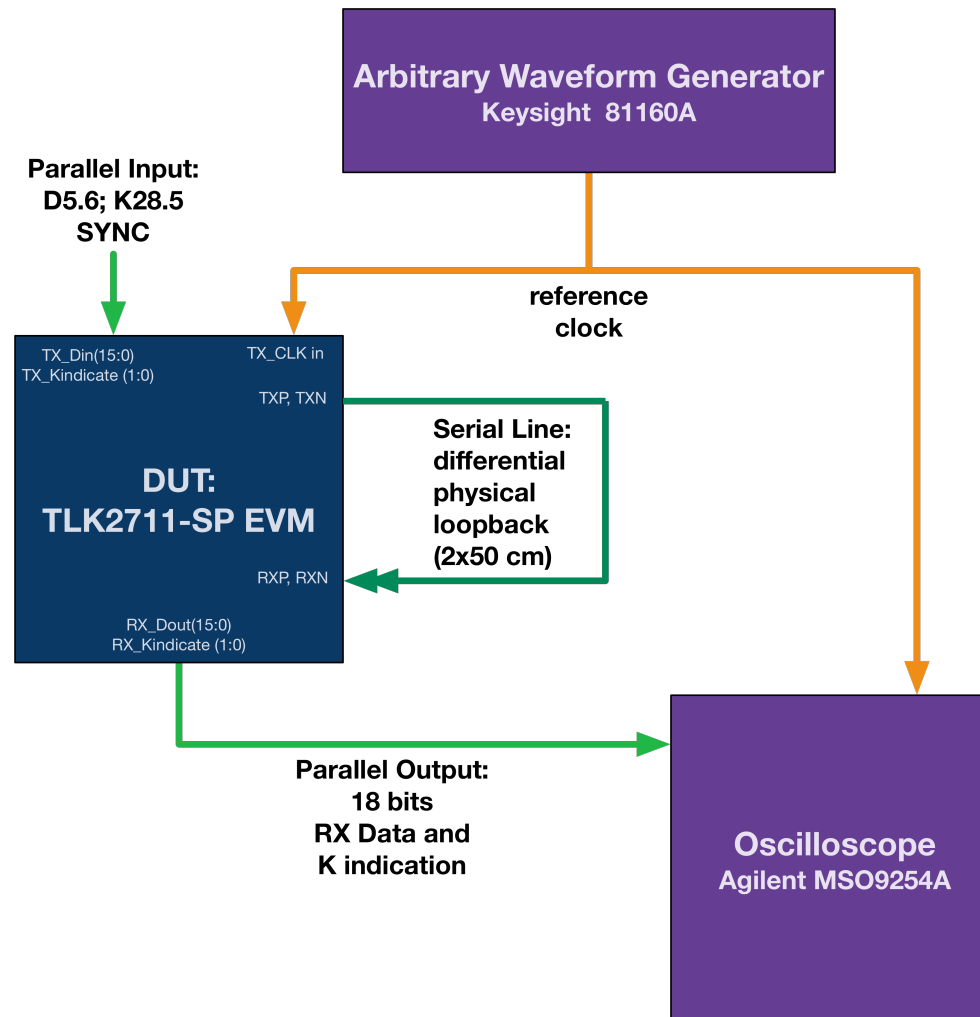A Thales / Finmeccanica Company

Radiation and the TLK2711-SP

- Two mechanisms (see [1]):
  - Bit errors effecting 1-8 bits
  - Burst errors effecting 100-1000 bits in a row
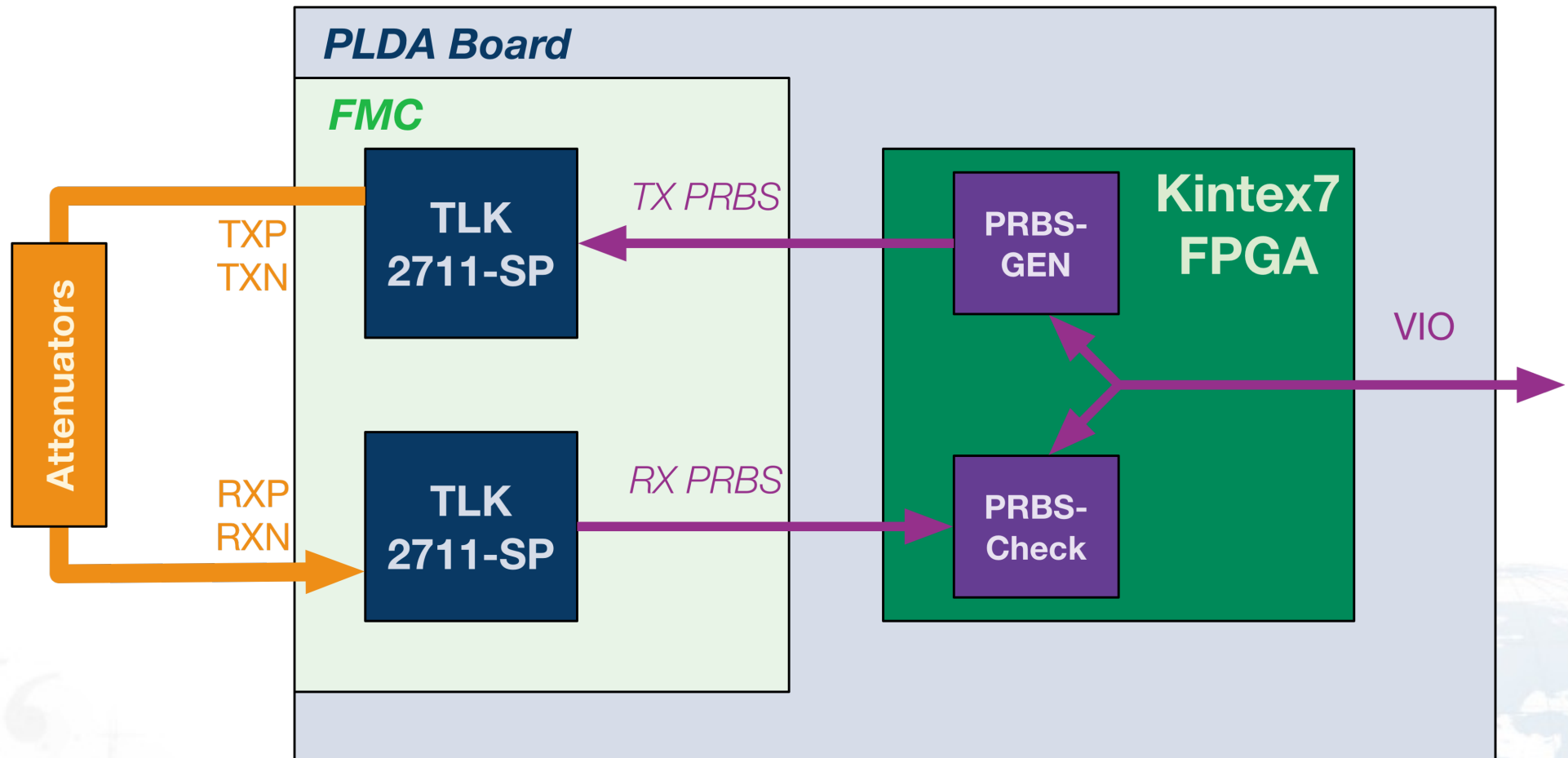
- overall roughly $4.7 \cdot 10^{-5}$ events/s

3.9 e-5

8.3 e-6

Bit error rate

Burst error rate

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Byte Alignment Recovery Test

Arbitrary Waveform Generator
Keysight 81160A

Parallel Input:
D5.6; K28.5
SYNC

TX_Din(15:0)
TX_Kindicate (1:0)

TX_CLK in

TXP, TXN

reference
clock

DUT:
TLK2711-SP EVM

Serial Line:
differential
physical
loopback
(2x50 cm)

RXP, RXN

RX_Dout(15:0)
RX_Kindicate (1:0)

Parallel Output:
18 bits
RX Data and
K indication

Oscilloscope
Agilent MSO9254A

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Byte Alignment Recovery Test

8 ns clock slip with 10dB line attenuation

LOS- Behaviour Test

Error Model

- EM- and other influences negated by shielding and proper wiring

- Radiation most significant error source
- Nominal error rate negligible

- Overall Error rate $< 5 \cdot 10^{-5}$ events/s
- Composed of Bit- and Burst errors

Forward Error Correction:

not feasible ➔ Burst errors

Hybrid Scheme:

no ➔ more Burst errors than Bit errors

Bit errors affect single bits, or 8 bits at once

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Comparison of ARQs

$$E(x) = \frac{L_{data}(x)}{(L_{frame}(x) + L_{gap} + L_{wait}) + (p_r(x) * (L_{frame}(x) + L_{gap} + L_{wait} + L_{loss}))}$$
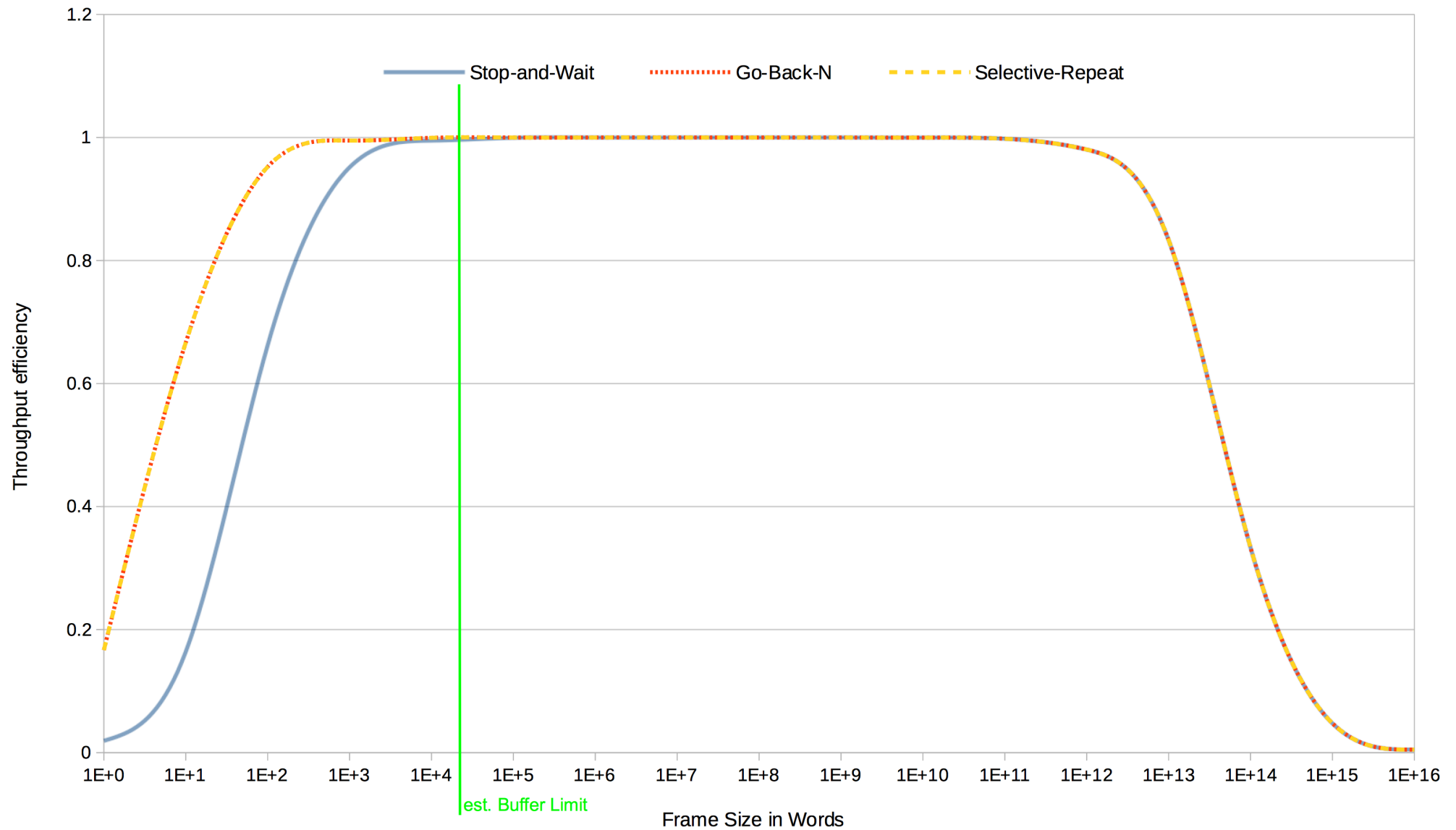
with:

$$L_{frame}(x) = L_{data}(x) + L_{head} + L_{foot}$$

$$p_r(x) = \frac{L_{frame}(x) * 16 \frac{bit}{word}}{n_{error}} * 1 \, error$$

ARQ-Method	L_{gap} (word)	L_{wait} (word)	L_{head} (word)	L_{foot} (word)	L_{loss} (word)
Stop-and-Wait	2	47	1	2	0
Go-Back-N	2	0	1	2	50
Selective-Repeat	2	0	1	2	0

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Comparison of ARQs

Frame Layout

Data line:

... | CRC | IDLE | IDLE | ID | Data | Data | ... | Data | Data | CRC | CRC | IDLE | IDLE | ID | Data | ...

Frame

ACK line:

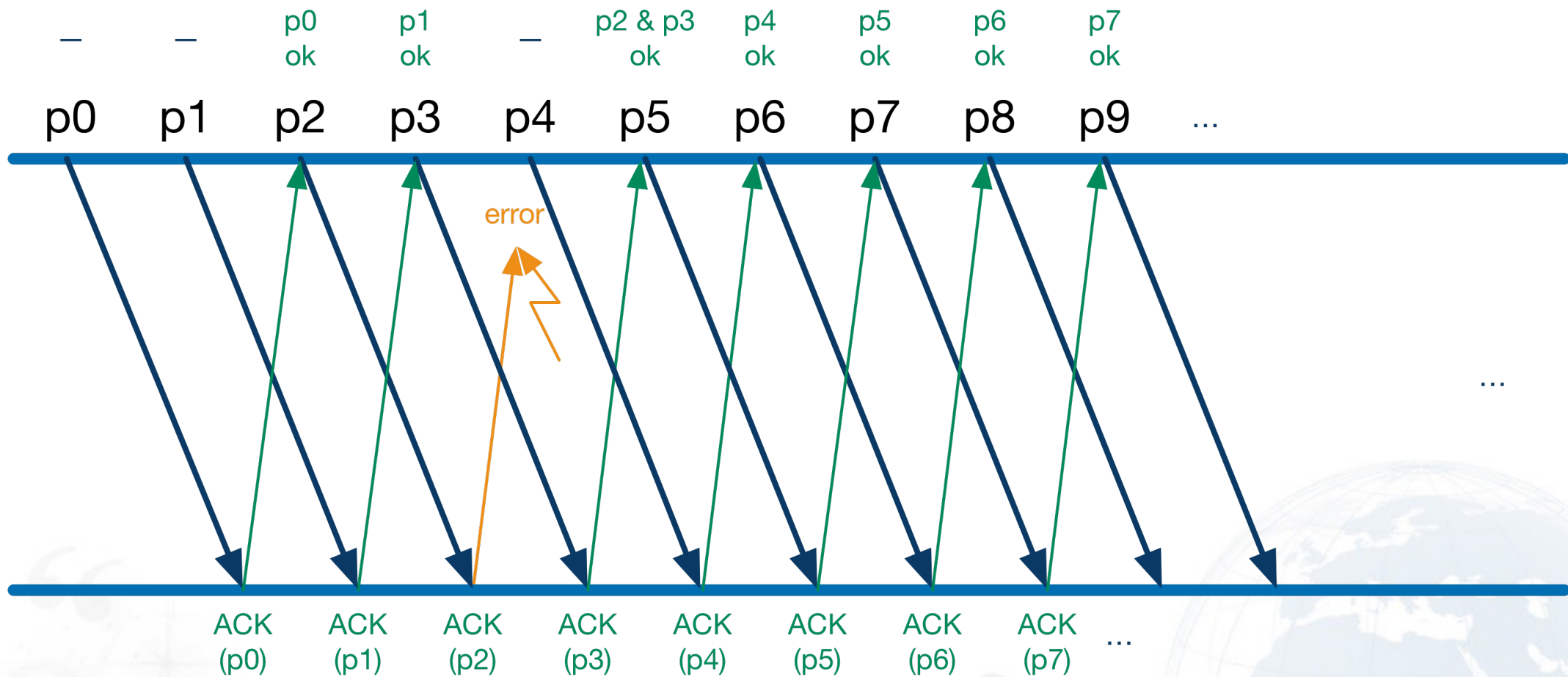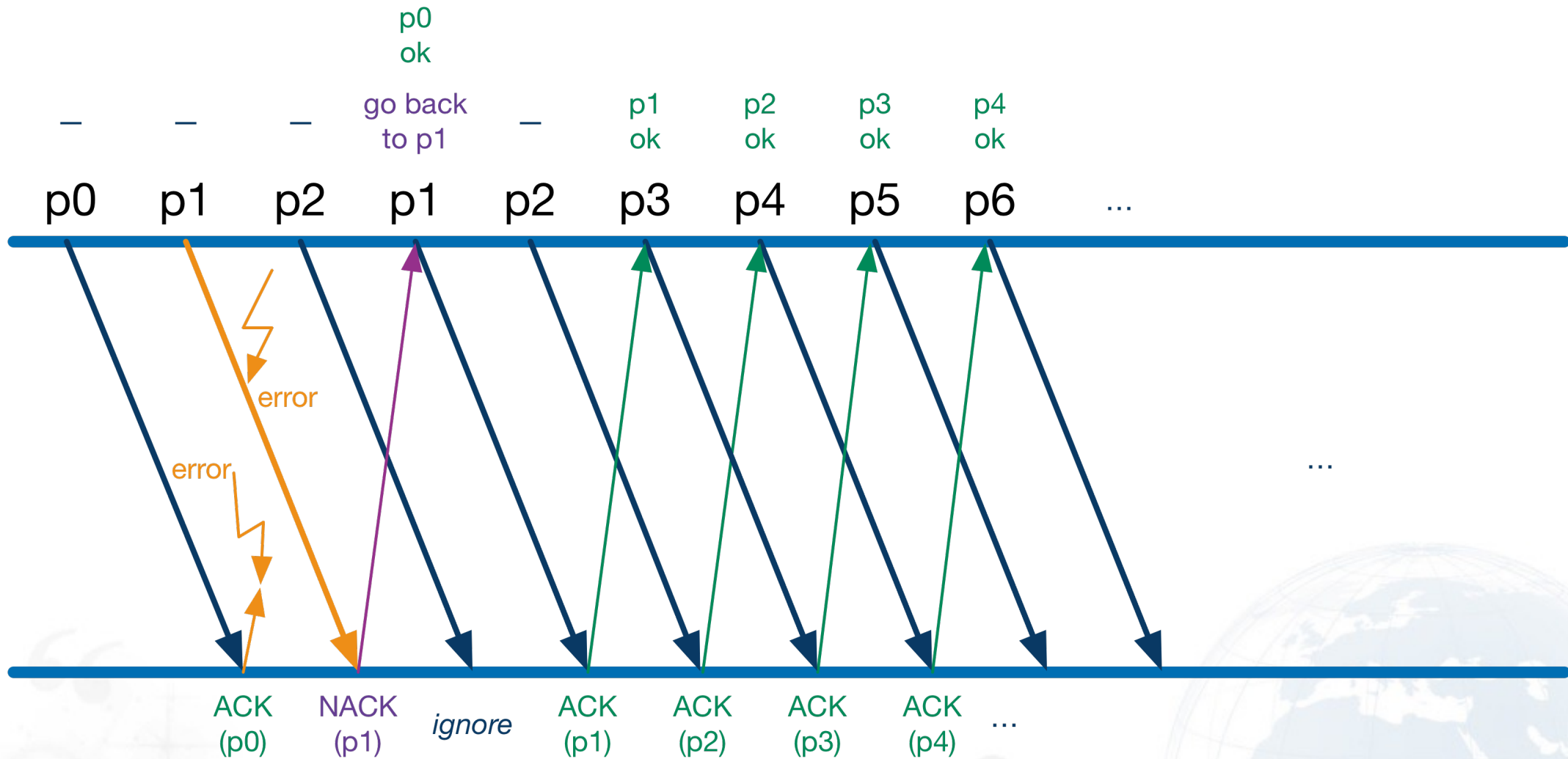... | IDLE | ACK | IDLE | IDLE | ... | IDLE | NACK | IDLE | ... | IDLE | BufF | IDLE | ...

Control Chars chosen with increased HD to data words etc.

- CRC-32C over frame data
    - Max Frame size: HD = 4
    - Smaller Frames: HD > 6
    - Risk for missed Burst-Error < $2.9 \cdot 10^{-39}$

- Invalid 10b-Code indication from TLK
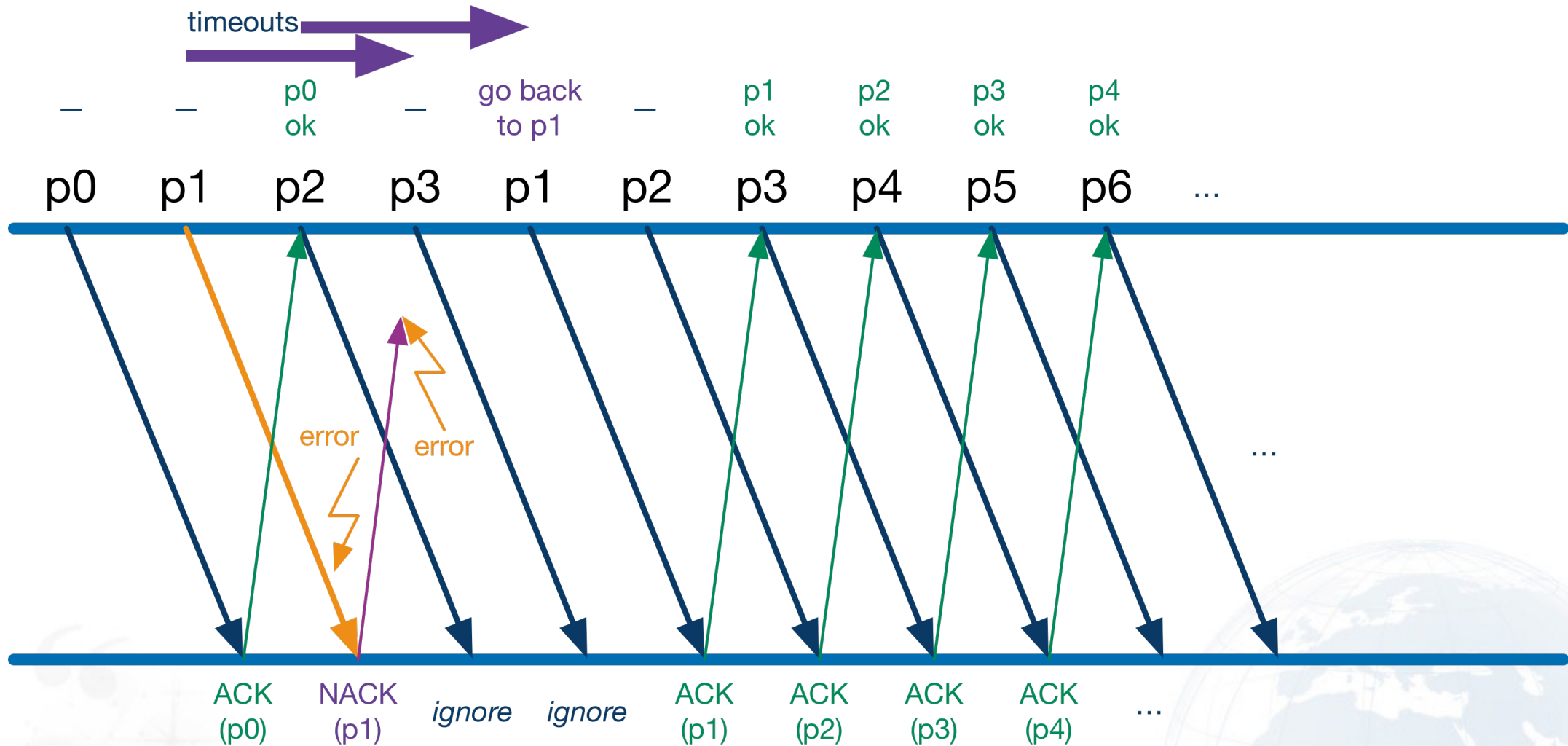- Unused K-Chars

- Frame ID encoded with Hamming (8,4)
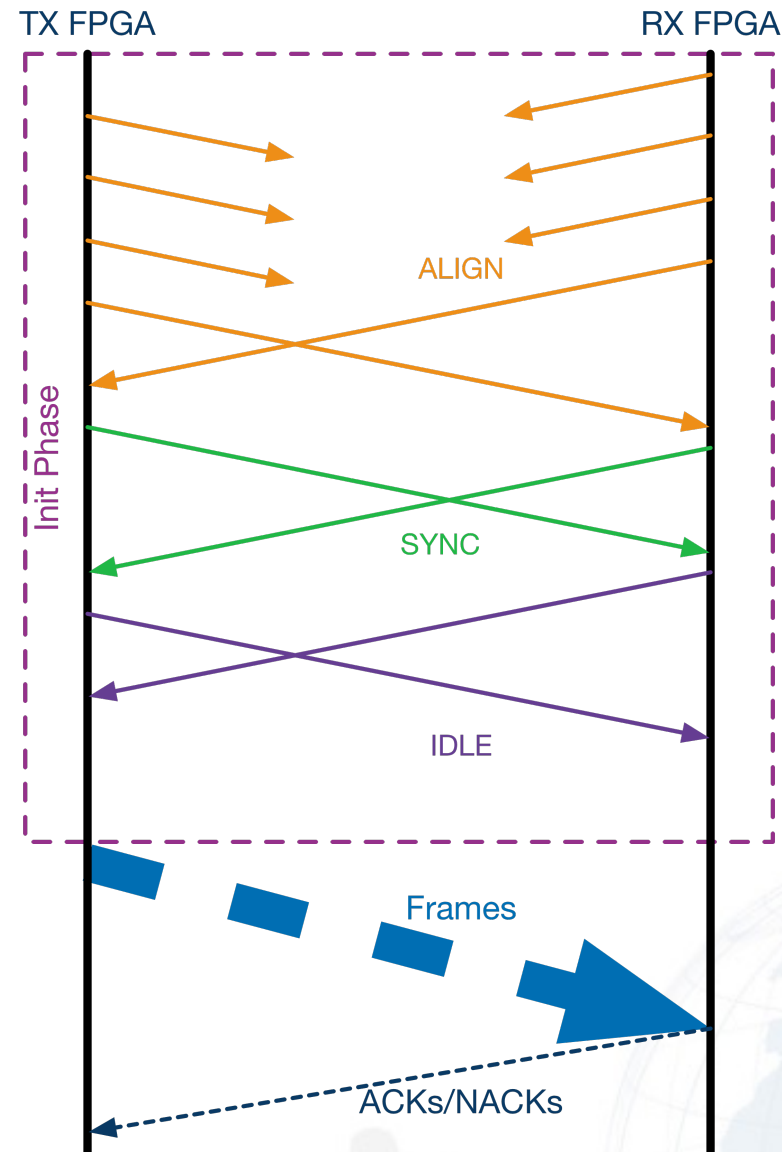
Faulty ACK-Line - dropped ACK

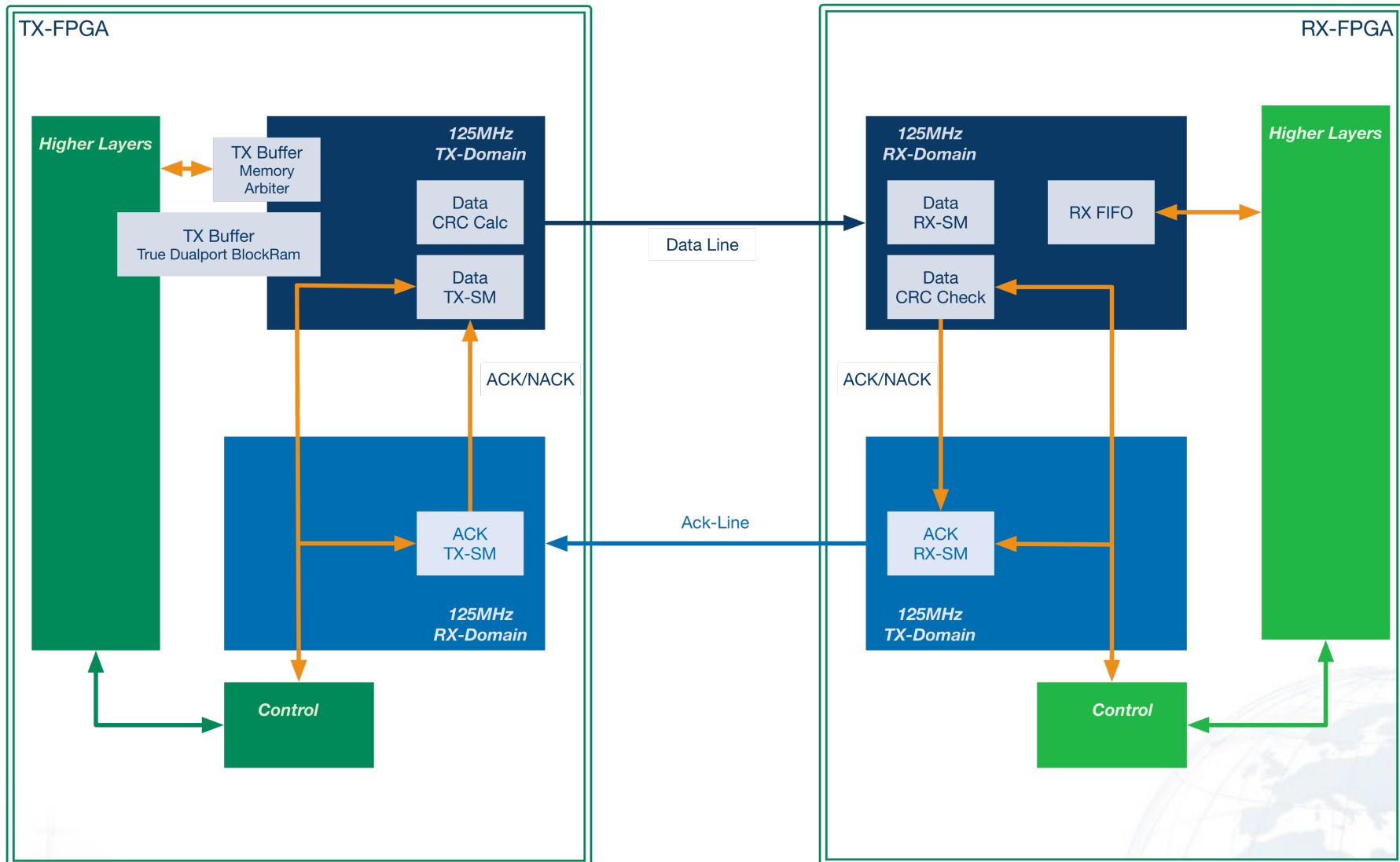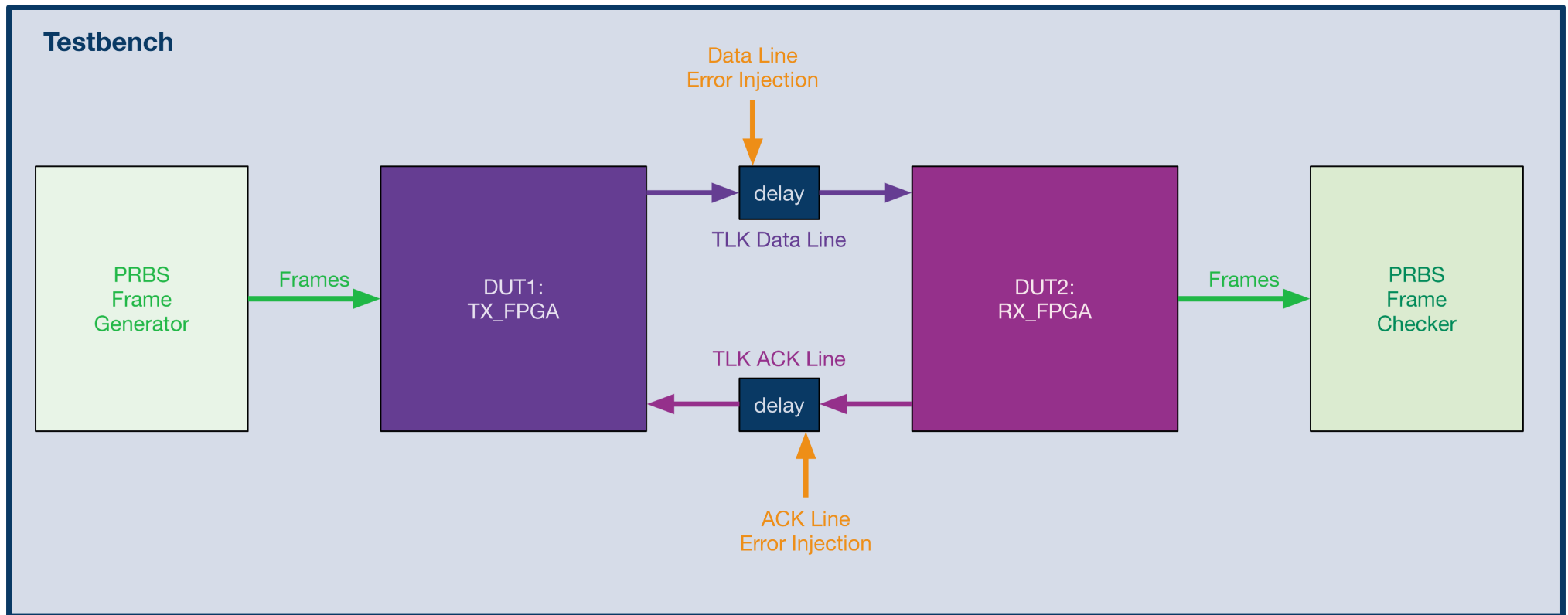# Faulty ACK-Line - dropped ACK before NACK

Faulty ACK-Line - dropped NACK

- Needed for active receiver transitions after PoR

- Communicate reinit to other side

- For reinit: two step strategy

Implementation - Clock Domains

TX-FPGA

RX-FPGA

Higher Layers

TX Buffer Memory Arbiter

TX Buffer True Dualport BlockRam

125MHz TX-Domain

Data CRC Calc

Data TX-SM

Data Line

125MHz RX-Domain

Data RX-SM

RX FIFO

Data CRC Check

Higher Layers

ACK/NACK

ACK/NACK

ACK TX-SM

125MHz RX-Domain

Ack-Line

ACK RX-SM

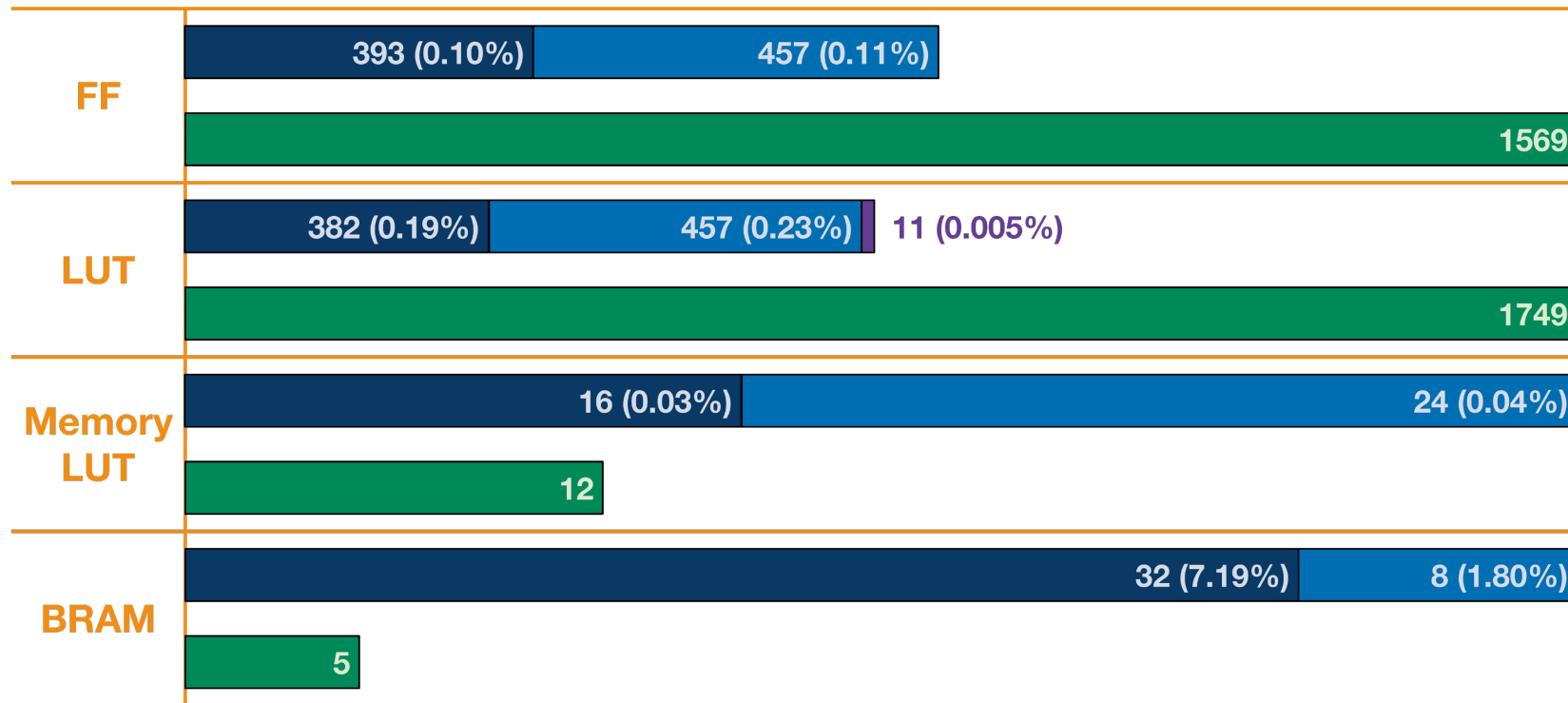*125MHz TX-Domain*

Control

Control

Clock Domain Crossing

Currently incomplete

Test of Implementation

- Startup initialisation and nominal data transfer

- Bit error(s) within one frame
- Burst error within one frame

- Single dropped ACK, single dropped NACK
- Sequence of dropped ACKs, NACKs

- Reinit without reset due to blocked Data or ACK-line
- Reinit with reset

Resource Usage

FF
- 393 (0.10%)
- 457 (0.11%)
- 1569

LUT
- 382 (0.19%)
- 457 (0.23%)
- 11 (0.005%)
- 1749

Memory LUT
- 16 (0.03%)
- 24 (0.04%)
- 12

BRAM
- 32 (7.19%)
- 8 (1.80%)
- 5

Legend: TX Block | RX Block | Other | Space Fibre IP Core (single channel, 5 GBit/s, optimised)

% in relation to available resources of the Kintex 7 (XC7K325T)

(Space Fibre unknown Virtex 6)

- 5 BUFG per TX, RX (30% overall)
- 1 MMCM (10%), 2 PLL (20%)

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Conclusion

- Error Model:
  - Mostly due to Radiation
  - More burst- than bit-errors

- Protocol:
  - Modified Go-back-N with CRC-32C
  - Init, reinit phase
  - 5% overhead w. 200 byte frames, <1% w. 1000 bytes
  - Encapsulation of all foreseen errors

- Implementation:
  - Clock domain isolation
  - slim implementation, small footprint

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Next Steps

- Complete and perform System Tests

- Check Test-Scenarios for full coverage
- Validation and Verification in accordance to ECSS
- Tests in Hardware

Sources

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- **"Using the TLK2711-SP With Minimal Protocol"**. Texas Instruments: Application Report, last revised Aug.2011, . – see http://www.ti.com/lit/an/ sgla001a/sgla001a.pdf

- **"Radiation Models and Hard- ware Design"** Some, Raphael, presentation in 2002, 2002. – see http://webhost.laas.fr/TSF/IFIPWG/Workshops&Meetings/44/W2/02-Some.pdf

- **"Single Event Effects and Total Dose Test Results for TI TLK2711 Transceiver"** Koga, R. ; Yu, P. ; George, J., In: Radiation Effects Data Workshop, 2008 IEEE, 2008, S. 69–75

- **"Checksum and CRC Data Integrity, Techniques for Aviation. Carnegie Mellon University"** - Koopman, Philip: Tutorial; May 9, 2012, . – see https://users. ece.cmu.edu/ ˜koopman/pubs/KoopmanCRCWebinar9May2012.pdf

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